TOSHIBA COMPANION CHIP FOR TX3922

PLUM2

1. General Description

The PLUM2 is a companion chip for TX3922. The PLUM2 is connected to TX3922 to build advanced portable information terminal systems.

Figure 1 shows a block diagram of PLUM2. The PLUM2 consists of a LCD / CRT controller, PCMCIA controller, SmartMedia controller, I/O bus controller and USB controller.

2. Features

(1) LCD / CRT Controller

LCDC

Panel:	STN / DSTN / TFT		
Display:	640 x 240, 640 x 480, 800 x 600		
Pixel:	8bit / pixel or 16bit / pixel		
Color:	STN/DSTN	256 color out of 64K	8bit / pixel
		64K color	16bit / pixel
	TFT	256 color out of 256K	8bit / pixel
		64K color	16bit / pixel
Mono:	STN/DSTN	64 grayscale	8bit / pixel

CRT

Display:	640 x 480, 800 x 600		
Pixel:	8bit / pixel or 16bit / pixel		
Color:		256 color out of 256K	8bit / pixel
		64K color	16bit / pixel
RAMDAC:	Analog RGB = 6:6:6		

Function

Simultaneous display CRT / LCD: Mirrored Output / Ghost Output

BitBlt accelerator

VRAM: SGRAM (8Mbit / 16Mbit / 32Mbit)

Power control function using CKE / CLK

(2) PCMCIA Controller

Compatible with the PCMCIA V2.1/JEIDA V4.2 specification (does not support Card Bus and ZV port).

3V / 5V I/O buffer

2 slots

(3) SmartMedia Controller

3V / 5V I/O buffer

1 slot

(4) I / O bus Controller

ISA-like bus

8 / 16bit bus

(5) USB Host Controller

Conforms to OHCI specification

2 ports

3. System Configuration

3.1. System Block Diagram

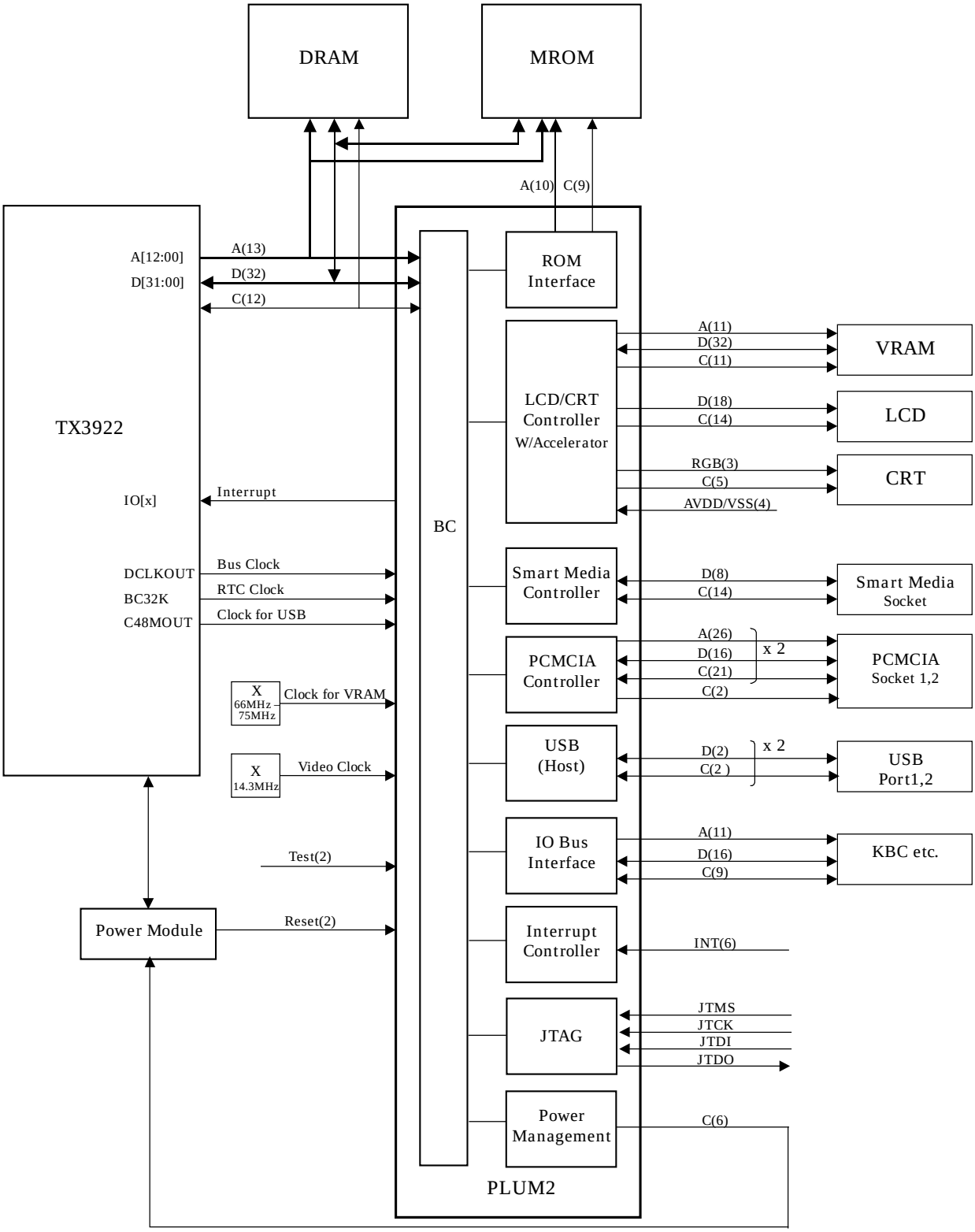
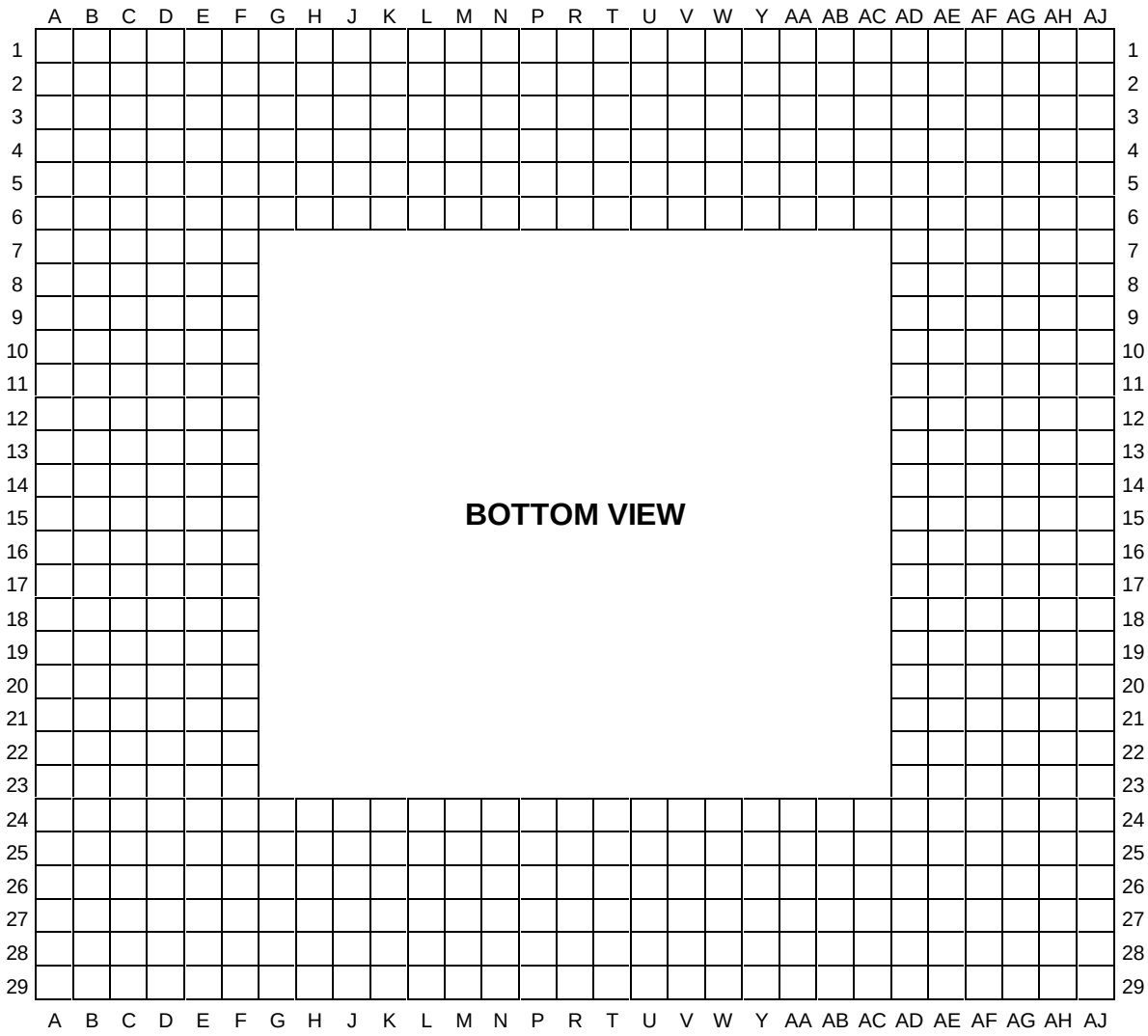


Figure 1 System Block Diagram

4. Pin Description

4.1. Pin Assignment



*Active-low signal

NO	PIN NAME	NO	PIN NAME	NO	PIN NAME	NO	PIN NAME	NO	PIN NAME
A01	MROMA[17]	C01	IO5BHE*	E01	IO5ADR[09]	G01	IO5ADR[01]	M01	IO5DAT[00]
A02	MROMA[14]	C02	IO5WR*	E02	IO5ADR[10]	G02	IO5ADR[02]	M02	IO5DAT[01]
A03	MRCS[06]*	C03	MROMA[19]	E03	IO5CS[04]*	G03	IO5ADR[07]	M03	IO5DAT[02]
A04	MRCS[03]*	C04	MROMA[15]	E04	IO5RD*	G04	IO5CS[01]*	M04	IO5DAT[03]
A05	DBGCS*	C05	MRCS[07]*	E05	VDDS	G05	VDD	M05	VDD
A06	RMCS03*	C06	MRCS[02]*	E06	VDD	G06	GND	M06	GND
A07	RMDAT[06]	C07	DBGWAIT	E07	NC	G24	APLLVSS2	M24	GND
A08	CLKBUS	C08	RMMCS1*	E08	VDDS	G25	VDDS	M25	VDDS
A09	RMDAT[04]	C09	RMDAT[05]	E09	VDD	G26	LCDGD[16]	M26	VRCS[00]*
A10	RMDAT[00]	C10	RMDAT[03]	E10	VDDS	G27	VRDAT[28]	M27	VRCS[01]*
A11	RMDAT[13]	C11	RMDAT[15]	E11	NC	G28	VRDAT[27]	M28	VRDQM[00]
A12	RMDAT[09]	C12	RMDAT[11]	E12	VDD	G29	VRDAT[26]	M29	VRDQM[01]
A13	RMALE	C13	RMCS00*	E13	VDDS	H01	IO5DAT[13]	N01	IO5INT[00]
A14	RMADR[10]	C14	RMADR[12]	E14	VDD	H02	IO5ADR[00]	N02	IO5INT[01]
A15	RMADR[06]	C15	RMADR[08]	E15	VDDS	H03	IO5ADR[03]	N03	IO5INT[03]
A16	RMADR[05]	C16	RMADR[03]	E16	NC	H04	IO5ADR[08]	N04	IO5INT[02]
A17	RMADR[01]	C17	RMCAS[02]*	E17	VDD	H05	NC	N05	VDDS
A18	RMDAT[24]	C18	RMCAS[00]*	E18	VDDS	H06	GND	N06	GND
A19	RMDAT[26]	C19	RMDAT[29]	E19	VDD	H24	GND	N24	GND
A20	RMDAT[28]	C20	RMDAT[17]	E20	VDDS	H25	NC	N25	VDD
A21	RMDAT[16]	C21	RMDAT[21]	E21	VDD	H26	LCDGD[17]	N26	TEST[1]
A22	RMDAT[19]	C22	LCDGD[07]	E22	VDDS	H27	VRDAT[25]	N27	VRADR[10]
A23	RMDAT[23]	C23	LCDGD[04]	E23	NC	H28	VRDAT[24]	N28	VRDQM[02]
A24	CLKMEM	C24	LCDGD[01]	E24	VDD	H29	VRDAT[23]	N29	VRDQM[03]
A25	LCDGD[02]	C25	LCDDEN	E25	APLLVDD	J01	IO5DAT[10]	P01	TEST[0]
A26	LCDFP	C26	BKLOFF	E26	PWRCNT[02]	J02	IO5DAT[12]	P02	IO3INT[01]
A27	CLKVIDEO	C27	APLLLP	E27	LCDGD[12]	J03	IO5DAT[15]	P03	IO3INT[00]
A28	IO5CLRL*	C28	PWRCNT[00]	E28	LCDGD[13]	J04	IO5ADR[04]	P04	INTO
A29	APLLVSS1	C29	LCDGD[09]	E29	VRDAT[31]	J05	VDDS	P05	NC
B01	MROMA[21]	D01	IO5CS[02]*	F01	IO5ADR[05]	J06	GND	P06	GND
B02	MROMA[18]	D02	IO5CS[03]*	F02	IO5ADR[06]	J24	GND	P24	GND
B03	MROMA[13]	D03	MROMA[22]	F03	IO5CS[00]*	J25	VDD	P25	NC
B04	MRCS[05]*	D04	MROMA[20]	F04	IO5WAIT*	J26	VRDAT[22]	P26	VRADR[09]
B05	MRCS[00]*	D05	MROMA[16]	F05	NC	J27	VRDAT[21]	P27	VRADR[08]
B06	RMMWA*	D06	MROMOE*	F06	NC	J28	VRDAT[20]	P28	VRADR[07]
B07	RMDAT[07]	D07	MRCS[04]*	F07	GND	J29	VRDAT[19]	P29	VRADR[06]
B08	RCLR*	D08	MRCS[01]*	F08	NC	K01	IO5DAT[06]	R01	VDD
B09	PCLR*	D09	RMMCS0*	F09	GND	K02	IO5DAT[09]	R02	SMCIN*
B10	RMDAT[01]	D10	CLKRTC	F10	GND	K03	IO5DAT[11]	R03	SMCD*
B11	RMDAT[14]	D11	RMDAT[02]	F11	GND	K04	IO5DAT[14]	R04	SMDT[04]
B12	RMDAT[10]	D12	RMDAT[12]	F12	GND	K05	VDD	R05	UVCC3
B13	RMRD*	D13	RMDAT[08]	F13	GND	K06	GND	R06	GND
B14	RMADR[11]	D14	RMWT*	F14	NC	K24	GND	R24	GND
B15	RMADR[07]	D15	RMADR[09]	F15	GND	K25	VDDS	R25	VDDS
B16	RMADR[02]	D16	RMADR[04]	F16	GND	K26	VRDAT[18]	R26	VRADR[05]
B17	RMADR[00]	D17	RMCAS[03]*	F17	GND	K27	VRDAT[17]	R27	VRADR[04]
B18	RMCAS[01]*	D18	RMDAT[25]	F18	GND	K28	VRDAT[16]	R28	VRADR[03]
B19	RMDAT[27]	D19	RMDAT[30]	F19	NC	K29	VRCKE	R29	VRADR[02]
B20	RMDAT[31]	D20	RMDAT[20]	F20	GND	L01	IO5DAT[04]	T01	SMDT[05]
B21	RMDAT[18]	D21	LCDGD[06]	F21	GND	L02	IO5DAT[05]	T02	SMDT[03]
B22	RMDAT[22]	D22	LCDGD[03]	F22	NC	L03	IO5DAT[07]	T03	SMDT[06]
B23	LCDGD[08]	D23	LCDGD[00]	F23	GND	L04	IO5DAT[08]	T04	SMDT[02]
B24	LCDGD[05]	D24	LCDDSP	F24	NC	L05	VDDS	T05	VDD
B25	LCDCLK	D25	LCDOFF	F25	NC	L06	NC	T06	NC
B26	LCDLP	D26	APLLRO	F26	LCDGD[14]	L24	NC	T24	NC
B27	IO5CLRH	D27	PWRCNT[01]	F27	LCDGD[15]	L25	VDD	T25	VDD
B28	APLLAGS	D28	LCDGD[11]	F28	VRDAT[30]	L26	VRRAS*	T26	VRADR[00]
B29	IO5PWR	D29	LCDGD[10]	F29	VRDAT[29]	L27	VRCAS*	T27	VRDAT[00]
						L28	VRWE*	T28	VRDAT[01]
						L29	VRCLK	T29	VRADR[01]

*Active-low signal

NO	PIN NAME	NO	PIN NAME	NO	PIN NAME	NO	PIN NAME	NO	PIN NAME
U01	SMDT[07]	AB01	C2VCC5*	AD01	C2VS[01]	AF01	C2DATL[07]	AH01	C2IOR*
U02	SMDT[01]	AB02	C2CD[02]*	AD02	C2DATH[03]	AF02	C2DATH[07]	AH02	C2ADR[17]
U03	SMVS	AB03	C2DATL[04]	AD03	C2DATH[05]	AF03	C2ADR[09]	AH03	C2ADR[20]
U04	SMDT[00]	AB04	C2DATL[06]	AD04	C2OEN*	AF04	C2ADR[18]	AH04	C2ADR[22]
U05	UVCC3	AB05	VDD	AD05	NC	AF05	C2WEN*	AH05	C2ADR[24]
U06	GND	AB06	NC	AD06	NC	AF06	C2ADR[21]	AH06	C2ADR[05]
U24	GND	AB24	NC	AD07	GND	AF07	C2ADR[23]	AH07	C2ADR[03]
U25	VDDS	AB25	VDDS	AD08	NC	AF08	C2ADR[25]	AH08	C2REG*
U26	VRDAT[05]	AB26	LCDLUM[1]	AD09	GND	AF09	C2ADR[04]	AH09	C2BVD[01]
U27	VRDAT[04]	AB27	DACG	AD10	GND	AF10	C2BVD[02]	AH10	C2DATL[01]
U28	VRDAT[03]	AB28	IREF	AD11	GND	AF11	C2DATH[01]	AH11	C2WP
U29	VRDAT[02]	AB29	LCDLEV[3]	AD12	NC	AF12	USBD2M	AH12	NC
V01	SMWP*	AC01	C2CD[01]*	AD13	GND	AF13	USBD1P	AH13	USBOC1*
V02	SMRDY	AC02	C2VS[02]	AD14	NC	AF14	CLKUSB	AH14	USBPWR2*
V03	SMWE*	AC03	C2DATL[05]	AD15	GND	AF15	C1VPPG	AH15	C1VCC5*
V04	SMRE*	AC04	C2EN[01]*	AD16	GND	AF16	C1DATL[05]	AH16	C1DATL[04]
V05	VDD	AC05	UVCC2	AD17	GND	AF17	C1DATL[07]	AH17	C1DATL[06]
V06	GND	AC06	GND	AD18	GND	AF18	C1ADR[10]	AH18	C1EN[01]*
V24	GND	AC24	GND	AD19	NC	AF19	C1IOW*	AH19	C1OEN*
V25	VDD	AC25	VDD	AD20	GND	AF20	C1ADR[14]	AH20	C1ADR[09]
V26	VRDAT[09]	AC26	JTCK	AD21	GND	AF21	C1ADR[16]	AH21	C1ADR[13]
V27	VRDAT[08]	AC27	LCDLUM[0]	AD22	NC	AF22	C1ADR[07]	AH22	C1WEN*
V28	VRDAT[07]	AC28	EXTVREF	AD23	GND	AF23	C1ADR[05]	AH23	C1BSY*
V29	VRDAT[06]	AC29	VREF	AD24	NC	AF24	C1ADR[03]	AH24	C1ADR[15]
W01	SMALE			AD25	NC	AF25	C1BVD[02]	AH25	C1ADR[24]
W02	SMCE*			AD26	C1CD[02]*	AF26	C1DATH[00]	AH26	C1RST
W03	SMCLE			AD27	JTMS	AF27	C1DATH[01]	AH27	C1ADR[02]
W04	SMPWR2*			AD28	JTDI	AF28	C1VS[01]	AH28	C1BVD[01]
W05	NC			AD29	JTDO	AF29	C1VS[02]	AH29	C1DATL[01]
W06	GND			AE01	C2DATH[06]	AG01	C2ADR[10]	AJ01	C2ADR[08]
W24	GND			AE02	C2DATH[04]	AG02	C2ADR[11]	AJ02	C2ADR[14]
W25	NC			AE03	C2EN[02]*	AG03	C2ADR[13]	AJ03	C2BSY*
W26	VRDAT[14]			AE04	C2IOW*	AG04	C2ADR[19]	AJ04	C2ADR[15]
W27	VRDAT[13]			AE05	VDD	AG05	C2ADR[16]	AJ05	C2ADR[07]
W28	VRDAT[12]			AE06	UVCC2	AG06	C2ADR[12]	AJ06	C2RST
W29	VRDAT[10]			AE07	NC	AG07	C2ADR[06]	AJ07	C2ADR[02]
Y01	SMWPIN*			AE08	VDD	AG08	C2WAIT*	AJ08	C2ADR[00]
Y02	SMSTDN*			AE09	UVCC2	AG09	C2ADR[01]	AJ09	C2DATH[00]
Y03	SMPWR1*			AE10	VDD	AG10	C2DATL[00]	AJ10	C2DATL[02]
Y04	CDAUD			AE11	NC	AG11	C2DATH[02]	AJ11	UVCC2
Y05	VDDS			AE12	VDD	AG12	USBD2P	AJ12	NC
Y06	GND			AE13	NC	AG13	USBD1M	AJ13	USBOC2*
Y24	APVS[02]			AE14	VDDS	AG14	USBPWR1*	AJ14	CDSHDN*
Y25	APVD[02]			AE15	VDD	AG15	C1VPVC	AJ15	C1VCC3*
Y26	LCDLEV[4]			AE16	NC	AG16	C1DATH[03]	AJ16	C1DATL[03]
Y27	LCDLEV[1]			AE17	UVCC1	AG17	C1DATH[05]	AJ17	C1DATH[04]
Y28	VRDAT[15]			AE18	VDD	AG18	C1DATH[07]	AJ18	C1DATH[06]
Y29	VRDAT[11]			AE19	VDD	AG19	C1ADR[11]	AJ19	C1EN[02]*
AA01	C2VCC3*			AE20	UVCC1	AG20	C1ADR[08]	AJ20	C1IOR*
AA02	C2VPVC			AE21	VDD	AG21	C1ADR[19]	AJ21	C1ADR[17]
AA03	C2VPPG			AE22	UVCC1	AG22	C1ADR[22]	AJ22	C1ADR[18]
AA04	C2DATL[03]			AE23	NC	AG23	C1ADR[23]	AJ23	C1ADR[20]
AA05	UVCC2			AE24	VDD	AG24	C1ADR[25]	AJ24	C1ADR[21]
AA06	GND			AE25	UVCC1	AG25	C1WAIT*	AJ25	C1ADR[12]
AA24	APVS[01]			AE26	C1DATL[02]	AG26	C1ADR[01]	AJ26	C1ADR[06]
AA25	APVD[01]			AE27	C1CD[01]*	AG27	C1DATL[00]	AJ27	C1ADR[04]
AA26	DACB			AE28	VSYNC	AG28	C1DATH[02]	AJ28	C1REG*
AA27	DACR			AE29	HSYNC	AG29	C1WP	AJ29	C1ADR[00]
AA28	LCDLEV[2]								
AA29	LCDLEV[0]								

4.2. Pin Function

TX3922 System Bus Interface

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
RMDAT<31:00>	I/O	3.3V	System data bus	Hi-Z	
RMADR<12:00>	I	3.3V	Multiplexed address bus	I	
RMALE	I	3.3V	Address latch enable for upper address bus PLUM2 latches upper address internally and generates **MROMA<23:13>** for ROM interface.	I	
RMRD*	I	3.3V	Read signal	I	
RMWT*	I	3.3V	Write signal	I	
RMCS03*	I	3.3V	Chip select 3	I	
RMCS00*	I	3.3V	Chip select 0	I	
RMCAS<03:00>*	I	3.3V	CAS and byte enable signal	I	
RMMCS1*	I	3.3V	32 bit bus chip select 1	I	
RMMCS0*	I	3.3V	32 bit bus chip select 0	I	
RMMWA*	O	3.3V	32 bit bus wait signal	H	

* Active-low signal

ROM Interface

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
MROMA<22:13>	O	3.3V	Mask ROM upper address These signals output low level if RCLR* is asserted.	(*1)	
MRCS<07:01>*	O	3.3V	Mask ROM chip select signals These signals output low level if RCLR* is asserted.	(*2)	
MRCS<00>* / MROMA<23>	O	3.3V	Mask ROM chip select signal (MROMSL=00,01) or MROMA23 signal (MROMSL=10) These signals output low level if RCLR* is asserted.	(*2)	
MROMOE*	O	3.3V	Mask ROM output enable This signal outputs low level if RCLR* is asserted.	(*3)	

* Active-low signal

(*1) These signals output low level if RCLR* is asserted.
They output the levels of RMADR<09:00> if RCLR* is not asserted.

(*2) These signals output low level if RCLR* is asserted.
They output the levels which depend on RMCS00* and RMADR<12:00> if RCLR* is not asserted.

(*3) This signal outputs low level if RCLR* is asserted.
It outputs the level which depends on RMCS0*, RMRD* and RMADR<12:00> if RCLR* is not asserted.

Video RAM Interface

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
VRDAT<31:00>	I/O	3.3V	VRAM data	Hi-Z	(*4)
VRADR<10:00>	O	3.3V	VRAM address	L	(*5)
VRRAS*	O	3.3V	VRAM row address strobe	L	(*5)
VRCAS*	O	3.3V	VRAM column address strobe	L	(*5)
VRWE*	O	3.3V	VRAM write enable	L	(*5)
VRCLK	O	3.3V	VRAM clock	L	(*5)
VRCS<01:00>*	O	3.3V	VRAM chip select	L	(*5)
VRDQM<03:00>	O	3.3V	VRAM output enable/data mask	L	(*5)
VRCKE	O	3.3V	VRAM clock enable	L	(*5)

* Active-low signal

(*4) These signals are in a Hi-Z mode if VRAM is in a self-refresh mode.

(*5) These signals output low level if VRAM is in a self-refresh mode.

LCD Interface

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
LCDGD<17:00>	O	3.3V	Graphics/video output	L	(*6)
LCDCLK	O	3.3V	LCD clock	L	(*6)
LCDDEN	O	3.3V	LCD display enable	L	(*6)
LCDLP	O	3.3V	Line pulse	L	(*6)
LCDFP	O	3.3V	Field pulse	L	(*6)
LCDDSP	O	3.3V	LCD display on This signal outputs the level of LCDDSP bit in Power Control Register.	L	(*6)
LCDOFF	O	3.3V	LCD power off This signal outputs inverted level of LCDPWR bit in Power Control Register.	H	
BKLOFF	O	5V	Back light off This signal outputs inverted level of BKLIGHT bit in Power Control Register.	H	
LCDLEV<4:0>	O	OD	LCD contrast These signals output the levels of LCD Level Control Register.	L	
LCDLUM<1:0>	O	5V	LCD luminance These signals output the levels of LCD Luminance Control Register.	L	

* Active-low signal

OD: Open Drain

(*6) These signals output low level if LCDEN bit of Power Control Register is 0.

CRT Interface

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
HSYNC	O	5V	H-Sync	L	(*7)
VSYNC	O	5V	V-Sync	L	(*8)
DACR	O	-	DAC analog output R	Analog Signal	
DACG	O	-	DAC analog output G	Analog Signal	
DACB	O	-	DAC analog output B	Analog Signal	
IREF	O	-	Current reference control	Analog Signal	
VREF	O	-	Voltage reference	Analog Signal	
EXTVREF	I	-	External VREF input	Analog Signal	
APVD<02:01>	I	-	Analog VDD	-	
APVS<02:01>	I	-	Analog VSS	-	

* Active-low signal

(*7) This signal depends on LCD Timing Register (H-sync Start/End, Mode).

(*8) This signal depends on LCD Timing Register (V-sync Start/End, Mode).

PCMCIA 1

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
C1DATL<07:00>	I/O	3.3/5V	PCMCIA lower data	Hi-Z	(*9)
C1DATH<07:00>	I/O	3.3/5V	PCMCIA upper data	Hi-Z	(*9)
C1ADR<25:00>	O	3.3/5V	PCMCIA address	Hi-Z	(*9)
C1RST	O	3.3/5V	PCMCIA reset	Hi-Z	(*9)
C1EN<02:01>*	O	3.3/5V	PCMCIA enable	Hi-Z	(*9)
C1IOR*	O	3.3/5V	PCMCIA I/O read	Hi-Z	(*9)
C1IOW*	O	3.3/5V	PCMCIA I/O write	Hi-Z	(*9)
C1OEN*	O	3.3/5V	PCMCIA output enable	Hi-Z	(*9)
C1WEN*	O	3.3/5V	PCMCIA write enable	Hi-Z	(*9)
C1REG*	O	3.3/5V	PCMCIA attribute select	Hi-Z	(*9)
C1BSY*	I	3.3/5V	PCMCIA busy	surge current protection mode	(*10)
C1BVD<02:01>	I	3.3/5V	PCMCIA battery voltage detect	surge current protection mode	(*10)
C1VS<02:01>	I	3.3V	PCMCIA voltage sense	I	
C1CD<02:01>*	I	3.3V	PCMCIA card detect	I	
C1WP	I	3.3/5V	PCMCIA write protect	surge current protection mode	(*10)
C1WAIT*	I	3.3/5V	PCMCIA wait	surge current protection mode	(*10)
C1VPPG	O	3.3V	Voltage select	L	(*11)
C1VPVC	O	3.3V	Voltage select	L	(*11)
C1VCC5*	O	3.3V	Voltage select	L	(*11)
C1VCC3*	O	3.3V	Voltage select	L	(*11)

* Active-low signal

(* 9) These signals are in a Hi-Z mode if D7 bit of PCMCIA Slot1 Power Control Register is 0.

(*10) These signals go into a surge current protection mode if any of the following conditions are satisfied.

–Slot Off

If the Slot On bit of PCMCIA Slot Control Register (Offset 100h) is 0.

–Buffer Off

If the Buffer Off bit of PCMCIA Buffer Off Register (Offset 104h) is 0.

–Output-Disable

If the Output Enable bit of PCMCIA Power Control Register (Offset 008h) is 0.

–Card Power Off

If the Card Power Enable bit of PCMCIA Power Control Register (Offset 008h) is 0.

–Power Off

If Vcc Control bits of PCMCIA Power Control Register (Offset 008h) are 00 or 11.

–No Card

If no PCMCIA Card is asserted.

–Card-Reset

If the Card Reset bit of PCMCIA Interrupt and General Control Register (Offset 00Ch) is 0.

–If PCLR* is asserted.

–RCLR*

If the Disable Resume Reset bit of PCMCIA Power Control Register (Offset 008h) is 0 and RCLR* is asserted.

(*11) Please refer the description of PCMCIA Power Control Register in PLUM2 manual.

PCMCIA 2

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
C2DATL<07:00>	I/O	3.3/5V	PCMCIA lower data	Hi-Z	(*9)
C2DATH<07:00>	I/O	3.3/5V	PCMCIA upper data	Hi-Z	(*9)
C2ADR<25:00>	O	3.3/5V	PCMCIA address	Hi-Z	(*9)
C2RST	O	3.3/5V	PCMCIA reset	Hi-Z	(*9)
C2EN<02:01>*	O	3.3/5V	PCMCIA enable	Hi-Z	(*9)
C2IOR*	O	3.3/5V	PCMCIA I/O read	Hi-Z	(*9)
C2IOW*	O	3.3/5V	PCMCIA I/O write	Hi-Z	(*9)
C2OEN*	O	3.3/5V	PCMCIA output enable	Hi-Z	(*9)
C2WEN*	O	3.3/5V	PCMCIA write enable	Hi-Z	(*9)
C2REG*	O	3.3/5V	PCMCIA attribute select	Hi-Z	(*9)
C2BSY*	I	3.3/5V	PCMCIA busy	surge current protection mode	(*10)
C2BVD<02:01>	I	3.3/5V	PCMCIA battery voltage detect	surge current protection mode	(*10)
C2VS<02:01>	I	3.3V	PCMCIA voltage sense	I	
C2CD<02:01>*	I	3.3V	PCMCIA card detect	I	
C2WP	I	3.3/5V	PCMCIA write protect	surge current protection mode	(*10)
C2WAIT*	I	3.3/5V	PCMCIA wait	surge current protection mode	(*10)
C2VPPG	O	3.3V	Voltage select	L	(*11)
C2VPVC	O	3.3V	Voltage select	L	(*11)
C2VCC5*	O	3.3V	Voltage select	L	(*11)
C2VCC3*	O	3.3V	Voltage select	L	(*11)

* Active-low signal

PCMCIA1/2 Common

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
CDSHDN*	O	3.3V	Shut down This signal outputs the inverted level of D0 bit in PCMCIA Card Power Register.	H	
CDAUD	O	3.3V	Audio This signal outputs the level of XOR value of speaker outputs of PCMCIA cards. (C1BVD<02> xor C2BVD<02>)	L	

* Active-low signal

SmartMedia Interface

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
SMDT<07:00>	I/O	3.3/5V	SmartMedia data	surge current protection mode	(*12)
SMCE*	O	3.3/5V	SmartMedia chip enable	Hi-Z	(*13)
SMWE*	O	3.3/5V	SmartMedia write enable	Hi-Z	(*13)
SMRE*	O	3.3/5V	SmartMedia read enable	Hi-Z	(*13)
SMCLE	O	3.3/5V	SmartMedia command latch enable	Hi-Z	(*13)
SMALE	O	3.3/5V	SmartMedia address latch enable	Hi-Z	(*13)
SMWP*	O	3.3/5V	SmartMedia write protect	Hi-Z	(*13)
SMWPIN*	I	3.3/5V	SmartMedia write protect from card	surge current protection mode	(*12)
SMRDY	I	3.3/5V	SmartMedia ready	surge current protection mode	(*12)
SMCD*	I	3.3/5V	SmartMedia card detect	surge current protection mode	(*12)
SMCIN*	I	3.3/5V	SmartMedia card insert	surge current protection mode	(*12)
SMVS	I	3.3/5V	SmartMedia voltage sense	surge current protection mode	(*12)
SMPWR1*	O	3.3V	SmartMedia power 1. This signal outputs the inverted level of SMPWR1 bit in SSFDC Power Control Register.	H	
SMPWR2*	O	3.3V	SmartMedia power 2. This signal outputs the inverted level of SMPWR2 bit in SSFDC Power Control Register.	H	
SMSTDN*	O	3.3V	SmartMedia shutdown. This signal outputs the inverted level of SMSTDN bit in SSFDC Power Control Register.	H	

* Active-low signal

(*12) These signals go into a surge current protection mode, if SMBOF1-0 of SSFDC Power Control Register are X0.

(*13) These signals are in a Hi-Z mode if SMBOF1-0 of SSFDC Power Control Register are X0 or 01.

USB Interface

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
USBD1P	I/O	-	USB port 1 data (+)	I	(*14)
USBD1M	I/O	-	USB port 1 data (-)	I	(*14)
USBOC1*	I	5V	Port 1 over current detection input	surge current protection mode	(*15)
USBD2P	I/O	-	USB port 2 data (+)	I	(*14)
USBD2M	I/O	-	USB port 2 data (-)	I	(*14)
USBOC2*	I	5V	Port 2 over current detection input	surge current protection mode	(*15)
USBPWR1*	O	3.3V	USB port 1 power control	L	(*16)
USBPWR2*	O	3.3V	USB port 2 power control	L	(*16)

* Active-low signal

(*14) These signals are in an input mode if USBEN bit of Power Control Register is 0.

(*15) These signals go into a surge current protection mode, if USBEN bit of Power Control Register is 0.

(*16) These signals output low level if USBEN bit of Power Control Register is 0.

5V 16/8-bit I/O Bus

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
IO5DAT<15:00>	I/O	5V	16 bit data bus for I/O devices	L	(*17)
IO5ADR<10:00>	O	5V	Address bus for I/O devices	L	(*17)
IO5CS<4:0>*	O	5V	I/O chip select	L	(*17)
IO5WR*	O	5V	I/O write enable	L	(*17)
IO5RD*	O	5V	I/O read enable	L	(*17)
IO5BHE*	O	5V	I/O bus high enable	L	(*17)
IO5WAIT*	I	5V	I/O wait	surge current protection mode	(*18)

* Active-low signal

(*17) These signals output low level if IO5OE bit of Power Control Register is 0.

(*18) This signal goes into a surge current protection mode, if IO5OE bit of Power Control Register is 0.

Interrupt

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
INTO	O	3.3V	Interrupt output to TX3922	L	
IO5INT<03:00>	I	5V	Interrupt input for 16/8 bit I/O devices (5V input)	surge current protection mode	(*19)
IO3INT<01:00>	I	3.3V	Auxiliary interrupt (3V input)	I	

* Active-low signal

(*19) These signals go into a surge current protection mode, if IO5OE bit of Power Control Register is 0.

Power Management

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
IO5PWR	O	3.3V	Power supply control of 16/8 bit IO bus This signal outputs the level of IO5PWR bit in Power Control Register.	L	
PWRCNT<02:00>	O	3.3V	Power control signals These signals output the levels of EXTPW2-0 bits in Power Control Register.	L	
IO5CLRH	O	5V	Clear signals for 16/8 bit I/O devices (Active High) This signal outputs the inverted level of IO5CL1 bit in Reset Control Register.	L	(*20)
IO5CLRL*	O	5V	Clear signals for 16/8 bit I/O devices (Active Low) This signal outputs the level of IO5CL0 bit in Reset Control Register.	L	(*20)

* Active-low signal

(*20) These signals output low level if IO5OE bit of Power Control Register is 0.

Clear and Clock

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
PCLR*	I	3.3V	Power on clear	I	
RCLR*	I	3.3V	ROM I/F signal disable signal	I	
CLKRTC	I	3.3V	32kHz real time clock input	I	
CLKBUS	I	3.3V	System clock input	I	
CLKMEM	I	3.3V	VRAM clock input	I	
CLKUSB	I	3.3V	USB 48MHz clock input	I	
CLKVIDEO	I	3.3V	PLL input for video clock This signal should be connected to the external video clock generator (14.31818MHz), or to GND if another signal is used for video clock.	I	
APLLVDD	I		VDD for analog PLL	-	
APLLVSS <02:01>	I		VSS for analog PLL	-	
APLLRO	I		VCO center frequency set resistor connection	I	
APLLLP	I		Loop filter capacitor connection	I	
APLLAGS	I		Analog sense pin for connection of external components	I	

* Active-low signal

Test

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
TEST<01:00>	I	3.3V	Test pin These signals should be connected to VSS.	I	

* Active-low signal

Debug Board Interface

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
DBGCS*	O	3.3V	Debug board chip select	H	
DBGWAIT	I	3.3V	Debug wait control	I	

* Active-low signal

JTAG

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
JTDI	I	3.3V	JTAG data in Data is serially scanned in through this pin.	I	
JTDO	O	3.3V	JTAG data out Data is serially scanned out through this pin.	Hi-Z	
JTMS	I	3.3V	JTAG command signal	I	
JTCK	I	3.3V	JTAG clock	I	

* Active-low signal

Power Supply

NAME	I/O	LEVEL	DESCRIPTION	State on PCLR*	Notes
UVCC1	-	3.3/5V	VCC for PCMCIA slot1 I/O buffer	-	
UVCC2	-	3.3/5V	VCC for PCMCIA slot2 I/O buffer	-	
UVCC3	-	3.3/5V	VCC for SmartMedia I/O buffer	-	
VDDS	-	5V	Power supply (5V)	-	
VDD	-	3.3V	Power supply (3.3V)	-	
GND	-	GND	Signal ground	-	
NC	-	-	Not Connected	-	

* Active-low signal

5. Functional Block Descriptions

5.1. LCD/CRT Controller

- The PLUM2 has LCD controller and CRT controller. These controllers support two types of the display resolution (640x480 dot and 800x600 dot) and three color modes (256 color, 64k color and 64 grayscale).
- LCD controller supports three types of LCD panel (STN, DSTM and TFT).
- These controllers support two kinds of simultaneous display function. One is mirror output function with which these controllers display a same image on LCD and CRT screens. The other is ghost output function with which these controllers display different images on LCD and CRT screens.

5.2. PCMCIA Controller

- Compatible with the PCMCIA V2.1/JEIDA V4.2 specification (does not support Card-Bus and ZV-Port).
- Register specifications similar to those of Intel i82365SL (ExCA: Exchangeable Card Architecture).
- Supports up to two slots.
- Equipped with five Memory/Attribute windows and two I/O windows in each slot.
- Can use 3.3 V/5 V cards.
- Each Memory/Attribute window can access a memory space of up to 64MB.
- Each I/O window can access an I/O area of up to 64KB.
- Memory mapped I/O (register set accessible in the same fashion as I/O memory access).
- Controls external PCMCIA card power controller (TI TPS2205).

5.3. SmartMedia Controller

- Support up to one identical full SmartMedia port.
- Appropriate connector keying and level-shifting buffers required for 3.3V versus 5V SmartMedia interface implementations.
- 3.3V/5V SmartMedia can be used.

5.4. I/O Bus Interface

- It is an ISA like interface for 5V power supply I/O device.
- The bus width is 8 or 16-bit.
- For example keyboard controller, IDE device, Super I/O, and Ethernet controller can be connected.

5.5. USB Host Controller

- Support up to two USB slots.
- Conform to the OHCI specification.

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

V_{SS} = 0 V (GND)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD} V_{DDS}	V_{SS}-0.3 to +5.0 V_{SS}-0.3 to +7.0	V
	UVCC1 UVCC2 UVCC3	V_{SS}-0.3 to +7.0	V
Input voltage	V_{IN} V_{INS} V_{INU1} V_{INU2} V_{INU3}	V_{SS}-0.3 to V_{DD}+ 0.3 V_{SS}-0.3 to V_{DDS}+ 0.3 V_{SS}-0.3 to UVCC1+ 0.3 V_{SS}-0.3 to UVCC2+ 0.3 V_{SS}-0.3 to UVCC3+ 0.3	V
Input current	I_{IN}	±10	mA
Storage temperature	T_{STG}	- 40 to +125	°C

Note :

The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

6.2. Recommended Operating Conditions

V_{SS} = 0 V (GND)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power Supply voltage	V_{DD}		3.0	3.3	3.6	V
	V_{DDS}		4.75	5.0	5.25	V
	UCC1 UCC2 UCC3	3.3V mode 5V mode	3.0 4.75	3.3 5.0	3.6 5.25	V
Operating temperature	T_{OPR}		0	–	70	°C

Note:

The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified.

If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur.

Thus, when designing a product that includes this device, ensure that the recommended operating conditions for the device are always adhered to.

6.3. DC Characteristics

(T_a = 0°C to 70°C, VDD = 3.3V ± 0.3V, VDDS = 5.0V ± 0.25V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating current (w/CRT)	I_{DD1}	CLKBUS = 74MHz CLKMEM = 74MHz CLKRTC = 32KHz CLKUSB = 48MHz LCD 640×480×8bit frame rate 88Hz CRT 640×480×8bit frame rate 75Hz	–	200	–	mA
Operating current	I_{DD2}	CLKBUS = 74MHz CLKMEM = 74MHz CLKRTC = 32KHz CLKUSB = 48MHz LCD 640×480×8bit frame rate 88Hz	–	90	–	mA
Idle current (w/CRT)	I_{IDL1}	LCD ON CLKBUS = 4.625MHz CLKMEM = 74MHz LCD 640×480×8bit frame rate 88Hz CRT 640×480×8bit frame rate 75Hz	–	160	–	mA
Idle current	I_{IDL2}	LCD ON CLKBUS = 4.625MHz CLKMEM = 37MHz LCD 640×480×8bit frame rate 88Hz	–	70	–	mA
Static current	I_{DDS}	V_{DDS}, UVCC1/2/3 = 5.25V V_{DD} = 3.6V	–	20	100	µA
Input voltage (1) 3V CMOS	V_{IH1}	V_{DD} = 3.6V	V_{DD} × 0.8	–	V_{DD} + 0.3	V
		UVCC1/2/3 = 3.6V	UVCCn × 0.8	–	UVCCn + 0.3	V
	V_{IL1}	V_{DD} = 3.0V	-0.3	–	V_{DD} × 0.2	V
		UVCC1/2/3 = 3.0V	-0.3	–	UVCCn × 0.2	V
Input voltage (2) 5V CMOS	V_{IH2}	V_{DDS} = 5.25V	3.5	–	V_{DDS} + 0.3	V
		UVCC1/2/3 = 5.25V	3.5	–	UVCCn + 0.3	V
	V_{IL2}	V_{DDS} = 4.75V UVCC1/2/3 = 4.75V	-0.3	–	1.5	V
Input voltage (3) 3V CMOS SCHMITT	V_{IH3}	V_{DD} = 3.6V	V_{DD} × 0.8	–	V_{DD} + 0.3	V
		UVCC1/2/3 = 3.6V	UVCCn × 0.8	–	UVCCn + 0.3	V
	V_{IL3}	V_{DD} = 3.0V	-0.3	–	V_{DD} × 0.2	V
		UVCC1/2/3 = 3.0V	-0.3	–	UVCCn × 0.2	V
Input voltage (4) 5V TTL	V_{IH4}	V_{DDS} = 5.25V	2.0	–	V_{DDS}+ 0.3	V
	V_{IL4}	V_{DDS} = 4.75V	-0.3	–	0.8	V
Schmitt width	V_{TH}		–	0.4	–	V
Input current	I_{IH} I_{IL}	V_{IN}= V_{DD}, V_{DDS}, UVCC1/2/3	-10	–	10	µA
Input current (Pull-up resister)	I_{IHU}	V_{IN} = V_{DD}	10	–	200	µA

Output voltage (5)	V_{OH1}	I_{OH} = -4mA	2.4	–	–	V
	V_{OL1}	I_{OL} = 4mA	–	–	0.4	V
Output voltage (6)	V_{OH2}	I_{OH} = -8mA	2.4	–	–	V
	V_{OL2}	I_{OL} = 8mA	–	–	0.4	V

(1) V_{IH1}, V_{IL1}: C1BVD1, C1BVD2, C1WP, C2BVD1, C2BVD2, C2WP, DBGWAIT, MROMA13, MROMA14, MROMA15, RMADR[12:00], RMDAT[31:00], VRDAT[31:00], RMALE, SMRDY, SMVS, JTCK, JTDI, TEST0, TEST1, JTMS, C1BSY, C1WAIT, C2BSY, C2WAIT, RMCASO, RMCAS1, RMCAS2, RMCAS3, RMCS00, RMCS03, RMMCS0, RMMCS1, RMRD, RMWT, SMCD, SMCIN, SMWPIN, (C1DATH[07:00], C1DATL[07:00], C2DATH[07:00], C2DATL[07:00], SMDT[07:00])

(2) V_{IH2}, V_{IL2}: IO5INT[03:00], IO5WAIT, USBOC2, USBOC1, (C1DATH[07:00], C1DATL[07:00], C2DATH[07:00], C2DATL[07:00], SMDT[07:00])

(3) V_{IH3}, V_{IL3}: C1VS1, C1VS2, C2VS1, C2VS2, CLKBUS, CLKMEM, CLKRTC, CLKUSB, CLKVIDEO, IO3INT0, IO3INT1, C1CD1, C1CD2, C2CD1, C2CD2, PCLR, RCLR

(4) V_{IH4}, V_{IL4}: IO5DAT[15:00]

(5) V_{OH1}, V_{OL1}: BKLOFF, C1ADR[25:00], C1DATH[07:00], C1DATL[07:00], C1RST, C1VPPG, C1VPVC, C2ADR[25:00], C2DATH[07:00], C2DATL[O7:00], C2RST, C2VPPG, C2VPVC, CDAUD, HSYNC, INTO, IO5ADR[10:03], IO5CLRH, IO5PWR, LCDCLK, LCDDEN, LCDDSP, LCDFP, LCDGD[17:00], LCDLP, LCDLUMO, LCDLUM1, LCDOFF, MROMA[22:13], PWRCNT[02:00], RMDAT[31:00], SMALE, SMCLE, SMDT[07:00], JTDO, VRADR[10:00], VRCKE, VRCLK, VRDAT[31:00], VRDQM[03:00], VSYNC, C1EN1, C1EN2, C1IOR, C1IOW, C1OEN, C1REG, C1VCC3, C1VCC5, CIWEN, C2EN1, C2EN2, C2IOR, C2IOW, C2OEN, C2REG, C2VCC3, C2VCC5, C2WEN, CDSTDN, DBGCS, IO5BHE, IO5CLRL, IO5CS0, IO5CS1, IO5CS2, MRCS[07:00], MROMOE, RMMWA, SMCE, SMPWR1, SMPWR2, SMRE, SMSTDN, SMWE, SMWP, USBPWR1, USBPWR2, VRCAS, VRCSO, VRCS1, VRRAS, VRWE

(6) V_{OH2}, V_{OL2}: IO5ADR[02:00], IO5DAT0[15:00], IO5CS3, IO5CS4, IO5RD, IO5WR

7. AC Characteristics

The following operating conditions apply to all values specified in this section unless otherwise specified.

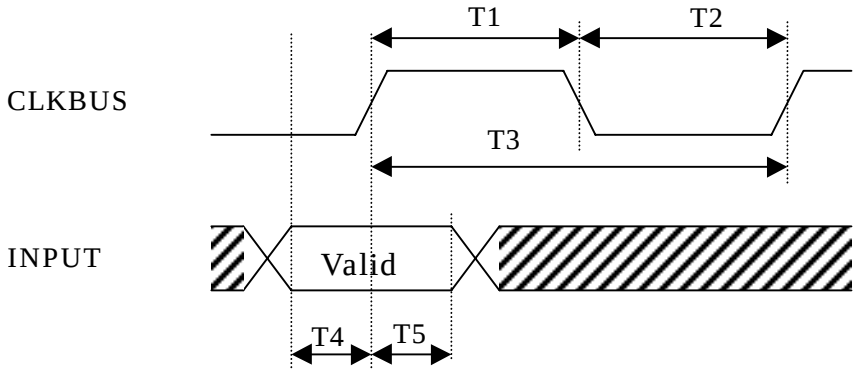
Ta = 0 to 70 C.

V_{DD} = 3.0 to 3.6 V

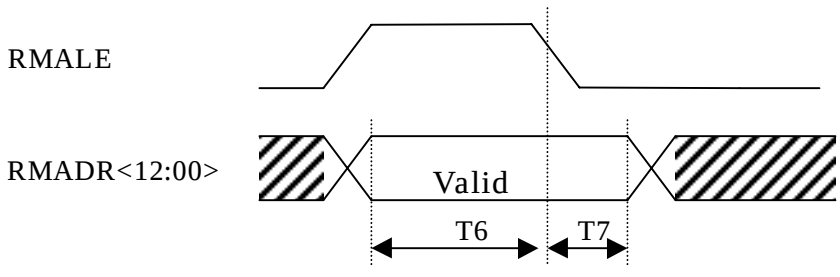
V_{DDS} = 4.75 to 5.25 V

External Capacitance Load (CL) = 40pF

7.1. TX3922 System Bus Interface

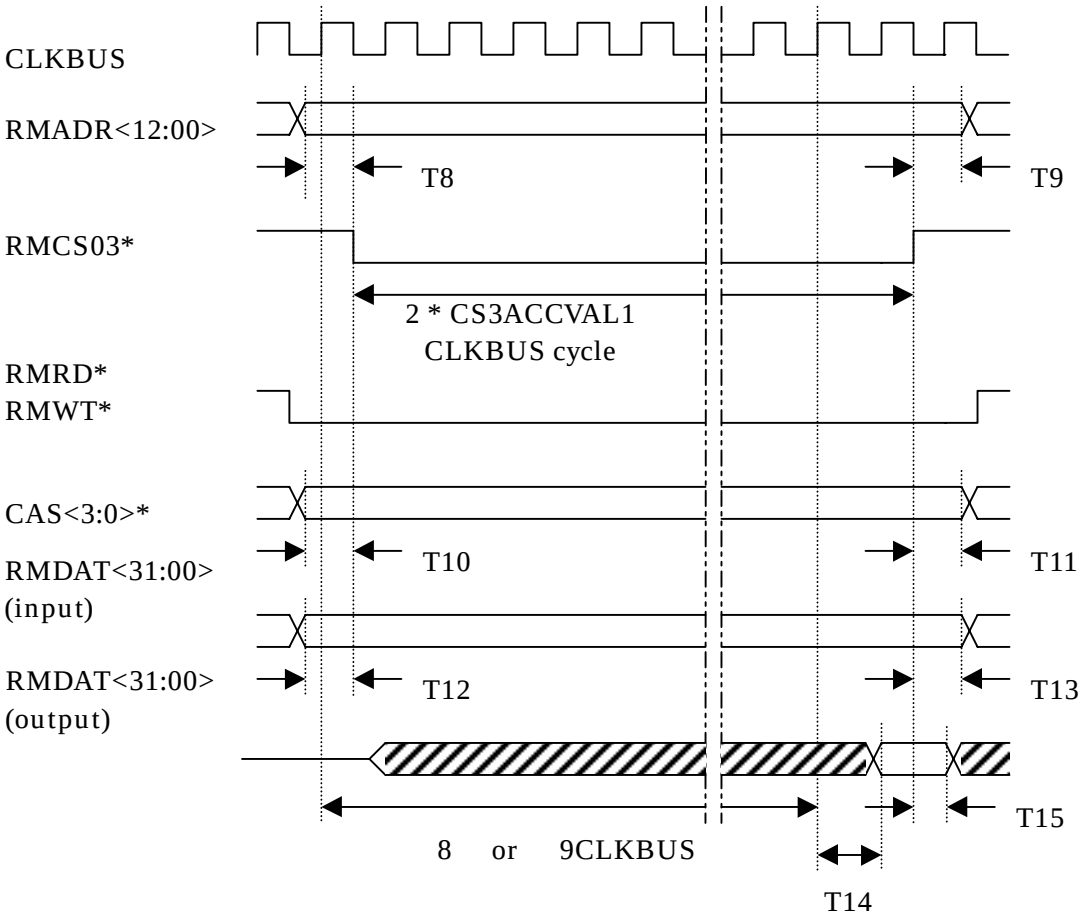


Item	Parameter	MIN	MAX	Unit	Notes
T1	CLKBUS high time	4.8	-	ns	
T2	CLKBUS low time	4.8	-	ns	
T3	CLKBUS period	12	-	ns	
T4	RMCS00* to CLKBUS Setup time	-	-	ns	
T5	RMCS00* to CLKBUS Hold time	-	-	ns	
T4	RMCS03* to CLKBUS Setup time	2	-	ns	
T5	RMCS03* to CLKBUS Hold time	0	-	ns	
T4	RMMCS0* to CLKBUS Setup time	2	-	ns	
T5	RMMCS0* to CLKBUS Hold time	0	-	ns	
T4	RMMCS1* to CLKBUS Setup time	2	-	ns	
T5	RMMCS1* to CLKBUS Hold time	0	-	ns	



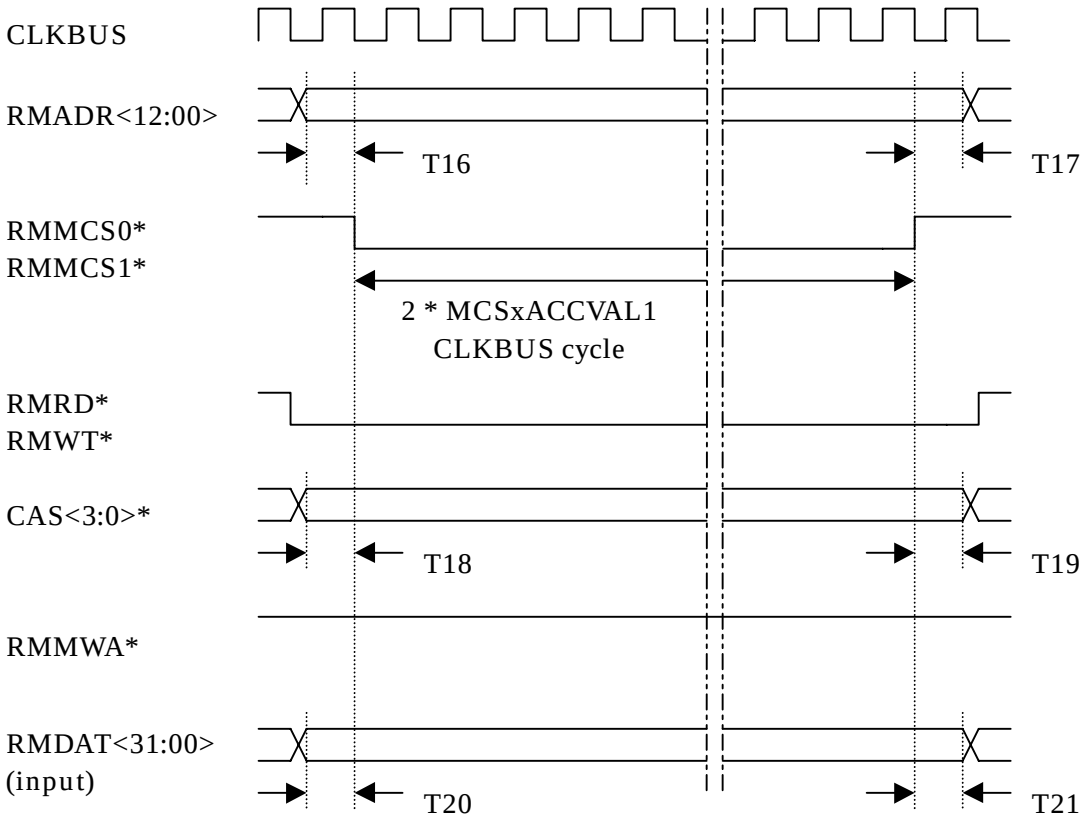
Item	Parameter	MIN	MAX	Unit	Note
T6	RMADR<12:00> to RMALE Setup time	10	-	ns	
T7	RMADR<12:00> to RMALE Hold time	5	-	ns	

Access timing for RMCS03* area



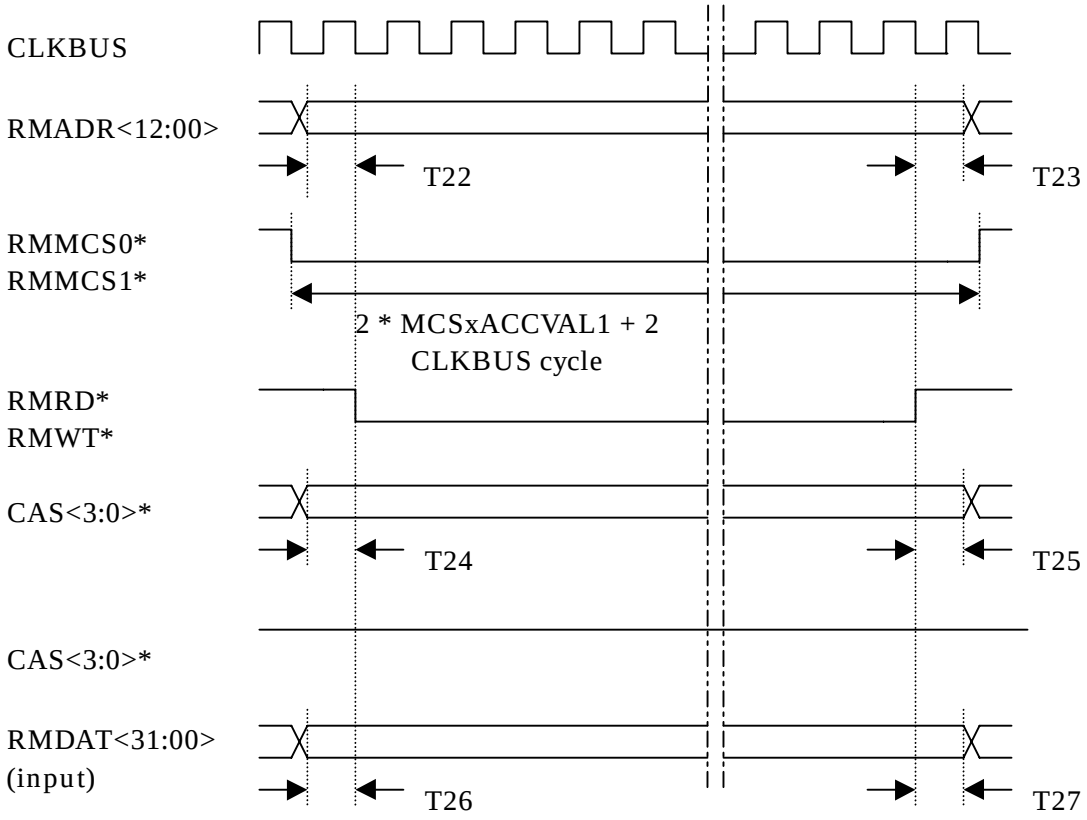
Item	Parameter	MIN	MAX	Unit	Note
T8	RMADR<12:00> to RMCS03* Setup time	0	-	ns	
T9	RMADR<12:00> to RMCS03* Hold time	0	-	ns	
T10	CAS<3:0>* to RMCS03* Setup time	0	-	ns	
T11	CAS<3:0>* to RMCS03* Hold time	0	-	ns	
T12	RMDAT<31:00> to RMCS03* Setup time	0	-	ns	
T13	RMDAT<31:00> to RMCS03* Hold time	0	-	ns	
T14	Delay CLKBUS to RMDAT<31:00>	-	20	ns	
T15	RMDAT<31:00> to RMCS03* Hold time	12	-	ns	

Access timing for RMMCSx* area (ENMCSxACC bit = 1)



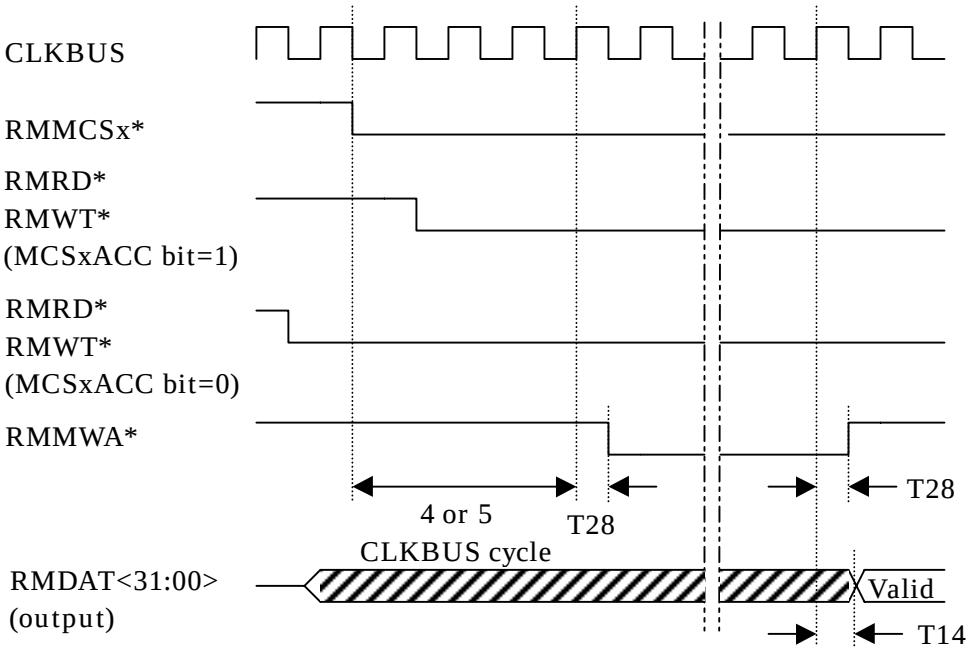
Item	Parameter	MIN	MAX	Unit	Note
T16	RMADR<12:00> to RMMCS<1:0>* Setup time	0	-	ns	
T17	RMADR<12:00> to RMMCS<1:0>* Hold time	0	-	ns	
T18	CAS<3:0>* to RMMCS<1:0>* Setup time	0	-	ns	
T19	CAS<3:0>* to RMMCS<1:0>* Hold time	0	-	ns	
T20	RMDAT<31:00> to RMMCS<1:0>* Setup time	0	-	ns	
T21	RMDAT<31:00> to RMMCS<1:0>* Hold time	0	-	ns	

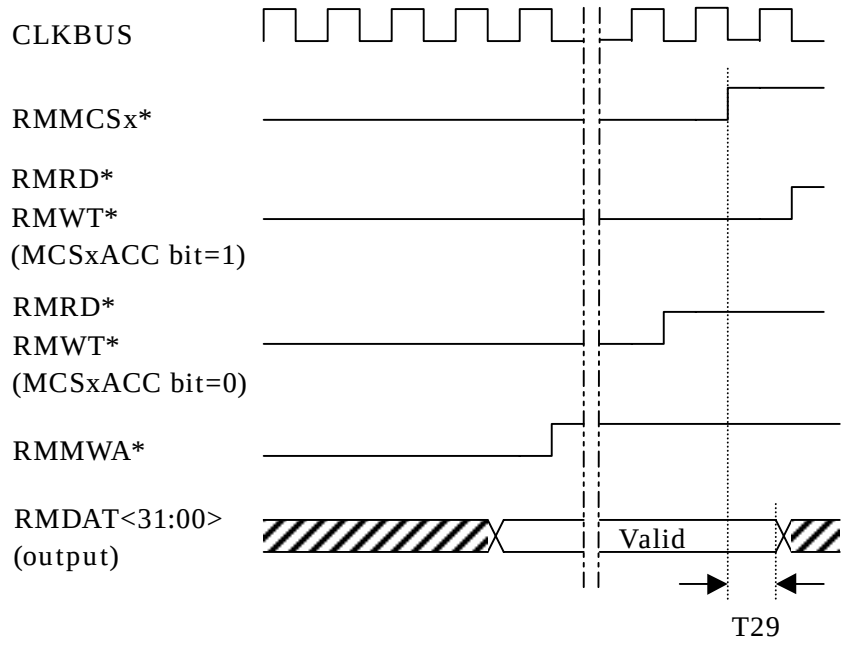
Access timing for RMMCSx* area (ENMCSxACC bit = 0)



Item	Parameter	MIN	MAX	Unit	Note
T22	RMADR<12:00> to RMRD* or RMWT* Setup time	0	-	ns	
T23	RMADR<12:00> to RMRD* or RMWT* Hold time	0	-	ns	
T24	CAS<3:0>* to RMRD* or RMWT* Setup time	0	-	ns	
T25	CAS<3:0>* to RMRD* or RMWT* Hold time	0	-	ns	
T26	RMDAT<31:00> to RMRD* or RMWT* Setup time	0	-	ns	
T27	RMDAT<31:00> to RMRD* or RMWT* Hold time	0	-	ns	

Access timing for RMMCSx area when RMMWA is asserted.



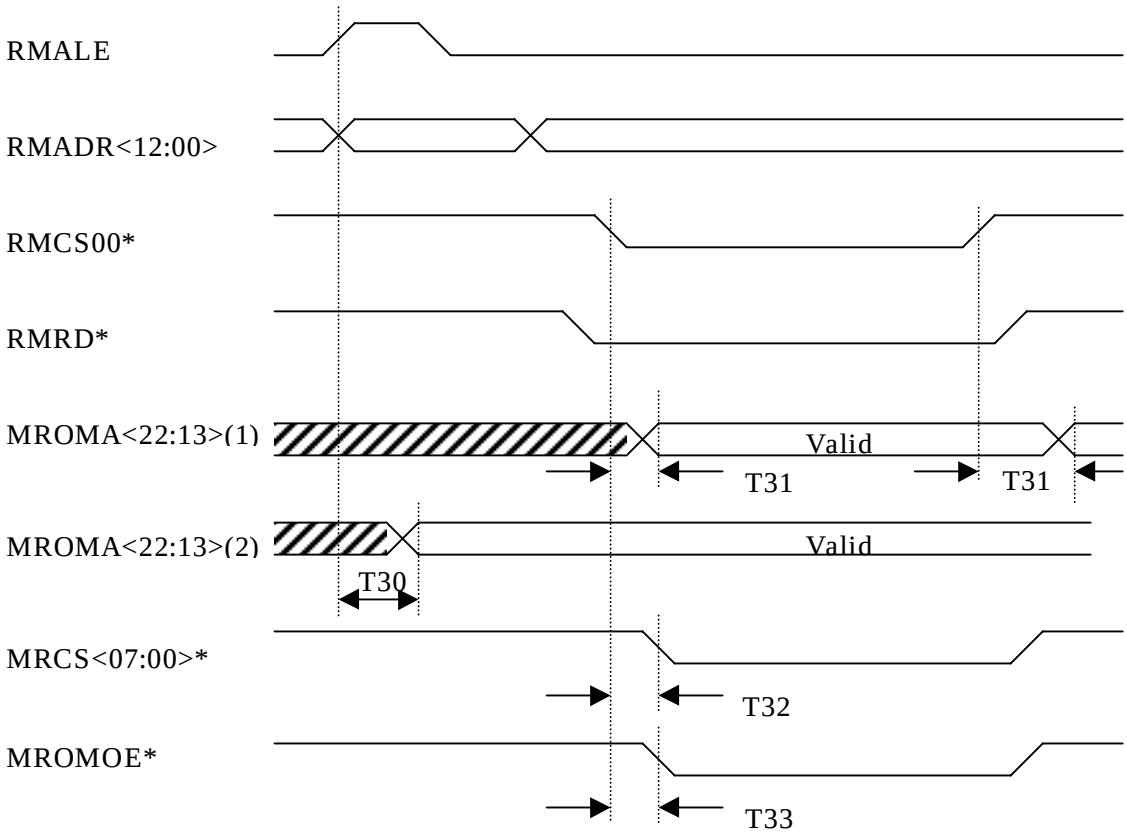


Item	Parameter	MIN	MAX	Unit	Note
T14	Delay CLKBUS to RMDAT<31:00>	-	20	ns	
T28	Delay CLKBUS to RMMWA*	-	15	ns	1
T29	RMDAT<31:00> to RMMCSx* Hold time	12	-	ns	1

Note:

1.This timing use a capacitive load (CL) to ground of 15pF.

7.2. ROM Interface



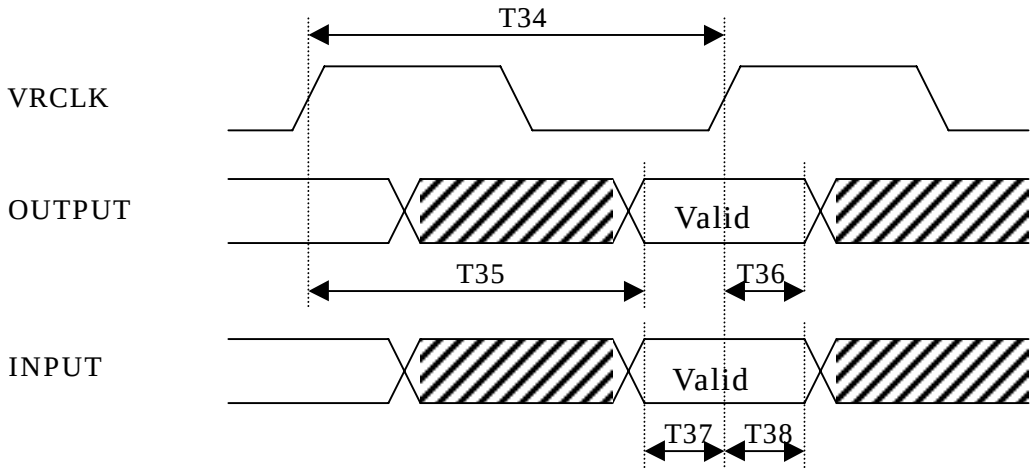
Item	Parameter	MIN	MAX	Unit	Note
T30	Delay RMALE to MROMA<22:13>	-	20	ns	2
T31	Delay RMCS00* to MROMA<22:13>	-	20	ns	3
T32	Delay RMCS00* to MRCS<07:00>*	-	20	ns	
T33	Delay RMCS00* to MROMOE*	-	20	ns	

Note:

2.MROMA<12:00> (1) is applied if MRMAEN bit of Mask ROM Control Register is 0. (Default)

3.MROMA<12:00> (2) is applied if MRMAEN bit of Mask ROM Control Register is 1.

7.3. Video RAM Interface



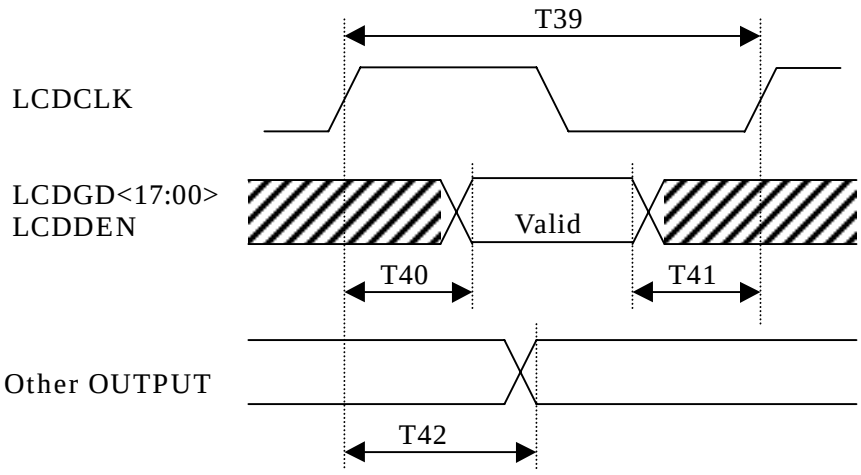
Item	Parameter	MIN	MAX	Unit	Note
T34	VRCLK period	12	-	ns	4
T37	VRDAT<31:00> to VRCLK Setup time	4.9	-	ns	4
T38	VRDAT<31:00> to VRCLK Hold time	0	-	ns	4
T35	Delay VRCLK to VRDAT<31:00>	-	8.7	ns	4
T36	VRDAT<31:00> to VRCLK Hold time	0.9	-	ns	4
T35	Delay VRCLK to other output signals	-	8.1	ns	4,5
T36	Other output signals to VRCLK Hold time	1.2	-	ns	4,5

Note:

4.This timing use a capacitive load (CL) to ground of 15pF.

5.Other output signals are VRADR<10:00>, VRRAS*, VRCAS*, VRWE*, VRCS<01:00>*, VRDQM<03:00> and VRCKE.

7.4. LCD Interface



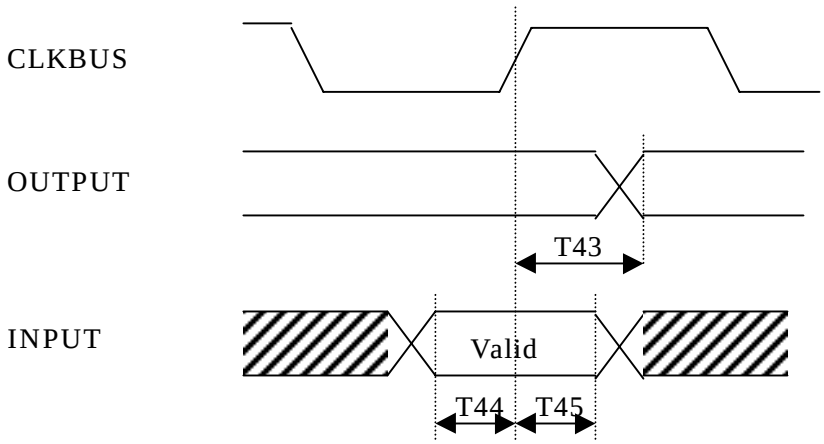
Item	Parameter	MIN	MAX	Unit	Note
T39	LCDCLK period	17	-	ns	
T40	Delay LCDCLK to LCDGD<17:00>	-	7	ns	6
T41	LCDGD<17:00> to LCDCLK time	-	4	ns	6
T40	Delay LCDCLK to LCDDEN	-	7	ns	6
T41	LCDDEN to LCDCLK time	-	4	ns	6
T42	Delay LCDCLK to LCDLP	0	12	ns	
T42	Delay LCDCLK to LCDFP	0	12	ns	

Notes:

6.DGD<31:00> and LCDEN signals are valid at the falling edge of LCDCLK.

7.DDSP, LCDOFF, BKLOFF, LCDLEV<4:0> and LCDLUM<1:0> are asynchronous to the LCDCLK.

7.5. PCMCIA1,PCMCIA2 and PCMCIA 1/2 Common Interface



PCMCIA1 Interface

Item	Parameter	MIN	MAX	Unit	Note
43	Delay CLKBUS to C1DATL<07:00>	6	26	ns	8
43	Delay CLKBUS to C1DATH<07:00>	6	26	ns	8
43	Delay CLKBUS to C1ADR<25:00>	6	32	ns	8
43	Delay CLKBUS to C1RST	6	32	ns	8
43	Delay CLKBUS to C1EN<02:01>*	6	32	ns	8
43	Delay CLKBUS to C1OR*	5	20	ns	8
43	Delay CLKBUS to C1OW*	5	20	ns	8
43	Delay CLKBUS to C1OEN*	5	20	ns	8
43	Delay CLKBUS to C1WEN*	5	20	ns	8
43	Delay CLKBUS to C1REG*	6	32	ns	8
43	Delay CLKBUS to C1VPPG	10	35	ns	8
43	Delay CLKBUS to C1VPVC	4	20	ns	8
43	Delay CLKBUS to C1VCC5*	4	20	ns	8
43	Delay CLKBUS to C1VCC3*	10	35	ns	8
44	C1DATL<07:00> to CLKBUS Setup time	10	-	ns	
45	C1DATL<07:00> to CLKBUS Hold time	0	-	ns	
44	C1DATH<07:00> to CLKBUS Setup time	10	-	ns	
45	C1DATH<07:00> to CLKBUS Hold time	0	-	ns	
44	Other input signals to CLKBUS Setup time	6	-	ns	9
45	Other input signals to CLKBUS Hold time	0	-	ns	9

Notes:

8. This timing use a capacitive load (CL) to ground of 50pF.
9. Other input signals are C1BSY*, C1BVD<02:01>, C1VS<02:01>*, C1CD<02:01>*, C1WP and C1WAIT*.

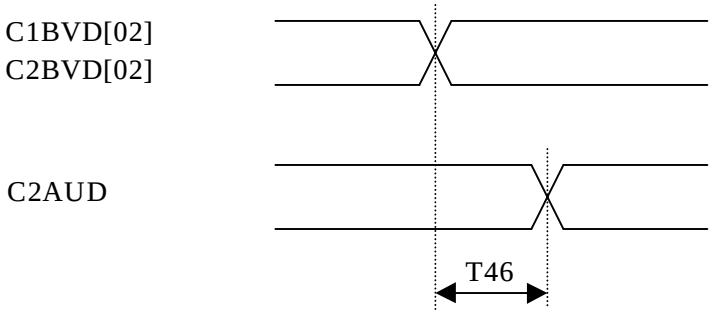
PCMCIA2 Interface

Item	Parameter	MIN	MAX	Unit	Note
43	Delay CLKBUS to C2DATL<07:00>	6	26	ns	10
43	Delay CLKBUS to C2DATH<07:00>	6	26	ns	10
43	Delay CLKBUS to C2ADR<25:00>	6	32	ns	10
43	Delay CLKBUS to C2RST	6	32	ns	10
43	Delay CLKBUS to C2EN<02:01>*	6	32	ns	10
43	Delay CLKBUS to C2OR*	5	20	ns	10
43	Delay CLKBUS to C2OW*	5	20	ns	10
43	Delay CLKBUS to C2OEN*	5	20	ns	10
43	Delay CLKBUS to C2WEN*	5	20	ns	10
43	Delay CLKBUS to C2REG*	6	32	ns	10
43	Delay CLKBUS to C2VPPG	10	35	ns	10
43	Delay CLKBUS to C2VPVC	4	20	ns	10
43	Delay CLKBUS to C2VCC5*	4	20	ns	10
43	Delay CLKBUS to C2VCC3*	10	35	ns	10
44	C2DATL<07:00> to CLKBUS Setup time	10	-	ns	
45	C2DATL<07:00> to CLKBUS Hold time	0	-	ns	
44	C2DATH<07:00> to CLKBUS Setup time	10	-	ns	
45	C2DATH<07:00> to CLKBUS Hold time	0	-	ns	
44	Other input signals to CLKBUS Setup time	6	-	ns	11
45	Other input signals to CLKBUS Hold time	0	-	ns	11

Notes:

10. This timing use a capacitive load (CL) to ground of 50pF.
11. Other input signals are C2BSY*, C2BVD<02:01>, C2VS<02:01>*, C2CD<02:01>*, C2WP and C2WAIT*.

PCMCIA 1/2 Common

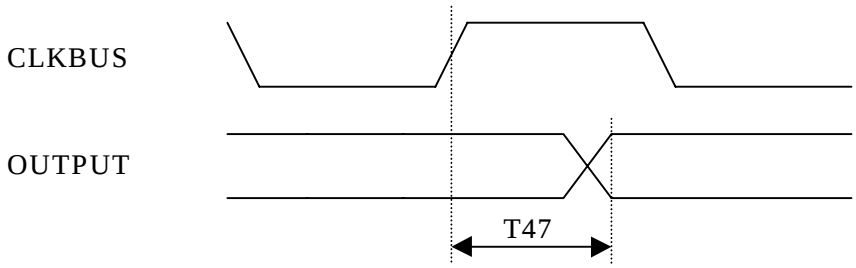


Item	Parameter	MIN	MAX	Unit	Note
43	Delay CLKBUS to C2CFSD*	12	31	ns	
46	Delay C1BVD[02] or C2BVD[02] to C2AUD	4	15	ns	12

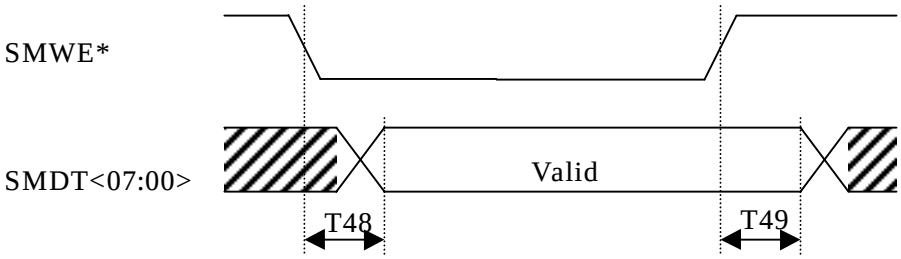
Note:

12.C2AUD signal is valid if I/O card is inserted.

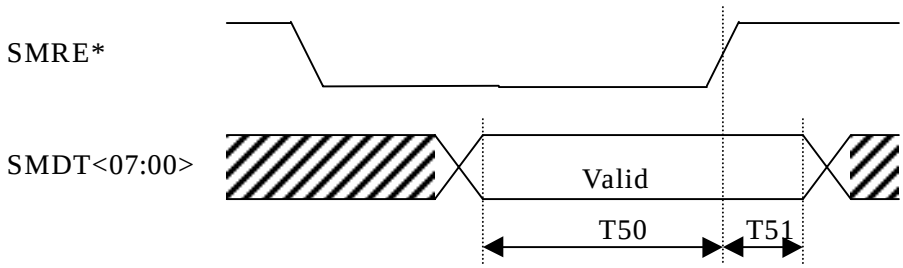
7.6. SmartMedia Interface



Item	Parameter	MIN	MAX	Unit	Note
T47	Delay CLKBUS to SMCE*	-	20	ns	
T47	Delay CLKBUS to SMWE*	-	20	ns	
T47	Delay CLKBUS to SMRE*	-	20	ns	
T47	Delay CLKBUS to SMCLE	-	20	ns	
T47	Delay CLKBUS to SMALE	-	20	ns	
T47	Delay CLKBUS to SMWP*	-	20	ns	
T47	Delay CLKBUS to SMPWR1	-	20	ns	
T47	Delay CLKBUS to SMPWR2	-	20	ns	
T47	Delay CLKBUS to SMSHDN*	-	20	ns	



Item	Parameter	MIN	MAX	Unit	Note
T48	Delay falling edge of SMWE* to SMDT<07:00>	-	5	ns	
T49	SMDT<07:00> to SMWE* Hold time	24	-	ns	



Item	Parameter	MIN	MAX	Unit	Note
T50	SMDT<07:00> to SMRE* Setup time	10	-	ns	
T51	SMDT<07:00> to SMRE* Hold time	0	-	ns	

Note:

13.There is not any AC timing requirement on SMWPIN*, SMRDY, SMCD*, SMCIN* and SMVS.

7.7. USB Interface

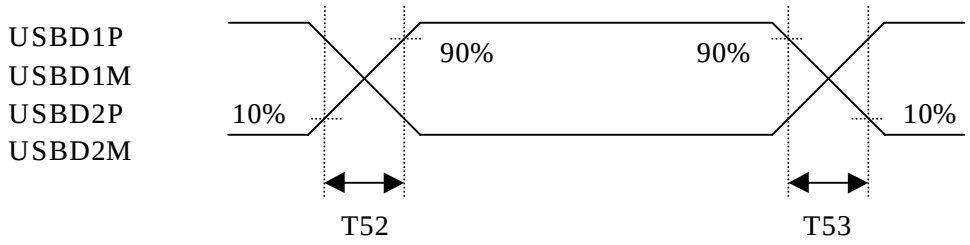


Table 1 Full-Speed Source USB Electrical Characteristics

Parameter	Symbol	Conditions[1,2,3]	Min	Max	Unit
Driver Characteristics:					
Transition Time[4,5]:					
Rise Time	T52	CL = 50pF	4	20	ns
Fall Time	T53	CL = 50pF	4	20	ns
Rise/Fall Time Matching	t_{RFM}	(T52/T53)	90	110	%
Data Source Timings:					
Full-speed Data Rate	T_{DRATE}	Average Bit Rate (12 Mbits/s +/- 0.25%)	11.97	12.03	Mbits/s
Frame Interval	T_{FRAME}	1.0 ms +/- 0.05%	0.9995	1.0005	ms

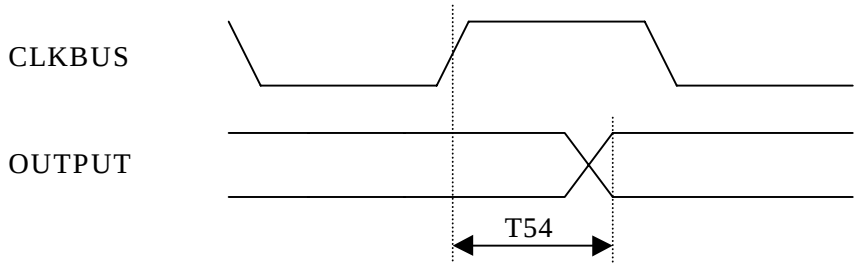
Table 2 Low-Speed Source USB Electrical Characteristics

Parameter	Symbol	Conditions[1,2]	Min	Max	Unit
Driver Characteristics:					
Transition Time[3,4,5]:					
Rise Time	T52	CL = 50 pF	75	–	ns
		CL = 350 pF	–	300	ns
Fall Time	T53	CL = 50 pF	75	–	ns
		CL = 350 pF	–	300	ns
Rise/Fall Time Matching	T_{RFM}	(T52/T53)	80	120	%
Data Source Timings:					
Low-speed Data Rate	T_{DRATE}	Average Bit Rate (1.5 Mbits/s +/- 1.5%)	1.4775	1.5225	Mbits/s

Note:

14. All voltages measured from the local ground potential, unless otherwise specified.
15. All timings use a capacitive load (CL) to ground of 50 pF, unless otherwise specified.
16. Full-speed timings have a 1.5KOhm pull-up to 2.8 V on the D+ data line.
17. Low-speed timings have a 1.5KOhm pull-up to 2.8 V on the D– data line.
18. Measured from 10% to 90% of the data signal.
19. The rising and falling edges should be smoothly transitioning (monotonic).
20. There is not other AC timing requirement on USBD1P, USBD1M, USBOC1*, USBD2P, USBD2M, USBOC2*, USBPWR1* and USBPWR2*.

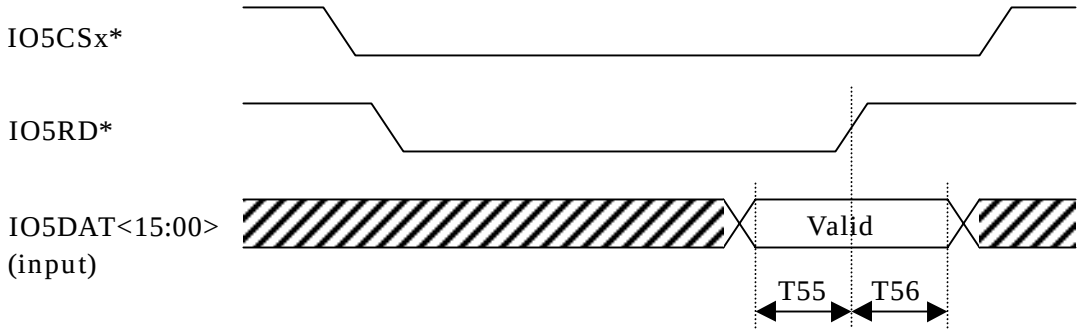
7.8. 5V 16/8-bit I/O Interface



Item	Parameter	MIN	MAX	Unit	Note
T54	Delay CLKBUS to all output signals	7	24	ns	21,22

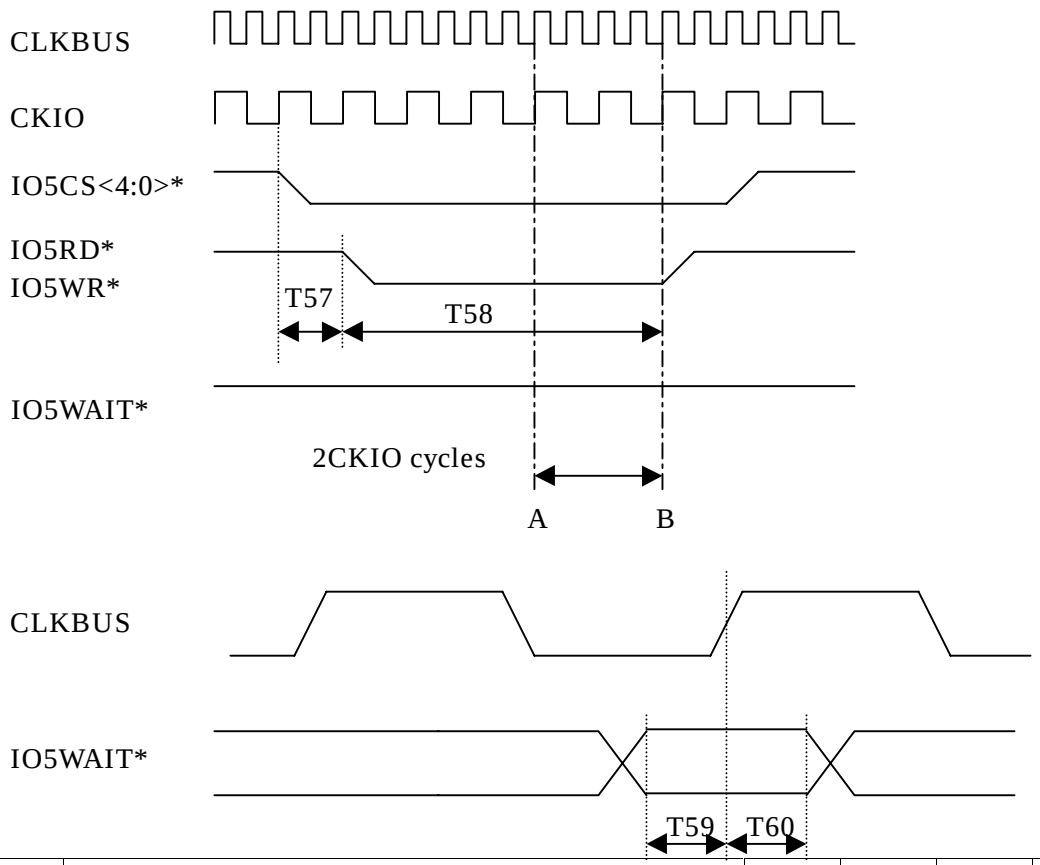
Note:

21. This timing use a capacitive load (CL) to ground of 50pF.
22. All output signals are IO5DAT<15:00>, IO5ADR<10:00>, IO5CS<4:0>*, IO5WR*, IO5RD* and IO5BEH*.



Item	Parameter	MIN	MAX	Unit	Note
T55	IO5DAT<15:00> to IO5RD* Setup time	18	-	ns	
T56	IO5DAT<15:00> to IO5RD* Hold time	0	-	ns	

I/O access timing when IO5WAIT* is not asserted.



Item	Parameter	MIN	MAX	Unit	Note
T59	IO5WAIT* to CLKBUS Setup time	3	-	ns	
T60	IO5WAIT* to CLKBUS Hold time	0	-	ns	

Note:

23.All output signal change at the rising edge of the CLKBUS.

24.An internal signal CKIO is a half-frequency clock derived from CLKBUS by frequency divider.

25.T57 is defined by I/O Wait Control Register1.

26.T58 is defined by I/O Wait Control Register2.

27.IO5WAIT* is sampled at the rising edge of the CKIO.

28.IO5WAIT* must be asserted before the time 'A' if IO5WAIT* is asserted.

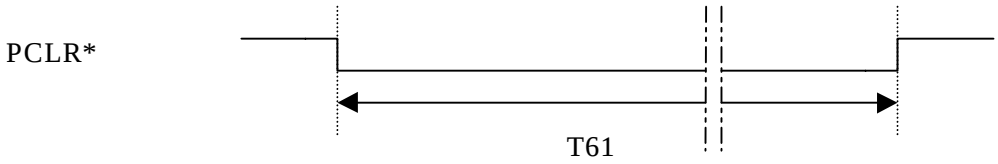
7.9. Interrupt Interface

All signals are asynchronous to CLKBUS.

7.10. Power Management Interface

All signals are asynchronous to CLKBUS.

7.11. PCLR



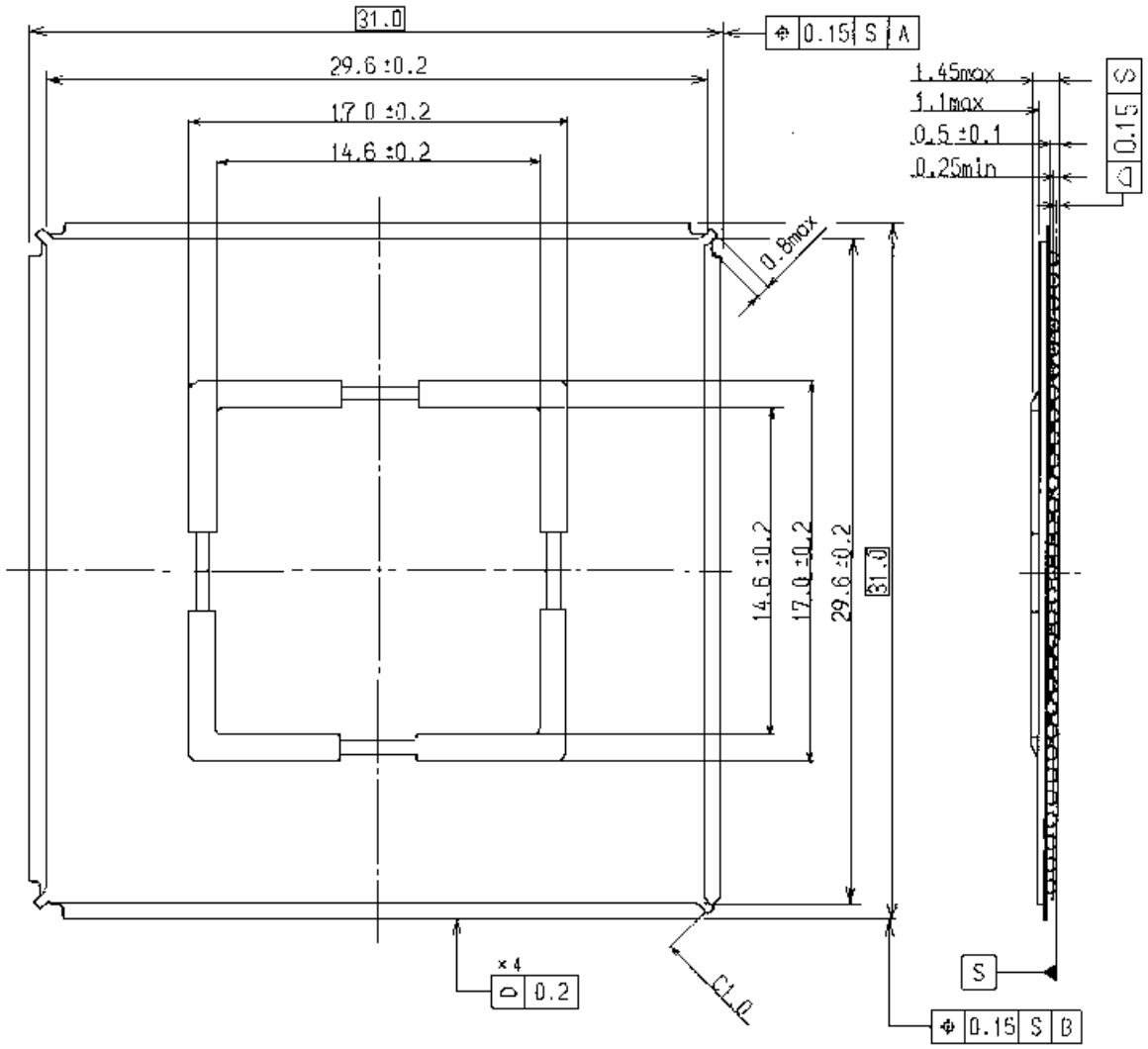
Item	Parameter	MIN	MAX	Unit	Note
T61	PCLR* asserted time	100	-	ns	

8. Package Dimension

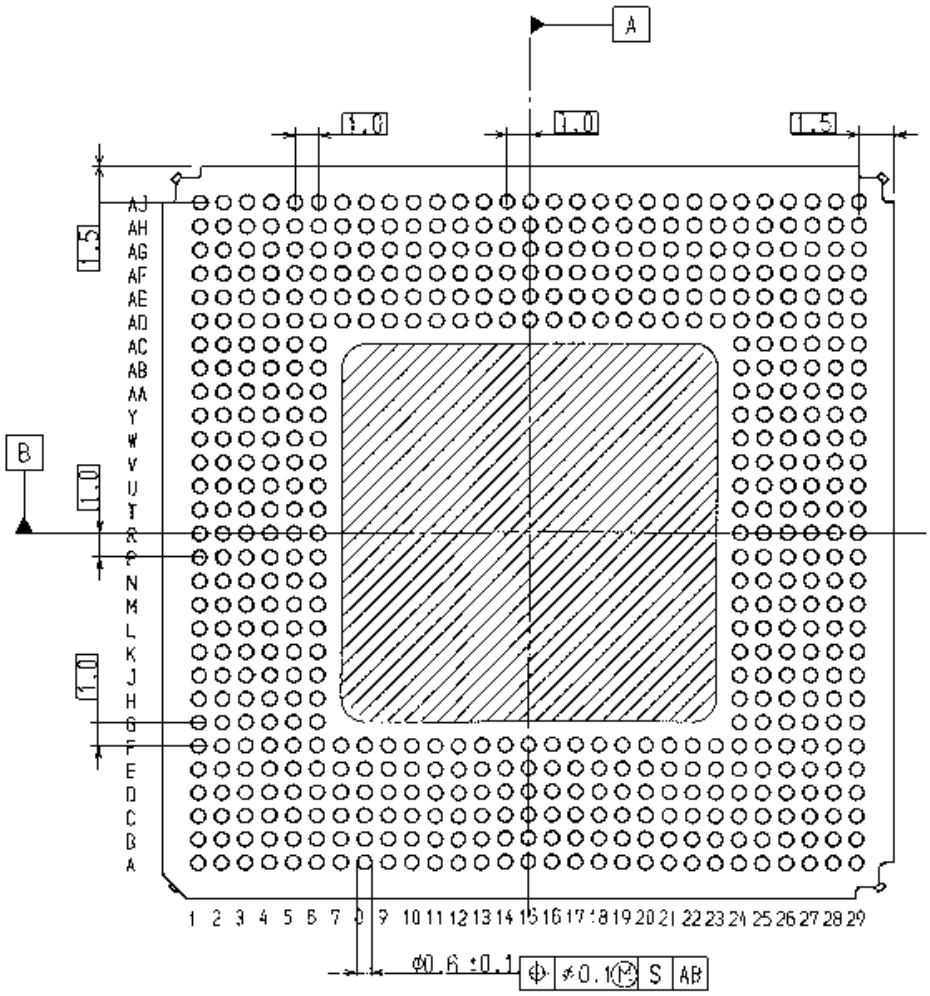
8.1. TC6358TB

TBGA552-3131-1.00B6 UNIT : mm

Top view



Bottom view


A
B
1.0
1.0
1.5
1.5
1.0
1.0
AJ AH AG AF AE AD AC AB AA Y W V U T R P N M L K J H G F E D C B A
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29
φ0.6 ±0.1
φ ≠0.1 M S AB