#### CMOS 4-BIT MICROCONTROLLER

### **TMP47P800N** TMP47P800F

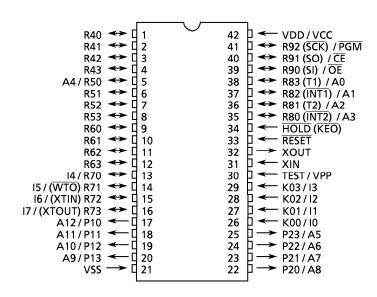
The 47P800 is the system evaluation LSI of 47C800 with 64K bits one-time PROM. The 47P800 programs / verifies using an adapter socket to connect with PROM programmer, as it is in TMM2764D.

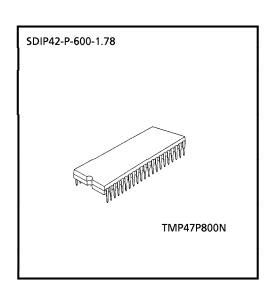
In addition, the 47P800 and the 47C800 are pin compatible. The 47P800 operates as the same as the 47C800 by programming to the internal PROM.

PART No.	ROM	RAM	PACKAGE	ADAPTER SOCKET
TMP47P800N	ОТР	E424 bit	SDIP42-P-600-1.78	BM1108
TMP47P800F	8192 × 8-bit	512 × 4-bit	QFP44-P-1414-0.80D	BM1111

### **PIN ASSIGNMENT (TOP VIEW)**

SDIP42-P-600-1.78





980901EBP1

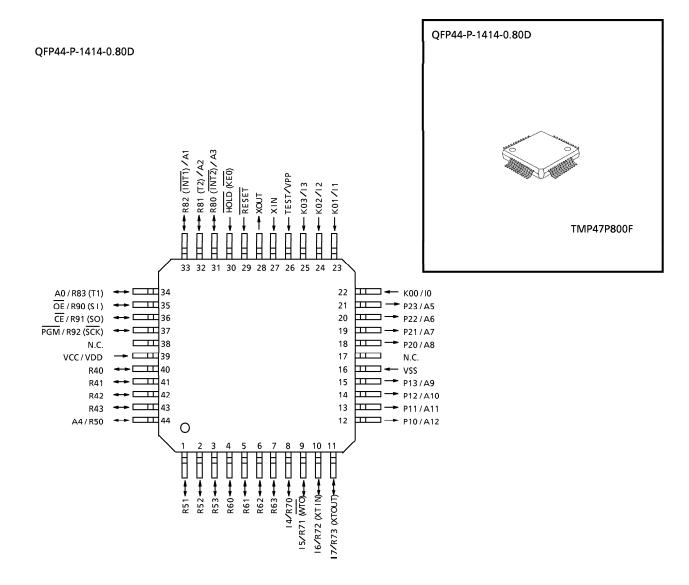
● For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter

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# **PIN ASSIGNMENT (TOP VIEW)**



### **PIN FUNCTION**

The 47P800 has MCU mode and PROM mode.

(1) MCU mode
The 47C800 and the 47P800 are pin compatible (TEST pin for out-going test. Be fixed to low level).

# (2) PROM mode

PIN NAME	Input/Output	FUNCTIONS	PIN NAME (MCU MODE)
A12 to A9			P10 to P13
A8 to A5	Input	Address inputs	P20 to P23
A4	·	Address in pats	R50
A3 to A0			R80 to R83
17 to 14	I/O	Data inputs / outputs	R73 to R70
13 to 10		Jata mpatty Catpata	K03 to K00
PGM		Program control input	R92
CE	Input	Chip Enable input	R91
ŌĒ		Output Enable input	R90
VPP		+ 21V / 5V (Program supply voltage)	TEST
vcc	Power supply	+ 5V	VDD
VSS		ov	VSS
R53 to R51			
R63 to R60	I/O	Be fixed to low level.	
R43, R42	1/0		
R41, R40			
RESET	Input PROM mode setting pins. Be fixed to low level.		
HOLD	Input		
XIN	Input	Resonator connecting pins	
хоит	Output	nesonates connecting pris	

#### **OPERATIONAL DESCRIPTION**

The following is an explanation of hardware configuration and operation in relation to the 47P800. The 47P800 is the same as the 47C800 except that an OTP is used instead of a built-in Mask ROM.

### 1. OPERATION MODE

The 47P800 has an MCU mode and PROM mode.

### 1.1 MCU mode

The MCU mode is set by fixing the TEST / VPP pin at the "L" level. Operation in the MCU Mode in the same as for the 47C800 except that the TEST / VPP pin does not have pull-down resistor and can not be used open.

### 1.1.1 Program memory

The program storage area is the same as for the 47C800.

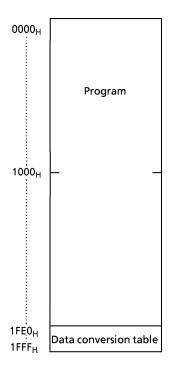


Figure 1-1. Program area

### 1.1.2 Data memory

The 47P800 has 256X4 bits data memory bank (RAM).

# 1.1.3 Input /Output Circuitry

(1) Control pins

This is the same as for the 47C800 except that there is no pull-down resistor for the TEST pin.

### (2) I/O ports

The input / output circuit of the 47C800 is the same as I/O code RA of the 47C800 external resistor, for example, is required when using as evaluator of other I/O codes (RB to RF) (Refer to Figure 1-2).

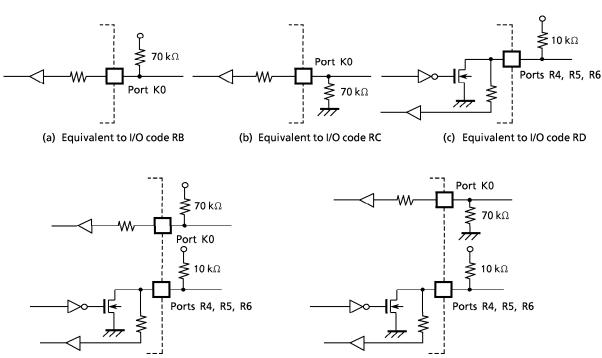


Figure 1-2. I/O code and external circuitry

(e) Equivalent to I/O code RF

(d) Equivalent to I/O code RE

### 1.2 PROM mode

The PROM mode is set by setting the RESET, HOLD, K00 and K01 pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification (A high-speed program mode is used set the ROM type the same as for the TMM2764D).

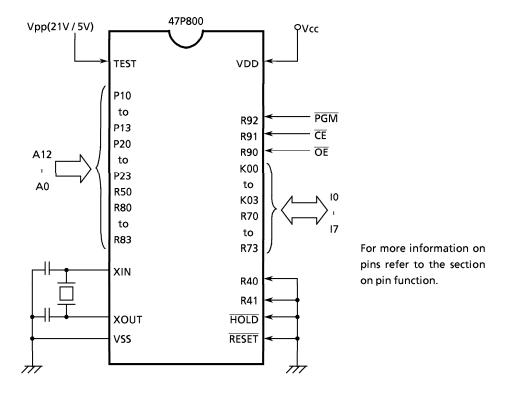
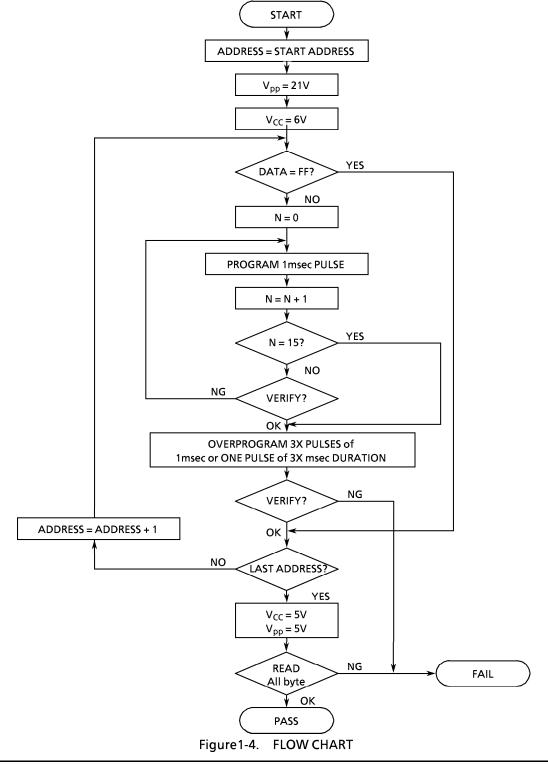


Figure 1-3. Setting for PROM mode

## 1.2.1 High Speed Programming Mode

The device is set up in the high speed programming mode when the programming voltage (21.0V) is applied to the VPP pin with Vcc = 6V and  $\overline{PGM} = V_{IH4}$ . The programming is achieved by applying a single TTL low level 1 msec, pulse the  $\overline{PGM}$  input after addresses and data are stable. Then the programmed data is verified by using program Verify Mode. If the programmed data is not correct, another program pulse of 1 msec is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 15 times). After correctly programming the selected address, one additional program pulse with pulse width 4 times that needed for programming is applied. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5V.



### **ELECTRICAL CHARACTERISTICS**

ABSOLUTE MAXMUM RATINGS  $(V_{SS} = 0V)$ 

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V <sub>DD</sub>		– 0.3 to 7	٧
Input Voltage	V <sub>IN</sub>		- 0.3 to V <sub>DD</sub> + 0.3	٧
	V <sub>OUT1</sub>	Except the sink open drain pin, but include R7	- 0.3 to V <sub>DD</sub> + 0.3	
Output Voltage	V <sub>OUT2</sub>	The sink open drain pin except R7	– 0.3 to 10	V
	I <sub>OUT1</sub>	Ports R	3.2	
Output Current (Per 1 pin)	I <sub>OUT2</sub>	Ports P1, P2	30	mA
Output Current (Total)	Σl <sub>OUT1</sub>	Ports P1, P2	120	mA
Power Dissipation [T <sub>opr</sub> = 70°C]	PD		600	mW
Soldering Temperature (time)	T <sub>sld</sub>		260 (10 s)	°C
Storage Temperature	T <sub>stg</sub>		– 55 to 125	°C
Operating Temperature	T <sub>opr</sub>		– 40 to 70	°C

RECOMMENDED OPERATING CONDITIONS

 $(V_{SS} = 0V, T_{opr} = -40 \text{ to } 70^{\circ}C)$ 

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
			in the Normal operating mode	4.5		
Supply Voltage High Input Voltage	$V_{DD}$		in the SLOW operating mode	2.7	6.0	V
			in the HOLD operating mode	2.0		
	V <sub>IH1</sub>	Except Hysteresis Input	V <sub>DD</sub> ≧ 4.5V	$V_{DD} \times 0.7$		
High Input Voltage	V <sub>IH2</sub>	Hysteresis Input	V <sub>DD</sub> = 4.3V	$V_{DD} \times 0.75$	V <sub>DD</sub>	V
	V <sub>IH3</sub>		VDD ( 4.5V	$V_{DD} \times 0.9$	$V_{DD}$ $V_{DD} \times 0.3$ $V_{DD} \times 0.25$ $V_{DD} \times 0.1$ $6.0$	
	$V_{IL1}$	VDD $\langle$ 4.5V $\rangle$ L1 Except Hysteresis Input $\rangle$ $V_{DD} \ge 4.5V$		$V_{DD} \times 0.3$		
Low Input Voltage	$V_{IL2}$	Hysteresis Input	V <sub>DD</sub> ≤ 4.5V	0	V <sub>DD</sub> × 0.25	V
	V <sub>IL3</sub>		V <sub>DD</sub> <4.5V		$V_{DD}$ $V_{DD} \times 0.3$ $V_{DD} \times 0.25$ $V_{DD} \times 0.1$	
Clask Francisco	fc	XIN, XOUT		0.4	6.0	MHz
Clock Frequency	fs	XTIN, XTOUT		30.0	V <sub>DD</sub> × 0.3 V <sub>DD</sub> × 0.25 V <sub>DD</sub> × 0.1	kHz

Note. Input voltage  $V_{IH3}$ ,  $V_{IL3}$ : in the SLOW or HOLD operation.

D.C. CHARACTERISTICS

 $(V_{SS} = 0V, T_{opr} = -40 \text{ to } 70^{\circ}C)$ 

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Тур.	Max.	UNIT
Hysteresis Voltage	$V_{HS}$	Hysteresis input		_	0.7	_	V
	I <sub>IN1</sub>	Port K0, TEST, RESET, HOLD	V <sub>DD</sub> = 5.5V				
Input Current	I <sub>IN2</sub>	Ports R (open-drain)	V <sub>IN</sub> = 5.5V / 0V	_	_	± 2	μΑ
Input Resistance	R <sub>IN2</sub>	RESET		100	220	450	kΩ
Output Leakage Current	I <sub>LO</sub>	Ports R, P (open drain)	V <sub>DD</sub> = 5.5V, V <sub>OUT</sub> = 5.5V	_	_	2	μΑ
Output Low Voltage	V <sub>OL2</sub>	Except XOUT XTOUT, Ports P1, P2	$V_{DD} = 4.5V$ , $I_{OL} = 1.6 \text{ mA}$	_	_	0.4	٧
Low Level Output Current	I <sub>OL1</sub>	Ports P1, P2	$V_{DD} = 4.5V, V_{OL} = 1.0V$	_	20	1	mA
Supply Current (in the Nomal mode)	I <sub>DD</sub>		V <sub>DD</sub> = 5.5V fc = 4 MHz	_	5	10	mA
Supply Current (in the SLOW mode)	I <sub>DDS</sub>		V <sub>DD</sub> = 5.0V fs = 32.768 kHz	_	5	8	mA
Supply Current (in the HOLD mode)	I <sub>DDH</sub>		V <sub>DD</sub> = 5.5V	_	0.5	10	μΑ

- Note 1. Typ. values show those at  $T_{opr} = 25^{\circ}C$ ,  $V_{DD} = 5V$ .
- Note 2. Input Current  $I_{IN1}$ ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.
- Note 3. Supply Current  $I_{DD}$ ,  $I_{DDH}$ ;  $V_{IN} = 5.3V/0.2V$ The K0 port is opened when the input resistor is contained. The voltage applied to the R port is within the valid range. Supply Current  $I_{DDS}$ ;  $V_{IN} = 2.8V/0.2V$ , low frequency clock is only oscillated (connecting

XTIN, XTOUT).

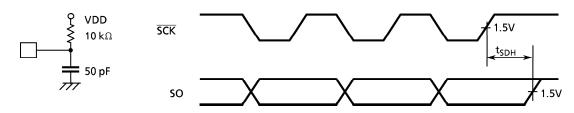
A.C. CHARACTERISTICS 
$$(V_{SS} = 0V, V_{DD} = 4.5 \text{ to } 6.0V, T_{opr} = -40 \text{ to } 70^{\circ}\text{C})$$

PARAMETER	SYMBOL	CONDITION	Min.	Тур.	Max.	UNIT	
Instruction Cycle Time	†	in the Normal mode	1.33	-	20	μS	
instruction cycle time	t <sub>cy</sub>	in the SLOW mode	235	-	267	μ3	
High level Clock Pulse Width	t <sub>WCH</sub>	For external clock operation	80	_	_	ns	
Low level Clock Pulse Width	t <sub>WCL</sub>	Tor external clock operation	00	_		115	
Shift Data Hold Time	t <sub>SDH</sub>		0.5t <sub>cy</sub> – 300	_	_	ns	

Note. Shift Data Hold Time:

External circuit for SCK pin and SO pin

Serial port (completion of transmission)



RECOMMENDED OSCILLATING CONDITIONS

(V<sub>SS</sub> = 0V, 
$$V_{DD}$$
 = 4.5 to 6.0V,  $T_{opr}$  =  $-40$  to  $70\,^{\circ}$ C)

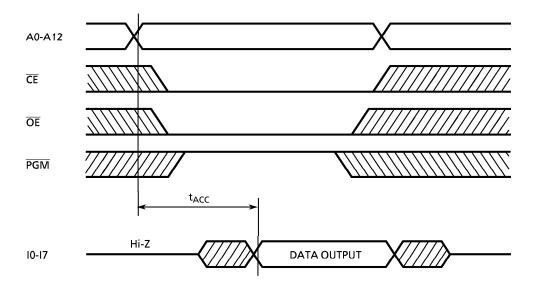
Recommended oscillating conditions of the 47P800 are equal to the 47C800's.

# D.C. / A.C. CHARACTERISTICS (PROM mode)

# $(V_{SS} = 0V)$

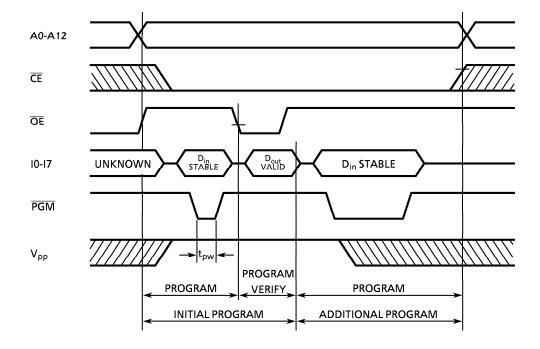
### (1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Тур.	Max.	UNIT
Output Level High Voltage	V <sub>IH4</sub>		V <sub>CC</sub> × 0.7	-	V <sub>CC</sub>	>
Output Level Low Voltage	V <sub>IL4</sub>		0	-	V <sub>CC</sub> × 0.12	<
Supply Voltage	V <sub>CC</sub>		4.75		6.0	V
Programming Voltage	V <sub>PP</sub>		4.75	_	6.0	\
Address Access Time	t <sub>ACC</sub>	$V_{CC} = 5.0 \pm 0.25 V$	0	-	350	ns



# (2) High Speed Programming Operation

PARAMETER	SYMBOL	CONDITION	Min.	Тур.	Max.	UNIT
Input High Voltage	V <sub>IH4</sub>		V <sub>CC</sub> × 0.7	-	V <sub>CC</sub>	٧
Input Low Voltage	V <sub>IL4</sub>		0	-	V <sub>CC</sub> × 0.12	V
Supply Voltage	V <sub>CC</sub>		4.75	-	6.0	V
V <sub>PP</sub> Power Supply Voltage	V <sub>PP</sub>		20.5	21.0	21.5	V
Programming Pulse Width	t <sub>PW</sub>	V <sub>CC</sub> = 6.0 ± 0.25V	0.95	1.0	1.05	ms



Difference compared with the 47C800
 The 47P800 is different from the 47C800 with respect to the following spec points.

PARAMETER SYMBOL	CONDITION	47C800 47P800				UNIT			
PARAIVIETER	STIVIBOL	CONDITION	Min.	Тур.	Max.	Min.	Тур.	Max.	UNII
Supply Voltage	V	in the NORMAL operation	4.5	_	6.0	4.5	_	6.0	V
Supply voltage	Supply Voltage V <sub>DD</sub>	in the SLOW 2.7	2.7	_	0.0	4.5		0.0	V
6 6	I <sub>DD</sub>	in the NORMAL operation	-	3	6	_	5	10	mA
Supply Current	I <sub>DDS</sub>	in the SLOW operation	I	30μA (V <sub>DD</sub> =	60μA = 3V)	1	5mA (V <sub>DD</sub>	8mA = 5V)	_

Note. Be fixed low level at MCU mode because of TEST pin does not have pull-down resistor.

### **TYPICAL CHARACTERISTICS**

