CMOS 4-bit Microcontroller

TMP47P186M / TMP47P187M

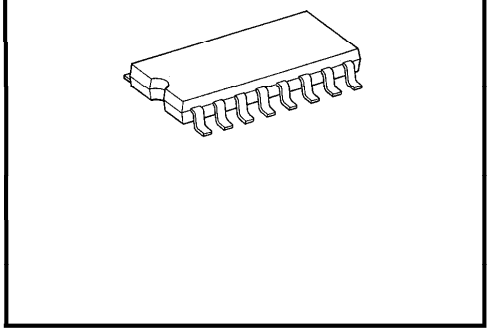
The TMP47P186M/187M is a system evaluation LSI with a built-in 1K-byte E²PROM as ROM. Like the MBM28C64, The TMP47P186M/187M can write / verify data using a PROM writer connection adaptor socket.

The TMP47P186M/187M is pin-compatible with mask ROM product TMP47E186M/187M. Writing a program to the built-in E²PROM enables the TMP47P186M/187M to operate the same as TMP47E186M/187M.

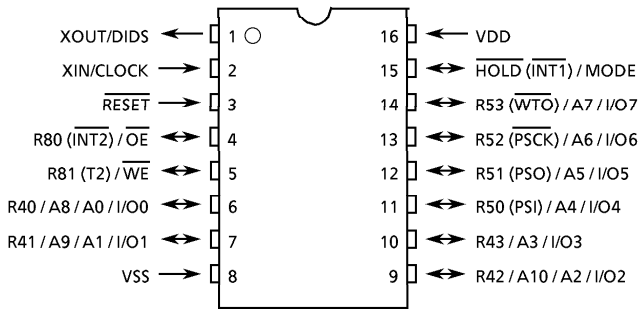
Part No.	ROM	RAM	E²PROM	Package	Adaptor socket	Oscillator
TMP47P186M	E²PROM	64 × 4 bit	16 × 8 bit	SOP16-P-300-1.27	BM11114	CR oscillator
TMP47P187M	1024 × 8 bit					crystal/ceramic oscillator

PIN ASSIGNMENT (TOP VIEW)

SOP16-P-300-1.27



SOP16-P-300-1.27



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PIN FUNCTIONS

The TMP47P186M/187M supports MCU and E²PROM modes.

(1) MCU mode
Pin-compatible with TMP47E186M/187M.

(2) E²PROM mode

PIN NAME	Input / Output	FUNCTION	PIN NAME (IN MCU MODE)
A10 to A8	Input	Inputs program memory addresses.	R42 to R40 *1
A7 to A4			R53 to R50 *1
A3 to A0			R43 to R40 *1
I/O7 to I/O4	Input / Output	Inputs / outputs program memory data.	R53 to R50 *1
I/O3 to I/O0			R43 to R40 *1
$\overline{OE}$	Input	Inputs output enable signal.	R80
$\overline{WE}$		Inputs write enable signal.	R81
$\overline{CE}$		Inputs chip enable signal.	$\overline{HOLD}$ (MODE) *2
CLOCK *3	Input	Oscillator connecting pin	XIN
DIDS *3	Input	Inputs address input timing control signal.	XOUT
VCC	Power supply	+ 5 V (or other voltage)	VDD
VSS		0 V (GND)	VSS

**1 : R43 to R40 and R53 to R50 are used in time sharing mode for input of program memory address and program memory data.*

**2 : The MODE signal is processed by the adaptor socket. The MODE signal, not the CE signal, is input to the HOLD pin.*

**3 : Generated by the adaptor socket.*

OPERATION

The following sections describe the configuration and operation of TMP47P186M/187M hardware. The TMP47P186M/187M uses the mask ROM built into TMP47E186M/187M as E²PROM. In every other respect, TMP47P186M/187M configuration and functions are identical to those of TMP47E186M/187M.

1. Operation modes

The TMP47P186M/187M supports MCU and E²PROM modes.

Mode \ Pin	XIN	XOUT	R80
MCU	Oscillator connected.		*
E²PROM	Clock input	L	H

L : 0 V
H : 5 V
* : don't care

Table 1 Operating Mode Setting

1.1 MCU Mode

Operation in MCU mode is the same as that of TMP47E186M/187M.

1.1.1 Program Memory

The program area is the same as that of TMP47E186M/187M.

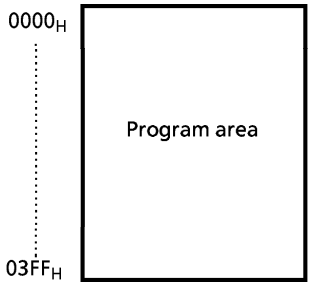


Figure 1.1.1 Program Area

1.1.2 Data Memory

The TMP47P186M/187M incorporates a 64 x 4-bit data memory (RAM, equivalent to TMP47E186M/187M).

1.1.3 Pin I/O Circuit

The pin I/O circuit is the same as that of TMP47E186M/187M.

1.2 E^2PROM mode

When reset ($\overline{RESET}$ pin = low), fixing to XOUT pin = low and R80 pin = high, inputting clock to XIN, and setting the $\overline{RESET}$ pin to high enters E^2PROM mode. In E^2PROM mode, programs can be written or verified in E^2PROM (1024 × 8bit) using the general-purpose PROM writer. (Set ROM type to MBM28C64 equivalence.)

1.2.1 Operating Modes in E^2PROM Mode

Mode \ Pin		$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	A	Operating state
Read	Data	L	L	H	D_{OUT}	Address	Operating
	Data polling				O7 = I7, O0 to I6 = Hi-Z		Writing
Standby		H	*	*	Hi-Z	*	Standby
Output disable		L	H	H			Operating
Write (single byte)		L	H	L	D_{IN}	Address	Writing
Write inhibit (No.1)		*	L	*	—	—	—
Write inhibit (No.2)		*	*	H			
Batch	Write (all-byte)	L	HV	L	all "L"	*	Writing
	Chip erase				all "H"		
	Security program				"FE_H"		

L : 0
H : 5 V
HV : 12 to 15 V
Hi-Z : High impedance
D_{IN} : Data input
D_{OUT} : Data output
* : don 't care

Table 1.2.1 Operating Mode Settings (In E^2PROM mode)

1.2.1.1 Read Mode ($\overline{CE}$ = $\overline{OE}$ = L, $\overline{WE}$ = H)

Setting the $\overline{CE}$ and $\overline{OE}$ pins to low level and the $\overline{WE}$ pin to high level enters read mode. Read mode has two functions: a data function to read internal data and a data polling function to detect termination of data write.

(1) Data function (Read data during normal operation)
When data are read during normal operation (except writing), the data at addresses specified by pins A0 to A12 are output to the I/O pins.

(2) Data polling function (Read data while writing data)
When data are read while writing data, the data being written ($\overline{I7}$) are output in inverted form to I/O pin 7. I/O pins 0 to 6 become high impedance.
This function enables detection of the termination of data write without using any additional external circuits.
Setting the $\overline{CE}$ or $\overline{OE}$ pin to high level sets the internal data bus and I/O pin to high impedance.

1.2.1.2 Standby Mode ($\overline{CE}$ = H)

Setting the $\overline{CE}$ pin to high level enters standby mode. This mode disables the E^{2}PROM and sets the I/O pins to high level.

1.2.1.3 Output Disable Mode ($\overline{CE}$ = L, $\overline{OE}$ = $\overline{WE}$ = H)

Setting the $\overline{CE}$ pin to low level and the $\overline{OE}$ and WE pins to high level enters output disable mode. In this mode, E^{2}PROM operates but the I/O ports are at high impedance.

1.2.1.4 Write (Single Byte) Mode ($\overline{CE}$ = $\overline{WE}$ = L, $\overline{OE}$ = H)

Setting the $\overline{CE}$ and $\overline{WE}$ pins to low level and the $\overline{OE}$ pin to high level enters write (single byte) mode. In this mode, only a single byte of the I/O pin data is written to the address specified by pins A0 to A12. Address input is latched at the falling edge of pin $\overline{CE}$ or $\overline{WE}$. Conversely, data input is latched at the rising edge of pin $\overline{CE}$ or $\overline{WE}$. Therefore, there is no need to save the address or data during write. The write timing is determined by the timing for setting the $\overline{CE}$ or $\overline{WE}$ pin to low level ($\overline{CE}$ control or $\overline{WE}$ control).

(1) $\overline{CE}$ control
When the $\overline{OE}$ pin at high level and the $\overline{WE}$ pin at low level, set the $\overline{CE}$ pin to low level (data write at $\overline{CE}$ = L).

(2) $\overline{WE}$ control
When the OE pin at high level and the $\overline{CE}$ pin at low level, set the $\overline{WE}$ pin to low level (data write at $\overline{WE}$ = L).

1.2.1.5 Write Inhibit Mode (No.1: $\overline{OE}$ = L, No.2: $\overline{WE}$ = H)

Setting the $\overline{OE}$ pin to low level enters write inhibit No.1 mode. Setting the $\overline{WE}$ pin to high level enters write inhibit No.2 mode. Data are not written in either of the write inhibit modes.

1.2.1.6 Batch Mode ($\overline{CE}$ = $\overline{WE}$ = L, $\overline{OE}$ = HV)

Setting the $\overline{CE}$ and $\overline{WE}$ pins to low level, and the $\overline{OE}$ pin to high voltage (12 to 15 V) enters batch mode. Batch mode includes three functions: write (all-byte) function, chip erase function, which simultaneously erases all bytes, and security program function, which maintains data confidentiality by preventing data from being read after they are written.

(1) Write (all-byte) function (I/O 0 to 7 = L)
In batch mode, setting all the I/O pins to low level and applying a low pulse to the $\overline{WE}$ pin writes all bytes at a time.

(2) Chip erase function (I/O 0 to 7 = H)
In batch mode, setting all the I/O pins to high level and applying a low pulse to the $\overline{WE}$ pin erases all bytes at a time.

(3) Security program function (I/O 0 to 7 = FE H)
In batch mode, applying a low pulse to the $\overline{WE}$ pin while outputting FEH to the I/O pins disables subsequent data reads. After security program execution, only the chip erase function can be used.
This function preserves data confidentiality.

1.2.2 E^2PROM Data Protection

E^2PROM has no data protection. To access the E^2PROM, set the registers of E^2PROM by the instruction. If TMP47E186M/187M is operated out of the guaranteed range, data in the E^2PROM may be changed by the runaways of the CPU. Under the condition out of the guaranteed range, such as power on or power off, please use the power-on-reset circuit and reset IC to reset the MCU certainly.

1. After power on, keep active Reset until Vcc stabilized.
2. Do not power off during E^2PROM access.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS	SPECIFICATION	UNIT
Supply voltage	V_{DD}		– 0.3 to 6.5	V
Input voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	V
Output current (per pin)	V_{OUT1}		3	mA
Output current (total for all pins)	ΣI_{OUT2}		12	mA
Power dissipation	PD		88	mW
Soldering temperature (time)	Tsld		260 (10 s)	°C
Storage temperature	Tstg		– 55 to 125	°C
Operating temperature	T_{OPR}		– 40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0 V, Topr = – 40 to 85 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS		Min.	Max.	UNIT
Supply voltage	V_{DD}	In the normal mode	Crystal *1 ceramic	fc = 6.0 MHz	4.5	5.5	V
				fc = 4.2 MHz	2.7		
			CR *2	fc = 2.5 MHz	2.2	3.4	
				fc = 1 MHz	2.0		
		In the hold mode	–	–	2.0	5.5	
Input high voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.9$		
Input low voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.1$	
Clock frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		0.4	6.0	MHz
			V_{DD} = 2.7 to 5.5 V			4.2	
			V_{DD} = 2.2 to 5.5 V (CR)			2.5	
			V_{DD} = 2.0 to 5.5 V (CR)			1.0	

*1 : TMP47P187M

*2 : TMP47P186M

DC CHARACTERISTICS

(V_{SS} = 0 V, Topr = – 40 to 85 °C)

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Hysteresis voltage	V_{HS}	Hysteresis input		–	0.7	–	V
Input current	I_{IN1}	$\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V	–	–	± 2	μA
Input resistance	R_{IN}	$\overline{RESET}$		100	220	450	kΩ
High-level output current	V_{OH}	Push-pull output portH	VDD = 4.5 V, IOH = – 1.6 mA	2.4	–	–	V
			VDD = 2.2 V, IOH = – 20 μA	2.0	–	–	
Low-level output voltage	V_{OL}	Excluding XOUT	VDD = 4.5 V, IOL = 1.6 mA	–	–	0.4	V
			VDD = 2.2 V, IOL = 20 μA	–	–	0.1	
Power supply current at normal operation	I_{DD}	Except for E²PROM Erase / write	V_{DD} = 5.5 V, fc = 4 MHz	–	2	4	mA
			V_{DD} = 3.0 V, fc = 4 MHz	–	1	2	
			V_{DD} = 3.0 V, fc = 400 kHz	–	0.5	1	
		During E²PROM Erase / write	V_{DD} = 5.5 V, fc = 4 MHz	–	5	7	
Power supply current in hold mode	I_{DDH}		V_{DD} = 5.5 V	–	0.5	10	μA
			V_{DD} = 3.0 V	–	0.3	1	

Note 1 : Typ. values are for when Topr = 25 °C, V_{DD} = 5 V.

Note 2 : Input current: IIN1 excludes current due to built-in pull-up resistors.

Note 3 : VIN = 5.3 V / 0.2 V (V_{DD} = 5 V) or VIN = 2.8 V / 0.2 V (V_{DD} = 3.0 V)

Data (16 × 8 bit) E²PROM CHARACTERISTICS

(V_{SS} = 0 V, Topr = – 40 to 85 °C)

PARAMETER	SYMBOL	CONDITIONS		UNIT
Programming time	t_{PW}		4.1 (Typ.)	ms
Erase time	t_{EW}		4.1 (Typ.)	
Number of overwrites		Topr = T_H, V_{DD} = 5 V	10^4 (Min.)	Cycle
Data hold characteristics		After overwriting 10^4 times, Ta = 55 °C.	10 (Min.)	Year

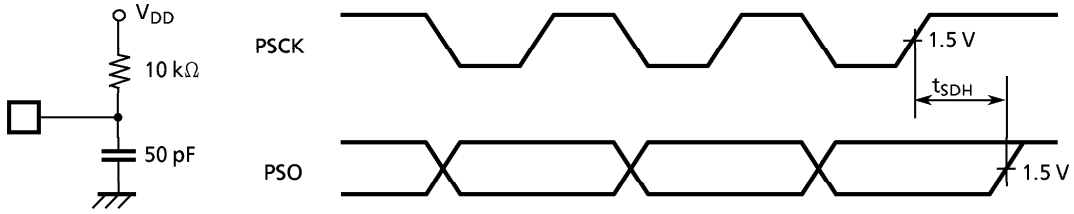
AC CHARACTERISTICS

(V_{SS} = 0V, Topr = – 40 to 85 °C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Instruction cycle time	tcy		V_{DD} = 4.5 to 5.5 V	1.3	–	20	μs
			V_{DD} = 2.7 to 5.5 V	1.9			
			VDD = 2.2 to 5.5 V	3.2			
			VDD = 2.0 to 5.5 V	8.0			
High-level clock pulse width	t_{WCH}	External clock (XIN input)	$V_{DD} \geqq 2.7$ V	80	–	–	ns
			$V_{DD} < 2.7$ V	160			
Low-level clock pulse width	t_{WCL}		$V_{DD} \geqq 2.7$ V	80			
			$V_{DD} < 2.7$ V	160			
Shift data storage time	t_{SDH}			0.5tcyc – 300	–	–	ns

Note : Shift data hold time:
$\overline{PSCK}$, PSO pin, External circuit

Serial port (end of transmission)



RECOMMENDED OSCILLATION CONDITIONS

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 40 to 85 °C)

Same as those for TMP47E186M/187M.

CAUTIONS

TMP47E186M/187M and TMP47P186M/187M are covered by a patent agreement between Toshiba Corporation and Bull CP8. These products cannot be used with IC cards and other portable devices (as defined below).

"PORTABLE DEVICE"

(I) A portable piece of equipment with a length or breadth ±10 mm, and a thickness ±3 mm of the dimensions defined under ISO standard 7816, or

(II) A portable device conforming to the electrical connection layout and shape specified under ISO standard 7816, part 2, or

(III) A portable and pocket-size device for the identification of the carrier of the device or of the device itself, and for the accumulation of information relating to the carrier of the device or the device itself.