SOT-3 Device
STM-1/STS-3/STS-3c Overhead Terminator
TXC-03003B

DATA SHEET

FEATURES

- Transport (Section) and Line Overhead byte processing
- Independent Path Overhead byte processing
- Transmit and receive pointer generation with respect to external clock and frame signals
- Line interface: byte-parallel data, clock and frame signals
- Terminal interface: byte-parallel data, clock, C1J1, SPE, parity bit and path overhead indication signals
- SDH/SONET alarm detection
- Alarm Indication Port (AIP) for path-protected ring applications
- VTAIS and Path AIS generation on alarms
- Downstream fault indications inserted in E1 byte
- Performance monitoring: B1, B2 and B3 coding violations, FEBE and pointer justification counts
- Microprocessor access:
  - Pin selectable for Intel or Motorola interface
  - Hardware/software interrupt capability
- Receive and transmit section and line overhead bytes available from on-chip RAM and via a serial I/O port
- Source timing mode: transmit side provides downstream device timing (optional V1 pulse)
- Data communication mode: for STM-1 VC-4/ STS-3c use
- Single +5 V, ±5 % power supply
- 160-pin 28 x 28 mm plastic quad flat package

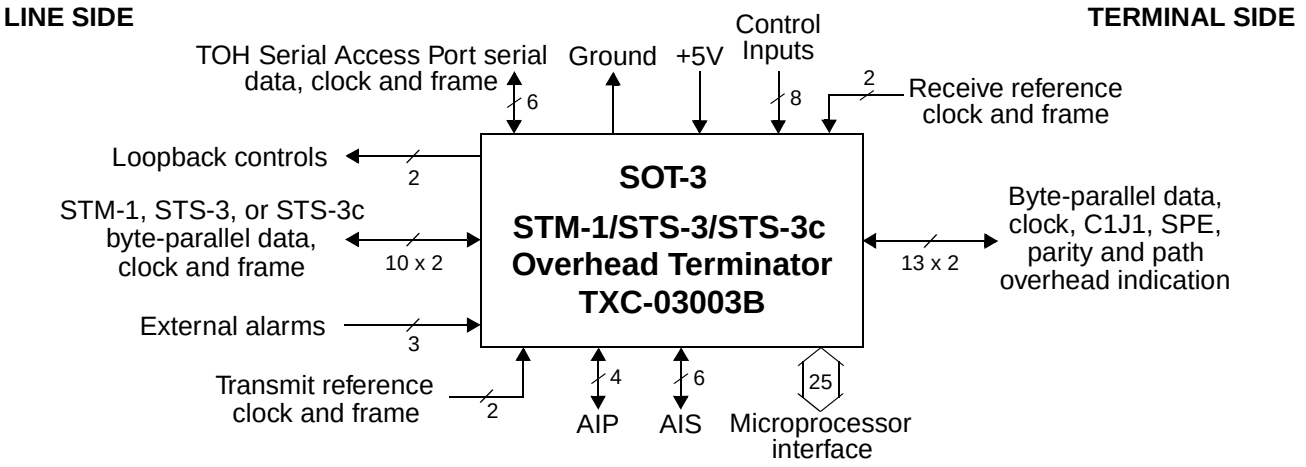
DESCRIPTION

The SOT-3 SDH/SONET overhead terminator is a programmable device that performs section, line and path overhead processing for STM-1/STS-3/STS-3c signals. The SOT-3 device performs pointer generation (with internal pointer justification) with respect to external clock timing in both the transmit and receive directions. It automatically adjusts pointers to account for differences between the input clock and frame, and the reference clock and frame. All overhead bytes are provided in the SOT-3 memory map with access via a microprocessor port and a serial I/O port.

The SOT-3 device generates path AIS and sends downstream AIS information via the E1 bytes. It also provides a serial Alarm Indication Port for use in path-protected ring architectures. In the transmit direction, section and line overhead bytes may be multiplexed into the signal from either the memory map or from the external serial interface.

APPLICATIONS

- Supports Telecom Bus and dual ring mode applications
- Add/drop multiplexer
- Digital cross-connect
- High speed data communication



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LIST OF FIGURES

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BLOCK DIAGRAM

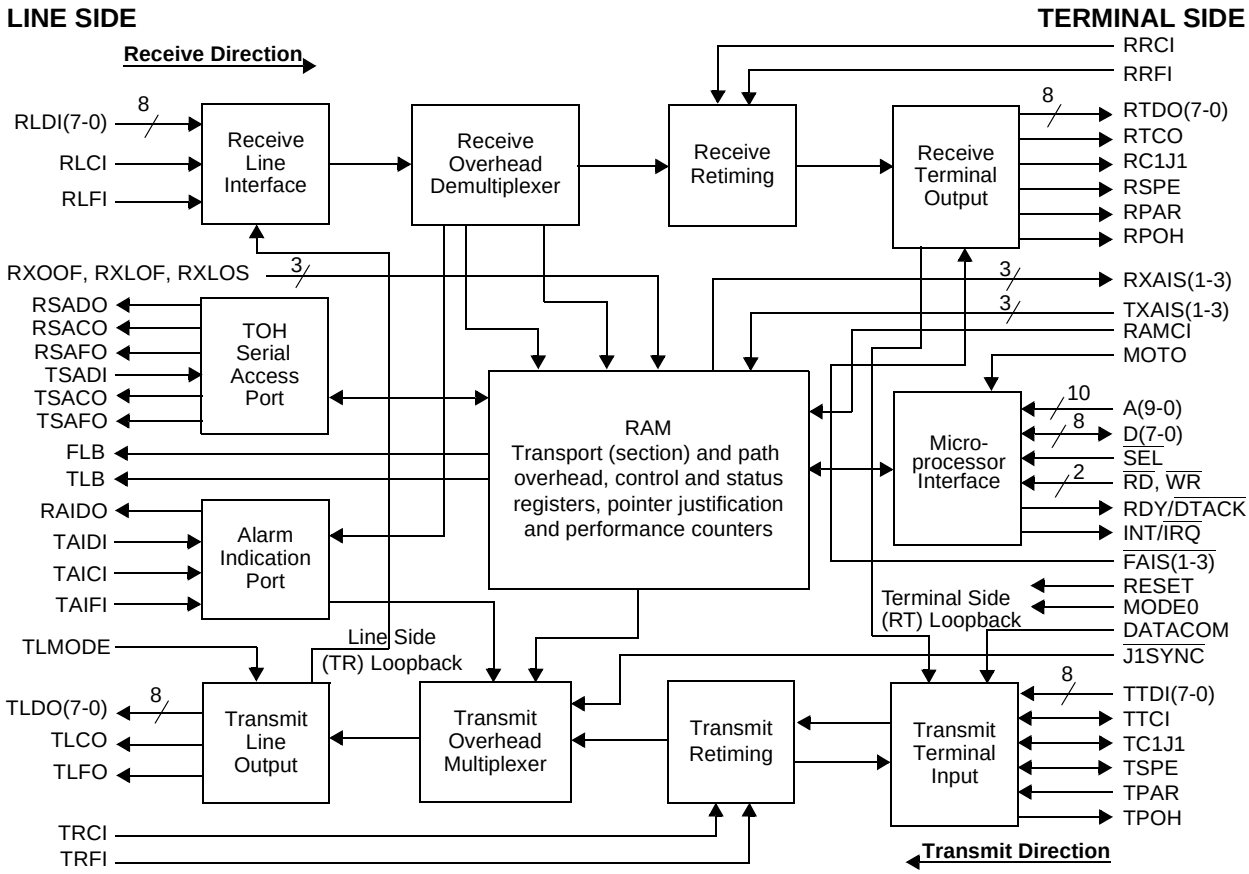


Figure 1. SOT-3 TXC-03003B Block Diagram

BLOCK DIAGRAM DESCRIPTION

A simplified block diagram of the SOT-3 device is shown in Figure 1. Each functional group of blocks in this diagram is described briefly in the following subsections. Supplemental detail is provided in the Operation section, which has the same order of presentation as this section, i.e., receive direction, transmit direction (including the bidirectional topics of parity and throughput delay) and auxiliary functions. The Pin Descriptions section provides information on the pins associated with each function, in the same order, with controls grouped at the end. Timing diagrams are provided in Figures 3 through 17.

RECEIVE DIRECTION

Receive Line Interface Block

The Receive Line Interface block terminates the receive line signals, which are derived from the line signal in an external STM-1/STS-3 155 Mbit/s framer device, such as the TranSwitch SYN155 Synchronizer VLSI device (TXC-02301B). The external framer device performs the functions of scrambling/descrambling, B1 byte BIP-8 generation and checking, and serial to byte conversion of the data stream. Byte-parallel data (RLDI(7-0)) and a framing pulse (RLFI) are clocked into the SOT-3 device from the framer on rising edges of a 19.44 MHz

clock (RLCI), as shown in Figure 3. Pin RLDI7 carries the most significant bit (MSB) of the data byte, which corresponds to bit 1 in a SDH/SONET serial bit stream. In addition, the SOT-3 device provides external alarm input pins for Receive Out Of Frame (RXOOF), Receive Loss Of Frame (RXLOF) and Receive Loss Of Signal (RXLOS) alarms. These external receive alarm indications are stored as status bits in the SOT-3 RAM block, from which they may be read via the Microprocessor Interface block by a read cycle of an external microprocessor. The SOT-3 device provides two output pins (FLB and TLB), driven by corresponding control bits in RAM, which can be used to invoke Facility Loopback and Terminal Loopback in the external framer device.

Receive Overhead Demultiplexer Block

The Receive Overhead Demultiplexer block writes the 81 STM-1 Section Overhead bytes or the 81 STS-3/STS-3c Transport Overhead bytes to the RAM block, where they are available for microprocessor access. The bytes are also provided at the output of the Transport Overhead Byte (TOH) Serial Access Port block for external processing. The Receive Overhead Demultiplexer block also performs the TOH processing of the B2 byte BIP-8 parity, line FEBE checking, K1 and K2 byte checking for an inconsistent APS and for a new APS indication, and detection of line RDI and line AIS prior to pointer tracking. A pointer tracking state machine interprets the incoming pointer bytes H1 and H2 to determine the location of the J1 Path Overhead (POH) byte. Pointer tracking is performed according to the latest ETSI and ANSI standards, with loss of pointer and AIS alarms reported for the STM-1 AU-4/STS-3c or for the three STS-3:STS-1 signals. Three sets of three eight-bit counters are provided to count pointer increments, decrements and New Data Flag (NDF) occurrences.

After pointer tracking, the Receive Overhead Demultiplexer block writes the Path Overhead bytes into RAM locations, and performs B3 BIP-8 parity checking and counts the number of detected bit or block errors. An H4 multiframe detector is provided with an optional V1 pulse generator. Control bits also permit the H4 byte to pass through the receiver transparently. A circuit is provided for C2 Mismatch and Unequipped detection, with alarm indications. The G1 byte is checked for an RDI status, and the number of FEBE errors is counted.

Receive Retiming Block

The Receive Retiming block provides pointer justification for the STM-1 VC-4/STS-3c signal or for each of the three STS-1 signals. The VC-4 or STS-1 signals, which consist of the POH bytes and payload, are justified to two external reference signals, which are a framing pulse (RRFI) and a clock (RRCI). The VC-4 consists of 2349 bytes (261 columns times 9 rows). Each of the three STS-1 signals in the STS-3 signal consists of 783 bytes (87 columns times 9 rows).

Receive Terminal Output Block

The Receive Terminal Output block provides a receive output interface for byte-parallel data (RTDO(7-0)), a 19.44 MHz clock signal (RTCO), a composite C1J1 signal (RC1J1) with an optional V1 signal, an SPE signal (RSPE) that identifies the POH byte and payload byte times, a path overhead indicator signal (RPOH), and an odd or even parity indication bit (RPAR), as shown in Figure 6. Parity is calculated over the data (RTDO(7-0)), the C1J1 (RC1J1) and the SPE (RSPE) signals only. The RTDO7 bit is the MSB and represents bit 1 in a SDH/SONET serial bit stream. The C1J1 signal is used in conjunction with the SPE signal to determine the location of the various bytes in the SDH/SONET signal. A high pulse on the RC1J1 pin indicates a C1 pulse when the RSPE pin is low, and a J1 (or V1) pulse when RSPE is high, as illustrated in Figure 22. The C1 pulse identifies the location of the first C1 byte in the SDH/SONET frame. A single J1 pulse, one clock cycle wide, identifies the starting location of the J1 byte in the Path Overhead bytes in the VC-4 format. Three J1 pulses are provided for the STS-3 format, each identifying the starting location of the J1 byte in one of the three STS-1 signals.

The optional V1 pulse is used to determine the starting location of the V1 bytes in asynchronous mapping formats such as VT1.5. For STM-1 VC-4 operation, an optional single V1 pulse, one clock cycle wide, will occur once every four frames following the J1 pulse. For STS-3 operation, three V1 pulses may be present every four frames. Each V1 pulse will occur on the third clock cycle after the corresponding J1 pulse, when the SPE signal is high. For example, in a VC-4 signal carrying TUG-3 signals, the J1 pulse identifies the J1 byte location (defined as the starting point for the VC-4) in the POH bytes. In the next column (first clock cycle), all the rows

are assigned as fixed stuff. Similarly, in the next column (second clock cycle), all the rows are assigned as fixed stuff. The next column (third clock cycle), which carries a Null Pointer Indication, defines the start of the TUG-3 designated as “A”. This column is where the V1 pulse occurs every four frames. However, the actual V1 byte occurs six clock cycles after the V1 pulse.

Receive side Alarm Indication Signals are provided at the terminal side outputs, as shown in Figures 18-20.

TRANSMIT DIRECTION

Transmit Terminal Input Block

In the transmit direction, the Transmit Terminal Input block, when operating in the normal mode, provides an input interface for byte-parallel data (TTDI(7-0)), a 19.44 MHz clock signal (TTCI), a composite C1J1 signal (TC1J1) with an optional V1 input signal, an SPE signal (TSPE) that identifies the POH byte and payload byte times, and an odd or even parity indication (TPAR). Internal parity is calculated over the data, C1J1 and SPE signals, or for the data byte only, with the sense (odd or even) of the calculation determined by the value of a bit in a control register. The result of this parity calculation is compared with the input signal present on the parity pin (TPAR). Other than providing an error indication, the SOT-3 device takes no action when a parity error is detected. The TTDI7 bit is the MSB and represents bit 1, the first bit transmitted in a SDH/SONET serial bit stream. The TC1J1 signal is used in conjunction with the TSPE signal to determine the location of the various parts of the SDH/SONET signal (see Figures 7 and 22).

In the data communication (datacom) and source timing modes, the 19.44 MHz clock signal (TTCI), the composite C1J1 signal (TC1J1), and the SPE signal (TSPE), become output signals. In the data communication mode, which is intended for STM-1 VC-4/STS-3c operation, the TSPE output signal, with the MODE0 pin high, is active for the payload byte times only (260 bytes per row). The TSPE signal is low during the Transport Overhead byte times and the single Path Overhead byte time. With the MODE0 pin low, the TSPE is high for the 258 payload times only, and low for the nine TOH byte times as well as the POH byte time and the two byte time slots immediately following. In addition, a Path Overhead byte indication signal (TPOH) is provided for identifying the POH byte times (see Figure 8). In the source timing mode, the TSPE output signal is active for the Path Overhead and payload byte times (261 bytes per row). The TSPE signal is low during the Transport Overhead byte times. An internal H4 multiframe generator provides an optional V1 pulse for the C1J1 (TC1J1) output signal (see Figures 9 and 22). The V1 pulse is synchronous with the transmitted H4 byte for the STM-1 VC-4 format, or there may be up to three V1 pulses, one for each of the three STS-1 signals. The optional V1 pulse is used to determine the starting location of the V1 byte in asynchronous mapping formats such as VT1.5 for multiple VT add/drop devices.

Transmit Retiming Block

The Transmit Retiming block provides pointer justification for the STM-1 VC-4/STS-3c signal or for each of the three STS3:STS-1 signals. The VC-4 or STS-1 signals, which consist of the POH bytes and payload, are justified to two external reference signals, a framing pulse (TRFI) and a clock (TRCI). The VC-4 consists of 2349 bytes (261 columns times 9 rows). Each of the three STS-1 signals in the STS-3 signal consists of 783 bytes (87 columns times 9 rows).

Transmit Overhead Multiplexer Block

The Transmit Overhead Multiplexer block performs the multiplexing of the Transport Overhead (TOH) and Path Overhead (POH) bytes into the SDH/SONET signal. The TOH bytes are inserted from RAM locations, which may be written either by the external microprocessor or from the TOH Serial Access Port. Control bits select the source of these bytes, as shown in Figures 24 and 25. Path overhead bytes may accompany the payload bytes, or they may be multiplexed into the transmitted signals from microprocessor-written RAM locations. The Transmit Overhead Multiplexer block also controls the state of the Path RDI alarm (bit 5 in the G1 byte) and Line RDI (bits 6-8 of the K2 byte), and the generation of Path and Line AIS and FEBE signals.

Transmit Line Output Block

The Transmit Line Output block provides transmit line signals for an external STM-1/STS-3 155 Mbit/s framer device, such as the TranSwitch SYN155 Synchronizer VLSI Device (TXC-02301B). The interface consists of a byte-parallel data output signal (TLDO(7-0)), a clock signal (TLCO), and a framing pulse (TLFO). The signals are derived from the reference clock (TRCI) and reference framing pulse (TRFI) input signals. The framing pulse may be active high or low, depending upon the state of the TLMODE pin. Data and the framing pulse are clocked out on falling edges of the clock TLCO when TLMODE is high, and on rising edges when TLMODE is low, as shown in Figures 4 and 5. TLDO7 is the MSB and represents bit 1, the first bit transmitted in a SDH/ SONET serial bit stream.

AUXILIARY FUNCTIONS

Transport Overhead Byte Serial Access Port Block

The Transport Overhead Byte (TOH) Serial Access Port block provides serial receive and transmit interfaces for the 81 Line Overhead and Section Overhead bytes in the SDH/SONET format, as shown in Figures 10 and 11. The receive interface consists of serial data (RSADO), a clock signal (RSACO), and a framing pulse (RSAFO). Data is clocked out on falling edges of RSACO. The framing pulse RSAFO identifies the location of bit 1 (MSB) of the first C1 byte. The transmit interface consists of a serial data input signal (TSADI), an output clock signal (TSACO), and framing pulse (TSAFO). Data is clocked in on rising edges of TSACO. The framing signal TSAFO identifies the starting location of bit 1 in the C1 byte.

Alarm Indication Port Block

The SOT-3 device supports a ring architecture using the Alarm Indication Port (AIP) block. The Alarm Indication Port receive output consists of serial data (RAIDO) and the receive clock and framing outputs of the TOH Serial Access Port block (RSACO and RSAFO), as shown in Figure 12. Alarm information to be used by the mate SOT-3 device in a ring architecture is clocked out on falling edges of the clock. Only the first 40 of the 81 RSACO clock cycles are used by the AIP. The serial data format consists of the corresponding 40 bits, numbered 39 through 0. Bit 39 is the MSB and is the first bit transmitted at the interface. The format conveys line and path FEBE information, line and path RDI alarm information, APS information, and the debounced K1 and K2 bytes, as shown in Figure 25.

The receive interface output signals, data (RAIDO), clock (RSACO) and framing (RSAFO), are connected to the transmit interface of the Alarm Indication Port of the mate SOT-3 device. The transmit interface consists of a serial data input signal (TAIDI), clock input signal (TAICI), and input framing signal (TAIFI). Data and the framing pulse are clocked in on rising edges of the clock, as shown in Figure 13.

Microprocessor Interface and RAM Blocks

The Microprocessor Interface block provides support of either an Intel-compatible or a Motorola-compatible formatted microprocessor bus interface, selectable by the MOTO control input pin. The memory of the SOT-3 device has 1024 8-bit register locations (addresses 000H through 3FFH). A memory map and a description of each location are provided in later sections of this Data Sheet.

The microprocessor interface consists of a 10-bit address input bus, an 8-bit bidirectional data bus, and various control and status pins, plus a RAM clock (RAMCI) input for operating the RAM. Read and write cycle timing for the Intel and Motorola interfaces is shown in Figures 14 -17. In addition, interrupt capability is provided by both a hardware interrupt (INT/$\overline{\text{IRQ}}$) pin and a software interrupt status register in memory. Each of the alarms in the SOT-3 device has one unlatched and one latched status bit in RAM associated with it, and a mask bit for disabling the software interrupt. The mask bit must be set to zero to disable the interrupt for the associated alarm. The latched status bits are located in latched registers, which latch on a positive alarm level and clear automatically when they are read, although the latched bits are maintained in the set condition for alarms which persist through the read cycle.

PIN DIAGRAM

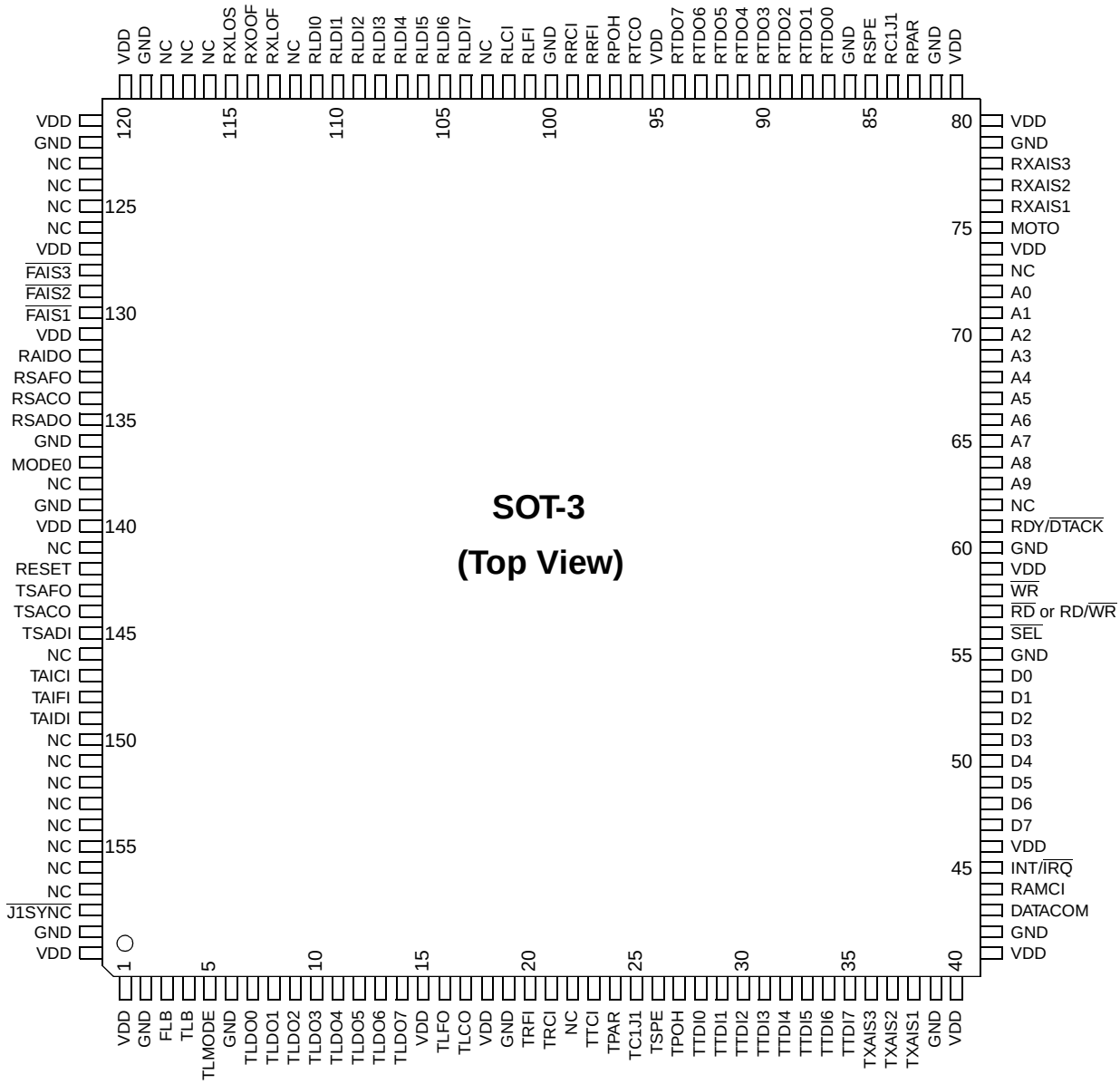


Figure 2. SOT-3 TXC-03003B Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY, GROUND AND NO CONNECT

Symbol	Pin No.	I/O/P *	Type	Name/Function
VDD	1,15,18,40,41,46,59, 74,80,81,95,120,121, 127,131,140,160	P		**VDD:** + 5 volt power supply, ± 5%. Nominal high level for signals.
GND	2,6,19,39,42,55,60, 79,82,86,100,119, 122,136,139,159	P		**Ground:** Zero volts reference. Nominal low level for signals.
NC	22,62,73,103, 112,116-118, 123-126, 138,141,146, 150-157			**No Connect:** NC pins are not to be connected, not even to another NC pin, but must be left floating. Connection of these pins may impair performance or cause damage to the device. (NC pins may have internal connections within the device. They may also be assigned functions in future versions of the device such that a connection would prevent backwards compatibility.)

* Note: I = Input; O = Output; P = Power

RECEIVE LINE SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type *	Name/Function
RLFI	101	I	CMOS	**Receive Line Frame In:** An active high framing pulse that occurs at the time of the third A2 byte of the STM-1/STS-3/STS-3c received data signal on RLDI.
RLCI	102	I	CMOS	**Receive Line Clock In:** This input clock has a nominal frequency of 19.44 MHz. Data (RLDI) and the framing signal (RLFI) are clocked in on the rising edges of this clock.
RLDI(7-0)	104-111	I	CMOS	**Receive Line Data In:** STM-1/STS-3/STS-3c byte-parallel data. The high level corresponds to logic 1. RLDI7 is defined as the most significant bit and the first bit received in the SDH/ SONET format.
RXLOF	113	I	TTL	**Receive Loss Of Frame In:** An external active high signal received from the SYN155 device or other line interface circuit that indicates a loss of frame alarm. The status of this alarm is conditionally recorded in status bit RLOF of the SOT-3 RAM.
RXOOF	114	I	TTL	**Receive Out Of Frame In:** An external active high signal received from the SYN155 device or other line interface circuit that indicates an out of frame alarm. The status of this alarm is conditionally recorded in status bit ROOF of the SOT-3 RAM.
RXLOS	115	I	TTL	**Receive Loss Of Signal In:** An external active high signal received from the SYN155 device or other line interface circuit that indicates a loss of signal. This signal is or-gated with the output of the internal SOT-3 circuit that detects loss of data input transitions to provide an alarm indication, which is recorded in status bit RLOS of the SOT-3 RAM.

* See Input, Output and I/O Parameters section below for Type Definitions.

RECEIVE REFERENCE TIMING

Symbol	Pin No.	I/O/P	Type	Name/Function
RRFI	98	I	CMOS	**Receive Reference Frame In:** An optional active high framing pulse reference, one RRCI cycle wide, that occurs every 125 microseconds. It can be used by the SOT-3 device to locate the receive terminal side frame timing. If it is not used, this pin must be set low. When it is not used, the pointer value will be arbitrary.
RRCI	99	I	CMOS	**Receive Reference Clock In:** A required clock input that has a nominal frequency of 19.44 MHz. Used for receive retiming, and for sourcing the receive terminal side output signals. The rising edge of RRCI is used for clocking in RRFI.

RECEIVE TERMINAL SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
RPAR	83	O	CMOS2mA	**Receive Terminal Parity:** Parity status bit that is calculated over the receive terminal side data RTDO(7-0), RSPE, and RC1J1 signals, for each RTCO clock cycle. Setting control bit TPLEV to 1 (0) selects even (odd) parity.
RC1J1	84	O	CMOS2mA	**Receive Terminal C1, J1 (and optional V1) Indications:** A composite synchronization signal which contains active high pulses in the location of the first C1 byte in the transport overhead and in the location(s) of the J1 byte(s) within the payload. The receive SPE indication (RSPE) is low during C1 and high during J1. For STM-1/STS-3c signals, there is one J1 pulse. For STS-3 signals, there are three J1 pulses, one for each STS-1. One or more V1 pulses may be present for asynchronous VT/TU mappings, and may be used in place of the H4 byte multiframe indication to determine the location of the V1 byte(s). Refer to Figure 22.
RSPE	85	O	CMOS2mA	**Receive Terminal SPE Indication:** RSPE is active high during STM-1 VC-4/STS-3c and STS-3:STS-1 SPE byte times (payload plus POH bytes, 261 byte times per subframe). This signal is low during the time that corresponds to the STM-1 section overhead and AU-4 pointer bytes and the STS-3 transport overhead bytes (nine byte times per subframe).

Symbol	Pin No.	I/O/P	Type	Name/Function
RTDO(7-0)	94-87	O	CMOS2mA	**Receive Terminal Data Out:** Byte-parallel data output for the STM-1 AU-4/STS-3c and STS-3 frames. Data is clocked out on the falling edge of the Receive Terminal Clock Out (RTCO). Data bytes are present for the A1, A2, three E1s, three H1s and H2s, H4 during VTAIS/ TUAIS, and 261 STM-1 VC-4 or STS-3/STS-3c SPE byte times. During other byte times, the data bytes are set equal to zero. The high level corresponds to logic 1. RTDO7 is defined as the most significant bit and is the first bit received.
RTCO	96	O	CMOS2mA	**Receive Terminal Clock Out:** Output clock, derived from RRCI, that has a nominal frequency of 19.44 MHz. Its falling edges are used for clocking out the byte-parallel data after retiming, and the RC1J1, RSPE, and RPAR signals.
RPOH	97	O	CMOS2mA	**Receive Terminal Path Overhead Bytes Indication:** RPOH is high during STM-1 VC-4/STS-3c and STS-3 path overhead byte times. For STM-1/STS-3c signals, RPOH will be high for one byte per subframe. For STS-3 signals, RPOH will be high for three bytes per subframe, one for each STS-1. RPOH is low at other times.

TRANSMIT TERMINAL SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
TTCI	23	I/O	CMOS2mA	**Transmit Terminal Clock In:** Transmit STM-1/STS-3 byte rate clock that has a nominal frequency of 19.44 MHz. In normal operation, byte-parallel data TTDI(7-0) and the TPAR, TC1J1 and TSPE input signals are clocked into the SOT-3 device on the rising edges of this clock. In the data communication and source timing modes, this clock becomes an output clock and is used for sourcing data (TTDI) and parity (TPAR) into the SOT-3 device on its falling edges, which are also used for clocking out TC1J1, TSPE and TPOH.
TPAR	24	I	CMOS	**Transmit Terminal Parity Input:** Parity input bit in which even (or odd) parity has been calculated over the transmit data byte (TTDI), TSPE, and TC1J1 signals in combination (or over the data byte alone) for each TTCI clock cycle. The SOT-3 device may be set up to compare this input value with a corresponding internally generated value. Even (odd) parity is calculated if control bit TPLEV is set to 1 (0). Parity is calculated for the 3-signal combination (data only) if control bit PDAT is set to 0 (1). If the comparison does not match, the BERR alarm bit is set. The TPAR input is ignored in the data communication and source timing modes.

Symbol	Pin No.	I/O/P	Type	Name/Function
TC1J1	25	I/O	TTL2mA	**Transmit Terminal C1, J1 (and optional V1) Indications:** In the normal mode, this is an input synchronization signal which contains active high pulses in the location of the first C1 byte in the transport overhead and in the location(s) of the J1 byte(s) within the payload. The transmit SPE indication (TSPE) must be low during C1 and high during J1. For STM-1/STS-3c signals, there is one J1 pulse. For STS-3 signals, there are three J1 pulses, one for each STS-1. One or more V1 pulses may be present for asynchronous VT/TU mappings, to determine the starting location of the V1 byte(s). In the data communication and source timing modes, this signal becomes an output.
TSPE	26	I/O	TTL2mA	**Transmit Terminal SPE Indication:** In the normal mode, TSPE is an active high input signal that occurs during the STM-1 VC-4/STS-3c or STS-3:STS-1 SPE byte times (261 byte times per row.) It is low during the time that corresponds to the STM-1 section overhead and AU pointer bytes and the STS-3/STS-3c transport overhead bytes (nine byte times per row). In the source timing and data communication modes, when the MODE0 pin is tied low, this signal becomes an output. In the data communication mode, which is intended for STM-1 VC-4/STS-3c operation, when MODE0 is tied high, the TSPE pin is low for the first 10 byte times per “row” of each STM-1/STS-3c frame, and high for the remaining 260 byte time slots of the row. When MODE0 is tied low, the TSPE signal is low for the first 12 byte time slots per “row” of the STM-1/STS-3c frame, and high for the remaining 258 byte time slots of the row. In the source timing mode of operation, the TSPE signal is low for the first nine byte time slots of each “row” of the frame, and high for the remaining 261 byte time slots of the frame.
TPOH	27	O	CMOS2mA	**Transmit Terminal Path Overhead Bytes Indication:** This signal is high during STM-1 VC-4/STS-3c path overhead byte times in the source timing and data communication modes.
TTDI(7-0)	35-28	I	CMOS	**Transmit Terminal Data In:** Byte-parallel data input for the STM-1 AU-4/STS-3c and STS-3 frames. The E1 bytes carrying an AIS indication are optional. No other TOH bytes are required. The path overhead bytes may accompany the payload. The high level corresponds to logic 1. TTDI7 is defined as the most significant bit and is the first bit transmitted.

TRANSMIT REFERENCE TIMING

Symbol	Pin No.	I/O/P	Type	Name/Function
TRFI	20	I	CMOS	**Transmit Reference Frame In:** An optional reference framing pulse input that the SOT-3 uses to locate the transmit line side frame timing. When used, it is active for one TRCI clock cycle every 125 microseconds. When not used, it must be set to the inactive level of the signal, which is controlled by TLMODE (pin 5), as follows: When TLMODE is low, set TRFI high. When TLMODE is high, set TRFI low When it is not used, the pointer value will be arbitrary.
TRCI	21	I	CMOS	**Transmit Reference Clock In:** A required clock input that has a nominal frequency of 19.44 MHz. Used for transmit retiming and for sourcing the transmit data (TLDO) and clock out (TLCO) signals. The optional framing pulse (TRFI) is clocked in on the rising (falling) edge of TRCI when TLMODE (pin 5) is high (low).

TRANSMIT LINE SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
TLDO(7-0)	14-7	O	CMOS2mA	**Transmit Line Data Out:** STM-1/STS-3/STS-3c byte-parallel data. Data is clocked out on the falling edge of the transmit line clock out (TLCO) if TLMODE (pin 5) is high. Otherwise, it is clocked out on the rising edge. The high level corresponds to logic 1. TLDO7 is defined as the most significant bit and is the first bit transmitted.
TLFO	16	O	CMOS2mA	**Transmit Line Frame Out:** An active high (low) framing pulse, one TLCO clock cycle wide, that occurs during the third A2 byte time of the transmitted data (TLDO), when TLMODE (pin 5) is set high (low).
TLCO	17	O	CMOS2mA	**Transmit Line Clock Out:** When TLMODE (pin 5) is set high (low), the byte-parallel data (TLDO) and the active high (low) framing signal (TLFO) are clocked out on falling (rising) edges of this TLCO clock, which is derived from TRCI after retiming.

TRANSPORT OVERHEAD BYTE (TOH) SERIAL ACCESS PORT INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
RSAFO	133	O	TTL4mA	**Receive TOH Serial Access Port Frame Out:** An active high framing pulse, one RSACO clock cycle wide, that identifies the most significant bit in the C1 byte of the RSADO serial data stream. This framing pulse is also used to identify the location of the first bit in the 40-bit serial format of the Receive Alarm Indication Port Data Out (RAIDO) signal.
RSACO	134	O	TTL4mA	**Receive TOH Serial Access Port Clock Out:** A gapped clock which has an average rate of 5.184 MHz. The clock is generated by dividing the RLCI input clock by three, and the gap is one clock cycle out of every five cycles. Serial data (RSADO) and a framing signal (RSAFO) are clocked out on the falling edge of this clock (see the timing diagram in Figure 10). The first 40 pulses of this clock in each frame are also used to clock out the Receive Alarm Indication Port Data Out signal (RAIDO) and its framing signal (RSAFO).
RSADO	135	O	TTL4mA	**Receive TOH Serial Access Port Data Out:** Serial bit stream that carries the contents of the receive line side Section Overhead bytes plus the AU-4 pointer in an STM-1 signal or the 81 Transport Overhead bytes in an STS-3/STS-3c frame. The high level corresponds to logic 1.
TSAFO	143	O	TTL4mA	**Transmit TOH Serial Access Port Frame Out:** An active high framing pulse, one TSACO clock cycle wide, that identifies the most significant bit (MSB) of the C1 byte in the TSADI serial data stream. Used for identifying the starting location of the 81 overhead bytes to be accepted into the SOT-3.
TSACO	144	O	TTL4mA	**Transmit TOH Serial Access Port Clock Out:** A gapped output clock which has an average rate of 5.184 MHz. The clock is generated by dividing the TRCI input clock by three, and the gap is one clock cycle for every five cycles. Serial data (TSADI) and a framing signal (TSAFO) are clocked in on the rising edge of this clock. Refer to the timing diagram in Figure 11.
TSADI	145	I	TTL	**Transmit TOH Serial Access Port Data In:** A serial bit stream that carries the contents of the transmit line side Section Overhead bytes plus the AU-4 pointer in the STM-1 format or the 81 Transport Overhead bytes in an STS-3c/STS-3 frame. The high level corresponds to logic 1.

ALARM INDICATION PORT INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
RAIDO	132	O	TTL	**Receive Alarm Indication Port Data Out:** A serial bit stream output that provides the status of receive alarms. It is normally connected to the TAIDI input of the mate SOT-3 device in ring applications. The data format is a serial stream of 40 bits that is transmitted once per frame, as described in Figure 25 (Operation section). The values present on this pin during the remaining 41 clock times of the frame are not defined. The high level corresponds to logic 1. This signal is clocked out on the falling edges of the Receive TOH Serial Access Port Clock Out signal (RSACO). The Receive TOH Serial Access Port Frame Out signal (RSAFO) indicates the position of the most significant bit (bit 39).
TAICI	147	I	TTL	**Transmit Alarm Indication Port Clock In:** Normally connected to the Receive TOH Serial Access Port Clock Out signal (RSACO) of the other SOT-3 device in a ring configuration. This is a gapped clock which has an average rate of 5.184 MHz. Data (TAIDI) and the framing signal (TAIFI) are clocked into the SOT-3 on the rising edges of this clock. TAICI is not monitored for loss of clock.
TAIFI	148	I	TTL	**Transmit Alarm Indication Port Frame In:** Normally connected to the Receive TOH Serial Access Port Frame Out signal (RSAFO) pin of the mate SOT-3 device in a ring configuration. An active high framing pulse, one TAICI clock cycle wide, which identifies the first bit (No. 39) of the Alarm Indication Port data input stream at TAIDI.
TAIDI	149	I	TTL	**Transmit Alarm Indication Port Data In:** Normally connected to the Receive Alarm Indication Port Data Out signal (RAIDO) pin of the mate SOT-3 device when two devices are used together in a ring configuration. The input alarm indications in the serial bit stream (see Figure 25 in the Operation section) are used to generate line and path RDI and FEBE alarm indications, and APS information, in the transmitted STM-1/STS-3 line signal. The alarm indications are clocked into the SOT-3 device on the rising edges of the input clock (TAICI). The high level corresponds to logic 1.

MICROPROCESSOR BUS INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
RAMCI	44	I	CMOS	**RAM Clock Input:** Asynchronous clock input used for internal RAM functions. This clock may be connected to the microprocessor clock. Requires clock rate of 16-20 MHz and duty cycle of 45-55%.
INT/$\overline{\text{IRQ}}$	45	O	TTL4mA	**Interrupt:** Intel mode (INT): A high on this output pin signals an interrupt request to the microprocessor. Motorola mode ($\overline{\text{IRQ}}$): A low on this output pin signals an interrupt request to the microprocessor.
D(7-0)	47-54	I/O	TTL8mA	**Data Bus:** These bidirectional data lines are used for transferring data between the SOT-3 RAM and the microprocessor. The high level corresponds to logic 1. D7 is defined as the most significant bit.
$\overline{\text{SEL}}$	56	I	TTLp	**Select:** A low enables data transfers between the microprocessor and SOT-3 RAM during a read or write cycle.
$\overline{\text{RD}}$ or RD/$\overline{\text{WR}}$	57	I	TTL	**Read or Read/Write:** Intel mode ($\overline{\text{RD}}$): An active low signal generated by the microprocessor for reading the SOT-3 RAM. Motorola mode (RD/$\overline{\text{WR}}$): An active high signal generated by the microprocessor for reading the SOT-3 RAM. A low is used to write to SOT-3 RAM locations.
$\overline{\text{WR}}$	58	I	TTL	**Write:** Intel mode: An active low signal generated by the microprocessor for writing to SOT-3 RAM. Motorola mode: Not used, left floating.
MOTO	75	I	TTL	**Motorola/Intel Processor Select:** A high selects a Motorola microprocessor compatible bus interface. A low selects an Intel microprocessor compatible bus interface.
RDY/ $\overline{\text{DTACK}}$	61	O (tri-state)	TTL8mA	**Ready or Data Transfer Acknowledge:** Intel mode (RDY): A high is an acknowledgment from the addressed RAM location that the transfer can be completed. A low indicates the SOT-3 cannot complete the transfer cycle, and that microprocessor wait states must be generated. Motorola mode ($\overline{\text{DTACK}}$): During a read cycle, a low signal indicates the information on the data bus is valid. During a write cycle, a low signal acknowledges the acceptance of data.
A(9-0)	63-72	I	TTL	**Address Bus:** These address line inputs are used by the microprocessor to select a SOT-3 RAM location for a read/write data transfer when the Select lead is low. The high level corresponds to logic 1. A9 is defined as the most significant bit.

CONTROLS

Symbol	Pin No.	I/O/P	Type	Name/Function
FLB	3	O	TTL4mA	**Facility Loopback Control Out:** An active high control signal provided by the SOT-3 device, when control bit FLB is set to 1 by the microprocessor, for enabling the facility loopback feature in the SYN155 (TXC-02301B) or other line interface circuit.
TLB	4	O	TTL4mA	**Terminal Loopback Control Out:** An active high control signal provided by the SOT-3 device, when control bit TLB is set to 1 by the microprocessor, for enabling the terminal loopback feature in the SYN155 (TXC-02301B) or other line interface circuit.
TLMODE	5	I	TTLp	**Transmit Line Interface Invert Control:** A high causes the Transmit Line Frame Out (TLFO) signal to be active high. This framing signal and data (TLDO(7-0)) will be clocked out on falling edges of the transmit line clock (TLCO). The Transmit Reference Frame In (TRFI) must be an active high indication. A low causes the Transmit Line Frame Out (TLFO) signal to be active low. The framing signal and data (TLDO(7-0)) will be clocked out on rising edges of the transmit line clock (TLCO). The Transmit Reference Frame In (TRFI) must be an active low indication. See Figures 4 and 5 for timing diagrams of operation with TLMODE (pin 5) set high and low.
DATACOM	43	I	TTL	**Data Communication Mode:** An active high select for the data communication (datacom) and source timing modes of operation. When high, datacom (source timing) mode is selected when control bit STIME is set to 0 (1). In the transmit direction, the SOT-3 device provides the transmit clock (TTCI), C1J1 and SPE as output signals, together with the POH output, for sourcing terminal data (TTDI) into the SOT-3 device.
$\overline{\text{FAIS1}}$	130	I	TTLp	**Generate Receive Path AIS and Transmit an RDI Indication for STM-1 AU-4/STS-3c or STS-3:STS-1 No. 1**: An active low input for controlling the generation of path AIS and Transmit RDI (when not in the RING mode) for STM-1 AU-4/STS-3c or STS-3:STS-1 No. 1. When this pin is not used it should held high. It should be noted that activation of this input may cause erratic J1 pulse and pointer movements.

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{FAIS2}}$	129	I	TTLp	**Generate Receive Path AIS and Transmit an RDI Indication for STS-3:STS-1 No. 2:** An active low input for controlling the generation of path AIS and Transmit RDI (when not in the RING mode) for STS-3 STS-1 No. 2. When this pin is not used it should held high. It should be noted that activation of this input may cause erratic J1 pulse and pointer movements.
$\overline{\text{FAIS3}}$	128	I	TTLp	**Generate Receive Path AIS and Transmit an RDI Indication for STS-3:STS-1 No. 3:** An active low input for controlling the generation of path AIS and Transmit RDI (when not in the RING mode) for STS-3 STS-1 No. 3. When this pin is not used it should held high. It should be noted that activation of this input may cause erratic J1 pulse and pointer movements.
MODE0	137	I	TTLp	**Mode Control**: A low is normally applied to this pin, to enable the full set of features and performance characteristics described in this Data Sheet. If this pin is instead tied high or left floating, the device emulates the features and performance characteristics of the predecessor SOT-3 device, Part Number TXC-03003-AIPQ, which are described in its Data Sheet, document number TXC-03003-MB.
$\overline{\text{J1SYNC}}$	158	I	TTLp	**J1 Byte Optional Synchronize Pulse:** When an active low pulse having a minimum duration of one clock cycle at 19.44 MHz is applied to this pin the starting locations of the three transmit path overhead RAM segment addresses J11, J12 and J13 are reset to 1C0H, 200H and 240H, respectively. The next J1 byte transmitted for a STM-1/STS-3c or for one of the three STS-3:STS-1 signals will start at the appropriate one of these three address locations.
RESET	142	I	TTL	**SOT-3 Reset:** An active high signal which resets the FIFOs, performance counters and parity counters to preset values. The transmit pointer generation and access ports are also reset. The receive pointer tracking state machine is set to path AIS state. Control bits and RAM locations are not affected. RESET must be used at power-up, after the power supply and all four input clocks are stable. The signal must be held high for a minimum duration of six 19.44 MHz clock cycles.

AIS INDICATIONS AND CONTROLS

Symbol	Pin No.	I/O/P	Type	Name/Function
RXAIS1	76	O	TTL4mA	**Receive AIS Indication for STM-1 AU-4/STS-3c or STS-3:STS-1 No. 1:** Active high output indication for the alarms that cause a receive VT or path AIS for STM-1 AU-4/STS-3c or STS-3:STS-1 No. 1. See Note 1.
RXAIS2	77	O	TTL4mA	**Receive AIS Indication for STS-3:STS-1 No. 2:** Active high output indication for the alarms that cause a receive VT or path AIS for STS-3:STS-1 No. 2. See Note 1.
RXAIS3	78	O	TTL4mA	**Receive AIS Indication for STS-3:STS-1 No. 3:** Active high output indication for the alarms that cause a receive VT or path AIS for STS-3:STS-1 No. 3. See Note 1.
TXAIS1	38	I	TTL	**Transmit AIS Control for STM-1 AU-4/STS-3c or STS-3:STS-1 No. 1:** Active high input that generates a line or path AIS for STM-1 AU-4/STS-3c or STS-1 No. 1 of STS-3, conditional on bit 2 and bit 0 at Address 3E0H. When bit 2 (TRPAISE) is 1, a Path AIS is generated. When bit 0 (TRLAISE) is 1, a Line AIS is generated.
TXAIS2	37	I	TTL	**Transmit AIS Control for STS-3:STS-1 No. 2:** Active high input that generates path AIS for STS-1 No. 2 of STS-3 (similar to TXAIS1, above). When high, with TRPAISE set to 1, path AIS is generated.
TXAIS3	36	I	TTL	**Transmit AIS Control for STS-3:STS-1 No. 3:** Active high input that generates AIS for STS-1 No. 3 of STS-3 (similar to TXAIS1, above). When high, with TRPAISE set to 1, path AIS is generated.

Note 1: See Figures 18 and 19 for description of conditions which cause a receive VT or path AIS and activate pin RXAISn, where n=1-3.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+7.0	V	Note 1
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	Note 1
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient operating temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Component Temperature x Time	TI		270 x 5	^oC x s	Note 1
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD		±2000	V	per MIL-STD-883D Method 3015.7

Notes:

1. Operating conditions outside the min-max ranges specified may cause permanent device failure. Exposure to conditions near the min or max limits for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient			41.4	$^oC/W$	0 ft/min airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}	133	167	200	mA	See Note 1.
P_{DD}	656	835	1050	mW	See Note 1.

Note 1: With inputs switching and V_{DD} / output load of 5.0 V / 0 pF for Min, 5.0 V / 25 pF for Typ and 5.25 V / 50 pF for Max.

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

INPUT PARAMETERS FOR CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	0.7 x V_{DD}			V	4.75 ≤ V_{DD} ≤ 5.25
V_{IL}			0.2 x V_{DD}	V	4.75 ≤ V_{DD} ≤ 5.25
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		3.5		pF	

INPUT PARAMETERS FOR TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 ≤ V_{DD} ≤ 5.25
V_{IL}			0.8	V	4.75 ≤ V_{DD} ≤ 5.25
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		3.5		pF	

INPUT PARAMETERS FOR TTLP

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 ≤ V_{DD} ≤ 5.25
V_{IL}			0.8	V	4.75 ≤ V_{DD} ≤ 5.25
Input leakage current		0.5	1.4	mA	V_{DD} = 5.25; Input = 0 volts
Input capacitance		3.5		pF	

Note: Input has a 9k (nominal) internal pull-up resistor.

INPUT/OUTPUT PARAMETERS FOR CMOS2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	0.7 x V_{DD}			V	4.75 ≤ V_{DD} ≤ 5.25
V_{IL}			0.2 x V_{DD}	V	4.75 ≤ V_{DD} ≤ 5.25
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		3.5		pF	
V_{OH}	V_{DD} - 0.8			V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			0.5	V	V_{DD} = 4.75; I_{OL} = 2.0
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.5	5.5	9.9	ns	C_{LOAD} = 15pF
t_{FALL}	2.0	3.9	8.0	ns	C_{LOAD} = 15pF

INPUT/OUTPUT PARAMETERS FOR TTL2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	
V_{OH}	V_{DD} - 0.8			V	$V_{DD} = 4.75$; $I_{OH} = -2.0$
V_{OL}			0.5	V	$V_{DD} = 4.75$; $I_{OL} = 2.0$
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.5	5.5	9.9	ns	$C_{LOAD} = 15pF$
t_{FALL}	2.0	3.9	8.0	ns	$C_{LOAD} = 15pF$

INPUT/OUTPUT PARAMETERS FOR TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	mA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	
V_{OH}	V_{DD} - 0.8			V	$V_{DD} = 4.75$; $I_{OH} = -4.0$
V_{OL}			0.5	V	$V_{DD} = 4.75$; $I_{OL} = 8.0$
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	1.9	4.5	8.0	ns	$C_{LOAD} = 25pF$
t_{FALL}	0.8	1.5	3.1	ns	$C_{LOAD} = 25pF$

OUTPUT PARAMETERS FOR CMOS2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.8			V	$V_{DD} = 4.75$; $I_{OH} = -2.0$
V_{OL}			0.5	V	$V_{DD} = 4.75$; $I_{OL} = 2.0$
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.5	5.5	9.9	ns	$C_{LOAD} = 15pF$
t_{FALL}	2.0	3.9	8.0	ns	$C_{LOAD} = 15pF$

OUTPUT PARAMETERS FOR TTL4mA

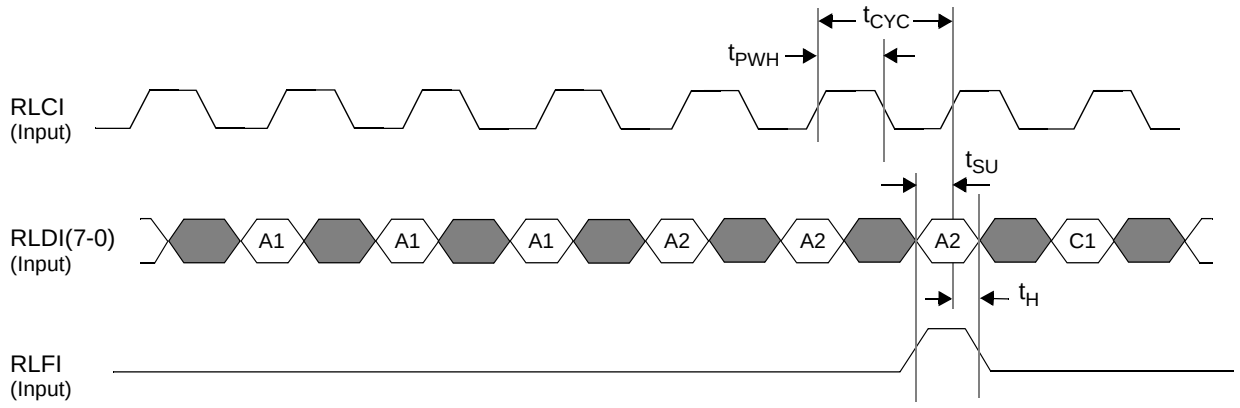
Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.8			V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			0.5	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.5	5.5	10.0	ns	C_{LOAD} = 15pF
t_{FALL}	1.0	2.0	4.0	ns	C_{LOAD} = 15pF

TIMING CHARACTERISTICS

Detailed timing diagrams for the SOT-3 device are illustrated in Figures 3 through 17, with values of the timing intervals following each figure. All output times are measured with a maximum 25 pF load capacitance. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals.

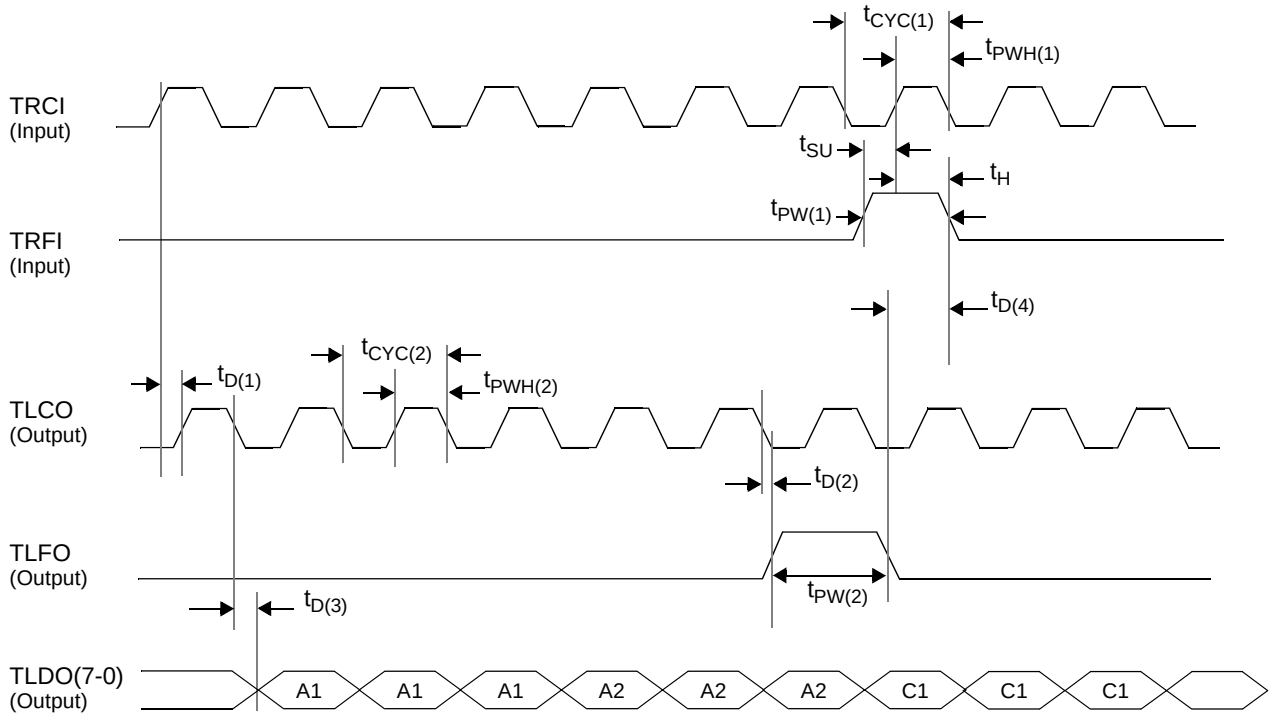
Overhead byte designations shown in the timing diagrams for data bus signals are intended only as timing references for the STM-1/STS-3/STS-3c frame and should not be interpreted as having any particular value. For example, in Figure 3, the pulse on the RLFI input should occur at the same time as the A2-3 byte on the RLDI(7-0) data bus.

Figure 3. Line Side Receive Timing



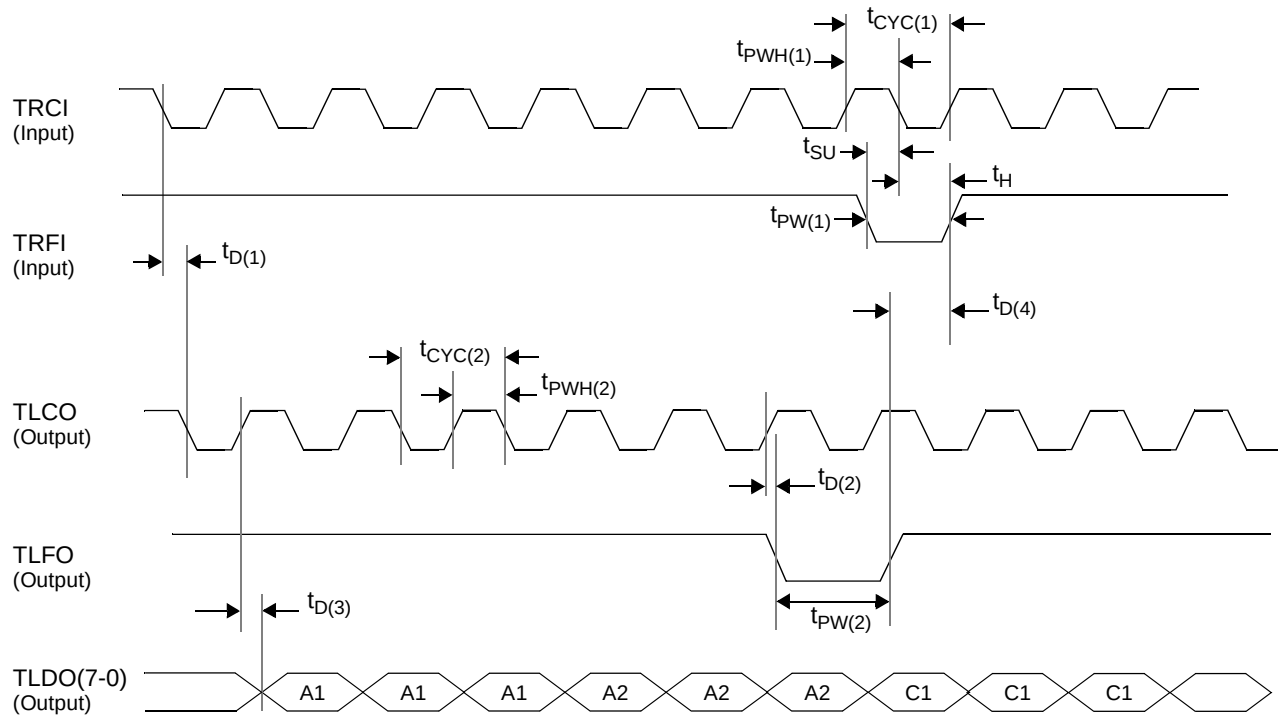
Parameter	Symbol	Min	Typ	Max	Unit
RLCI clock period	t_{CYC}	50	51.44		ns
RLCI duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
RLDI and RLFI set-up time to RLCI↑	t_{SU}	7.0			ns
RLDI and RLFI hold time after RLCI↑	t_H	3.0			ns

Figure 4. Line Side Transmit Timing with TLMODE (Pin 5) Tied High



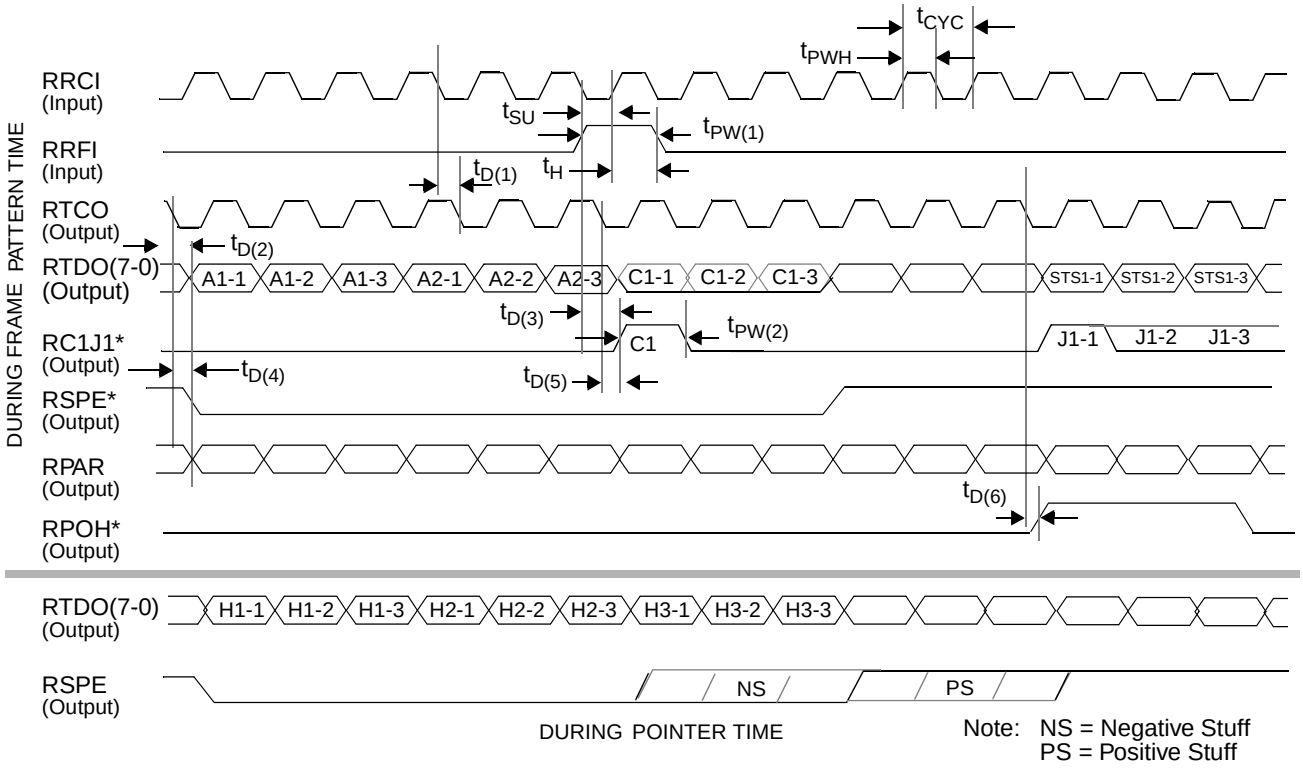
Parameter	Symbol	Min	Typ	Max	Unit
TRCI clock period	$t_{CYC(1)}$	50	51.44		ns
TRCI duty cycle ($t_{PWH(1)}/t_{CYC(1)}$)	--	45		55	%
TRFI set-up time to TRCI↑	t_{SU}	7.0			ns
TRFI hold time after TRCI↑	t_H	3.0			ns
TLCO↑ delay after TRCI↑	$t_{D(1)}$	6.0	15	30	ns
TLFO↑ delay after TLCO↓	$t_{D(2)}$	-2.0	0.0	5.0	ns
TLDO delay after TLCO↓	$t_{D(3)}$	-2.0	0.0	5.0	ns
TRFI pulse width	$t_{PW(1)}$	40			ns
TLFO pulse width	$t_{PW(2)}$	40	$t_{CYC(1)}$ Typ		ns
TLCO duty cycle ($t_{PWH(2)}/t_{CYC(2)}$)	--	45		55	%
TLFO↓ lead before TRFI↓	$t_{D(4)}$	20	$t_{CYC(1)}$ Typ		ns

Figure 5. Line Side Transmit Timing with TLMODE (Pin 5) Tied Low



Parameter	Symbol	Min	Typ	Max	Unit
TRCI clock period	$t_{CYC(1)}$	50	51.44		ns
TRCI duty cycle ($t_{PWH(1)}/t_{CYC(1)}$)	--	45		55	%
TRFI set-up time to TRCI↓	t_{SU}	7.0			ns
TRFI hold time after TRCI↓	t_H	3.0			ns
TLCO↓ delay after TRCI↓	$t_{D(1)}$	6.0	15	30	ns
TLFO↓ delay after TLCO↑	$t_{D(2)}$	-2.0	0.0	5.0	ns
TLDO delay after TLCO↑	$t_{D(3)}$	-2.0	0.0	5.0	ns
TRFI pulse width	$t_{PW(1)}$	40			ns
TLFO pulse width	$t_{PW(2)}$	40	$t_{CYC(1)}$ Typ		ns
TLCO duty cycle ($t_{PWH(2)}/t_{CYC(2)}$)	--	45		55	%
TLFO↑ lead before TRFI↑	$t_{D(4)}$	40	$t_{CYC(1)}$ Typ		ns

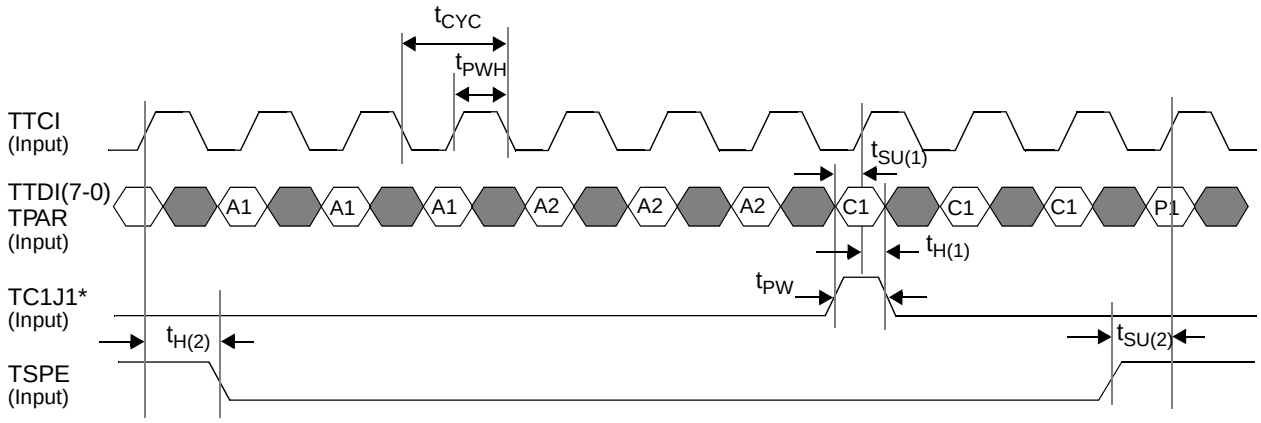
Figure 6. Terminal Side Receive Timing



Parameter	Symbol	Min	Typ	Max	Unit
RRCI clock period	t_{CYC}	50	51.44		ns
RRCI duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
RRFI set-up time to RRCI↑	t_{SU}	7.0			ns
RRFI hold time after RRCI↑	t_H	3.0			ns
RTCO↓ delay after RRCI↓	$t_{D(1)}$	6.0	15	30	ns
RTDO delay after RTCO↓	$t_{D(2)}$	-2.0	0.0	5.0	ns
RC1J1 C1 pulse delay after RRFI↑	$t_{D(3)}$	0	15	40	ns
RSPE, RPAR delay after RTCO↓	$t_{D(4)}$	-2.0	0.0	5.0	ns
RC1J1 C1 pulse delay after RTCO↓	$t_{D(5)}$	-2.0	0.0	5.0	ns
RPOH delay after RTCO↓	$t_{D(6)}$	-2.0	0.0	5.0	ns
RRFI pulse width	$t_{PW(1)}$	40			ns
RC1J1 C1 pulse width	$t_{PW(2)}$	40	t_{CYC} Typ	3 x t_{CYC}	ns

*Note: The location of the J1, SPE and POH indications will change with the pointer value(s). In the STM-1 or STS-3c mode, there will be a single J1 pulse. In the STS-3 mode, there will be three J1 locations, one for each STS-1. If the pointer values of 2 or 3 of the STS-1s are the same, the NRZ character of the STS-3 output causes the adjacent pulses to be a single entity as illustrated by the dotted line in the RC1J1 waveform above. The pointer value illustrated is 523 (Decimal). If the pointer values of the three STS-1s are different the STS-3 output will be RZ, yielding three J1 pulses.

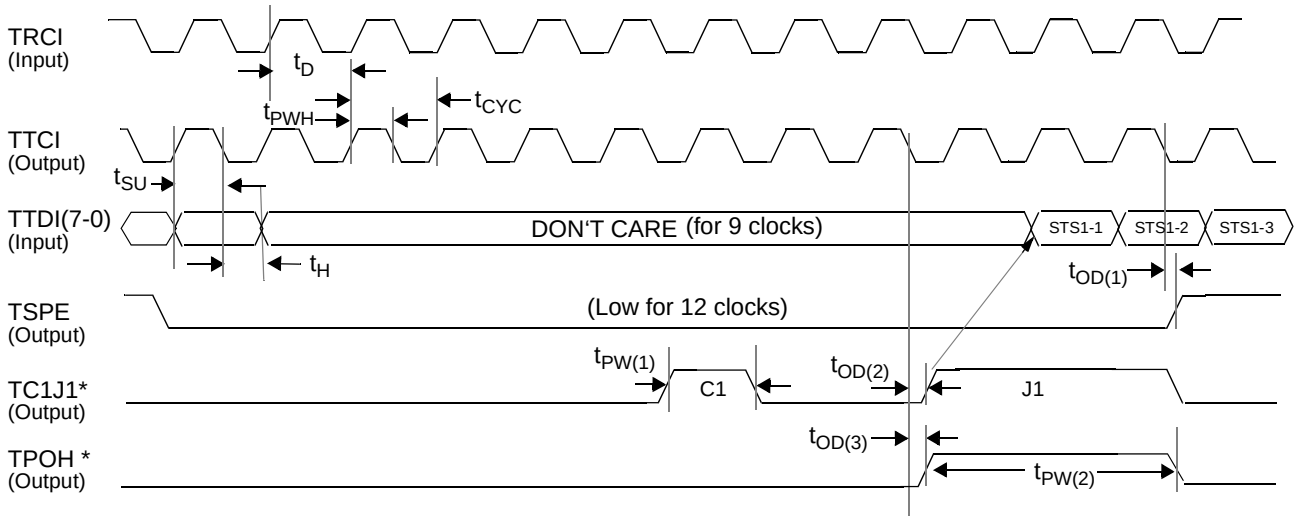
Figure 7. Terminal Side Transmit Timing in Normal Mode



Parameter	Symbol	Min	Typ	Max	Unit
TTCI clock period	t_{CYC}	50	51.44		ns
TTCI duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
TTDI/TPAR/TC1J1 set-up time to TTCI↑	$t_{SU(1)}$	7.0			ns
TTDI/TPAR/TC1J1 hold time after TTCI↑	$t_{H(1)}$	6.0			ns
TC1J1 pulse width	t_{PW}	40			ns
TSPE set-up time to TTCI↑	$t_{SU(2)}$	7.0			ns
TSPE hold time after TTCI↑	$t_{H(2)}$	6.0			ns

* Note: The signal TC1J1 is shown going active during the C1 time for the first STS-1 of the STS-3 signal. The signal is also active for the J1 byte (3 J1's in an STS-3 signal) and for V1 byte(s) if so configured. C1 signals occur once per frame, and J1 signals occur once per frame per STS (once in STS-3c or STM-1 mode, or 3 times in STS-3 mode.) The V1 pulse(s) occur once every four frames when enabled, depending on the VT/TU mappings.

Figure 8. Terminal Side Transmit Timing in Data Communication Mode

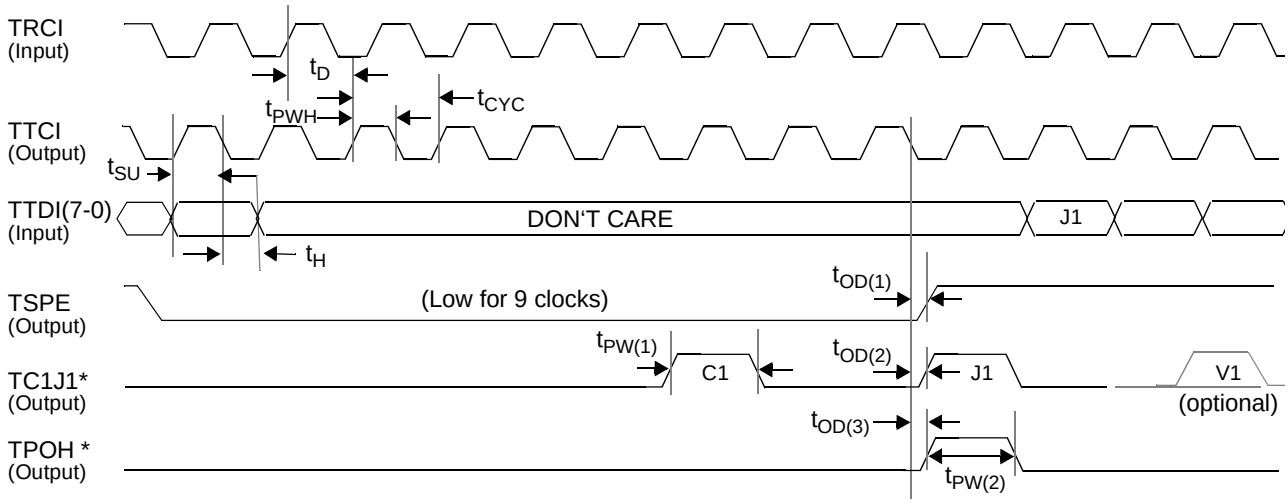


Note: Diagram assumes INVCI is set to zero. INVCI equal to one would cause the TTDI(7-0) data to be clocked in on the rising edge of TTCI, instead of on the falling edge as shown here. The TSPE, TC1J1 and TPOH outputs all have transitions on the falling edge of TTCI regardless of the state of INVCI. The arrows are used to clarify the relationship between the output J1 signal and the input J1 byte (C1 pulse also leads the input C1 time by one clock period). The extended TPOH and J1 pulses occur because the payload is STS-3c in data communication mode, but there are three POH columns.

Parameter	Symbol	Min	Typ	Max	Unit
TTCI↑ clock delay after TRCI↑	t_D	35		46	ns
TTCI clock period	t_{CYC}	50	51.44		ns
TTCI duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
TTDI set-up time to TTCI↓	t_{SU}	12			ns
TTDI hold time after TTCI↓	t_H	0.0			ns
TC1J1 pulse width	$t_{PW(1)}$	40	t_{CYC} Typ	3 x t_{CYC}	ns
TPOH pulse width	$t_{PW(2)}$	40	t_{CYC} Typ	3 x t_{CYC}	ns
TSPE output delay after TTCI↓	$t_{OD(1)}$	-2.0	0.0	5.0	ns
TC1J1 output delay after TTCI↓	$t_{OD(2)}$	-2.0	0.0	5.0	ns
TPOH output delay after TTCI↓	$t_{OD(3)}$	-2.0	0.0	5.0	ns

* Note: TPOH occurs every subframe during the transport path overhead byte time, and J1 occurs once per frame.

Figure 9. Terminal Side Transmit Timing in Source Timing Mode

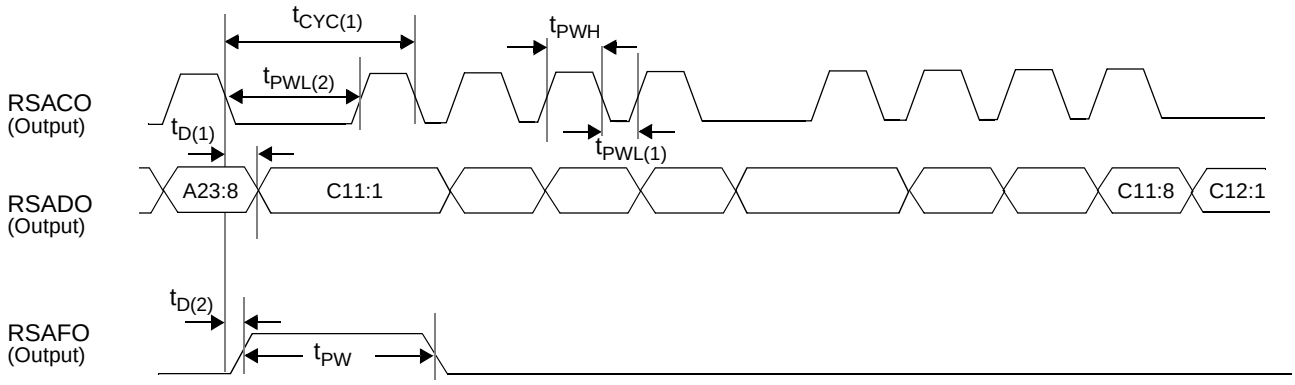


Note: Diagram assumes INVCI is set to zero. INVCI equal to one would cause the TTDI(7-0) data to be clocked in on the rising edge of TTCI, instead of on the falling edge as shown here. The TSPE, TC1J1 and TPOH outputs all have transitions on the falling edge of TTCI regardless of the state of INVCI.

Parameter	Symbol	Min	Typ	Max	Unit
TTCI↑ clock delay after TRCI↑	t_D	35		46	ns
TTCI clock period	t_{CYC}	50	51.44		ns
TTCI duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
TTDI set-up time to TTCI↓	t_{SU}	12			ns
TTDI hold time after TTCI↓	t_H	0.0			ns
TC1J1 pulse width	$t_{PW(1)}$	40	t_{CYC} Typ	3 x t_{CYC}	ns
TPOH pulse width	$t_{PW(2)}$	40	t_{CYC} Typ	3 x t_{CYC}	ns
TSPE output delay after TTCI↓	$t_{OD(1)}$	-2.0	0.0	5.0	ns
TC1J1 output delay after TTCI↓	$t_{OD(2)}$	-2.0	0.0	5.0	ns
TPOH output delay after TTCI↓	$t_{OD(3)}$	-2.0	0.0	5.0	ns

* Note 1: TPOH occurs every subframe during the transport path overhead byte time, and J1 occurs once per frame. V1, if enabled, occurs once every four frames to establish multiframe timing.

Figure 10. TOH Serial Access Port Receive Timing



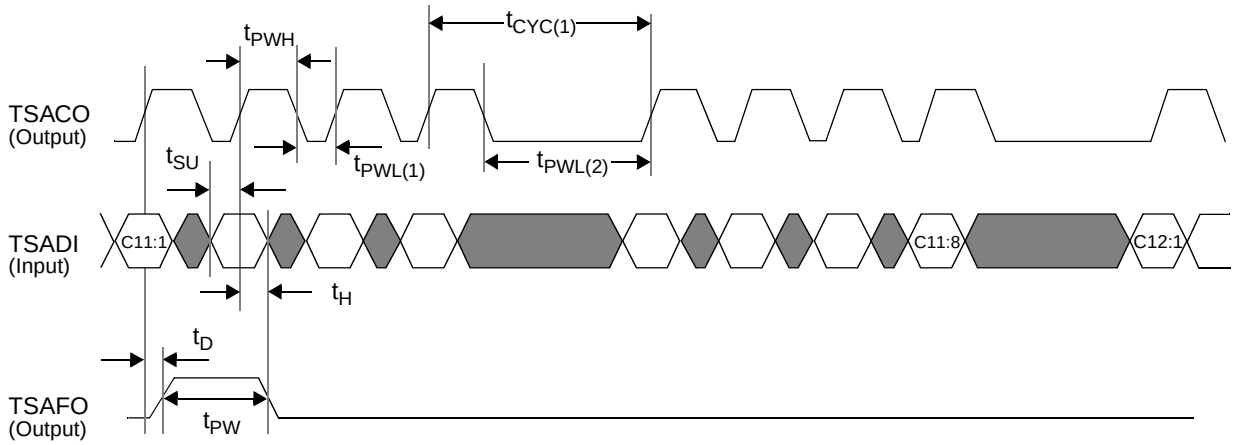
Parameter	Symbol	Min	Typ	Max	Unit
RSACO clock period	$t_{CYC(1)}$	3 x t_{CYC}*	**	6 x t_{CYC}*	ns
RSACO high time	t_{PWH}		2 x t_{CYC}*		ns
RSACO low time (non-gap time)	$t_{PWL(1)}$		1 x t_{CYC}*		ns
RSACO low time (gap time)	$t_{PWL(2)}$		4 x t_{CYC}*		ns
RSADO delay after RSACO↓	$t_{D(1)}$	-2.0	0.0	5.0	ns
RSAFO delay after RSACO↓	$t_{D(2)}$	-2.0	0.0	5.0	ns
RSAFO pulse width	t_{PW}		6 x t_{CYC}*		ns

*t_{CYC} is equal to one RLCI clock period (51.44 ns, nominal).

**Long term average RSACO clock period is 5/4(t_{CYC} x 3), or 192.9 ns, nominal.

Note: The RSACO clock output is derived from the receive line clock input (RLCI), so that these three TOH Serial Access Port receive side output signals do not function during a loss of this clock input.

Figure 11. TOH Serial Access Port Transmit Timing

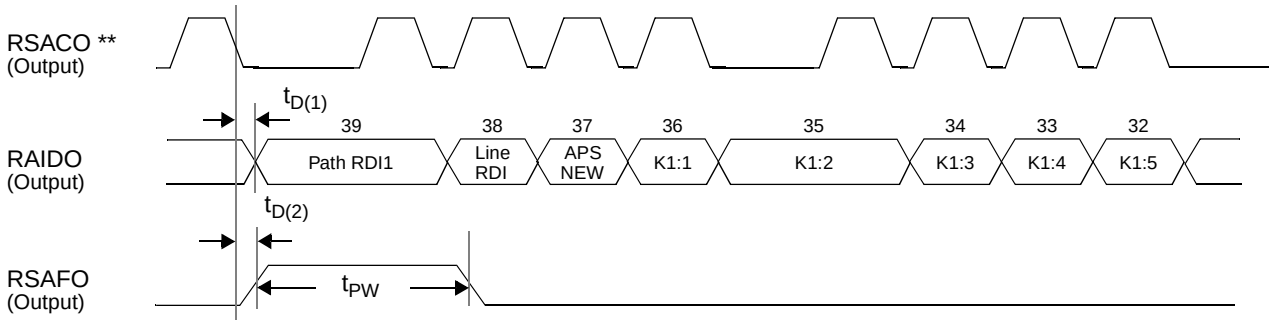


Parameter	Symbol	Min	Typ	Max	Unit
TSACO clock period	$t_{CYC(1)}$	3 x t_{CYC}*	**	6 x t_{CYC}*	ns
TSACO high time	t_{PWH}		2 x t_{CYC}*		ns
TSACO low time (non-gap time)	$t_{PWL(1)}$		1 x t_{CYC}*		ns
TSACO low time (gap time)	$t_{PWL(2)}$		4 x t_{CYC}*		ns
TSADI set-up time to TSACO↑	t_{SU}	7.0			ns
TSADI hold time after TSACO↑	t_H	3.0			ns
TSAFO delay after TSACO↑	t_D	-2.0	0.0	5.0	ns
TSAFO pulse width	t_{PW}		3 x t_{CYC}*		ns

* t_{CYC} is equal to one TRCI clock period (51.44 ns, nominal).

**Long term average TSACO clock period is 5/4(t_{CYC} x 3), or 192.9 ns, nominal.

Figure 12. Alarm Indication Port Receive Timing



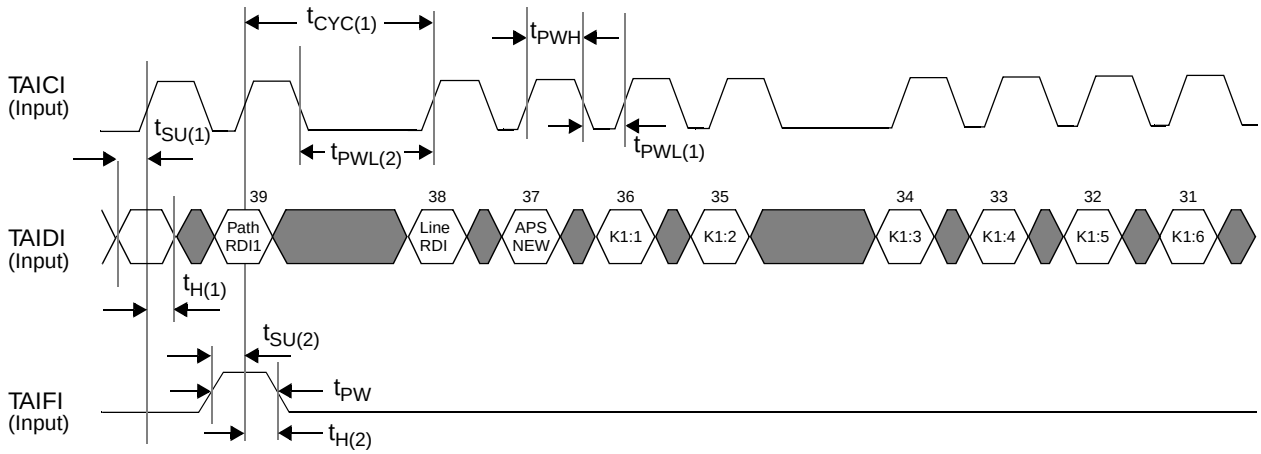
Parameter	Symbol	Min	Typ	Max	Unit
RAIDO delay after RSACO↓	$t_{D(1)}$	-2.0	0.0	5.0	ns
RSAFO delay after RSACO↓	$t_{D(2)}$	-2.0	0.0	5.0	ns
RSAFO pulse width	t_{PW}		6 x t_{CYC}*		ns

*t_{CYC} is equal to one RLCI clock period (51.44 ns, nominal).

**Timing characteristics of RSACO are shown in Figure 10.

Note: The RSACO clock output is derived from the receive line clock input (RLCI), so that the three Alarm Indication Port output signals shown here do not function during a loss of this clock input.

Figure 13. Alarm Indication Port Transmit Timing

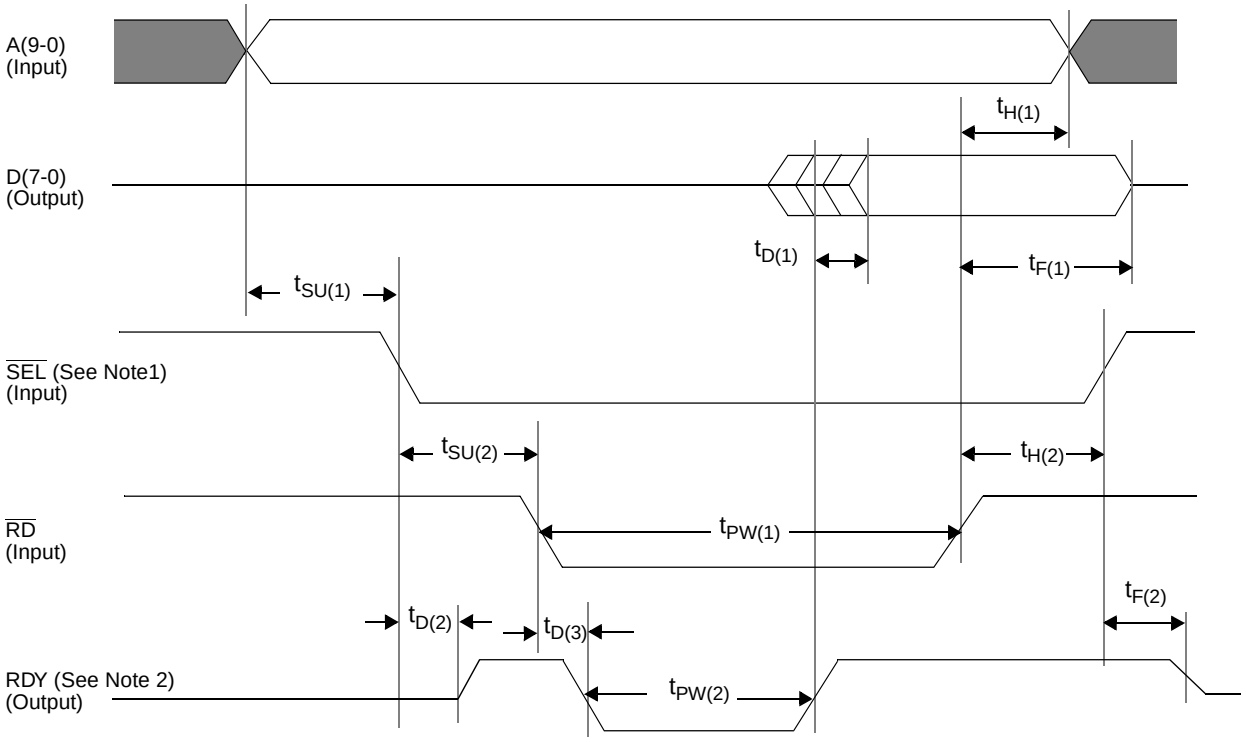


Parameter **	Symbol	Min	Typ	Max	Unit
TAICI clock period	$t_{CYC(1)}$	3 x t_{CYC}*		6 x t_{CYC}*	ns
TAICI high time	t_{PWH}		2 x t_{CYC}*		ns
TAICI low time (non-gap time)	$t_{PWL(1)}$		1 x t_{CYC}*		ns
TAICI low time (gap time)	$t_{PWL(2)}$		4 x t_{CYC}*		ns
TAIDI set-up time to TAICI↑	$t_{SU(1)}$	7.0			ns
TAIDI hold time after TAICI↑	$t_{H(1)}$	3.0			ns
TAIFI set-up time to TAICI↑	$t_{SU(2)}$	7.0			ns
TAIFI hold time after TAICI↑	$t_{H(2)}$	3.0			ns
TAIFI pulse width	t_{PW}		3 x t_{CYC}*		ns

* t_{CYC} is equal to one TRCI clock period (51.44 ns, nominal) from the SOT-3 device that is sourcing the Alarm Indication Port signals.

** In applications using the Alarm Indication Port, TAICI, TAIDI and TAIFI of one SOT-3 device would normally be connected to RSACO, RAIDO, and RSAFO, respectively, of another SOT-3 device. Timing characteristics of these signals are shown in Figure 12.

Figure 14. Microprocessor Interface Bus Timing: Read Cycle - Intel Mode

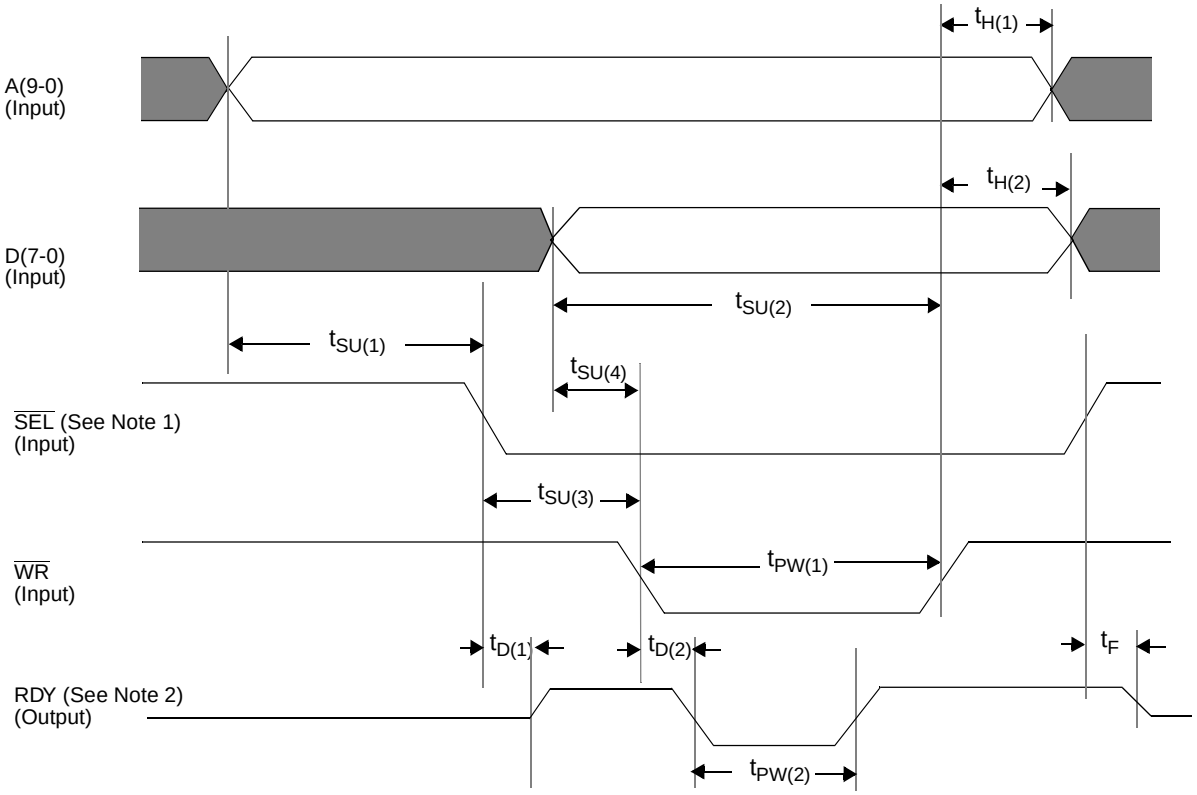


Parameter	Symbol	Min	Typ	Max	Unit
A(9-0) address hold time after $\overline{RD}\uparrow$	$t_{H(1)}$	5.0			ns
A(9-0) address set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
D(7-0) data valid delay after RDY$\uparrow$	$t_{D(1)}$			9.0	ns
D(7-0) data float time after $\overline{RD}\uparrow$	$t_{F(1)}$			7.0	ns
$\overline{RD}$ pulse width	$t_{PW(1)}$	40			ns
$\overline{SEL}\downarrow$ set-up time to $\overline{RD}\downarrow$	$t_{SU(2)}$	10			ns
$\overline{SEL}\downarrow$ hold time after $\overline{RD}\uparrow$	$t_{H(2)}$	0.0			ns
RDY$\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$			12	ns
RDY$\downarrow$ delay after $\overline{RD}\downarrow$	$t_{D(3)}$			13	ns
RDY pulse width (register access)	$t_{PW(2)}$	0.0	0.0	5.0	ns
RDY pulse width (RAM access)	$t_{PW(2)}$		14 RAMCI cycles		ns
RDY float time after $\overline{SEL}\uparrow$	$t_{F(2)}$			5.0	ns

Notes 1: $\overline{SEL}$ must be active low for $\overline{RD}$ to be valid, and $t_{SU(2)}$ must be as specified. If the SOT-3 is the only device on the bus, $\overline{SEL}$ can be grounded.

2: RDY goes low when the address being read corresponds to a RAM location but remains high during status or control register access.

Figure 15. Microprocessor Interface Bus Timing: Write Cycle - Intel Mode

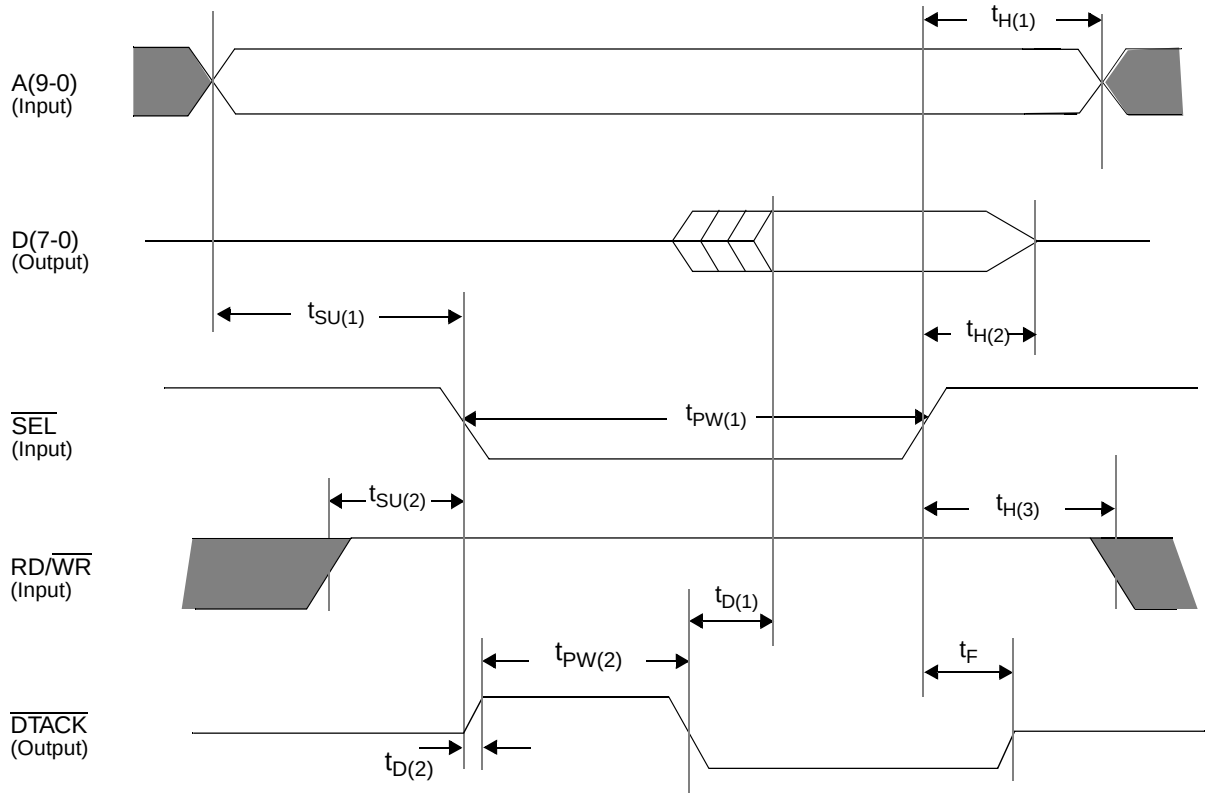


Parameter	Symbol	Min	Typ	Max	Unit
A(9-0) address hold time after $\overline{WR}\uparrow$	$t_{H(1)}$	5.0			ns
A(9-0) address set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
D(7-0) data valid set-up time to $\overline{WR}\uparrow$	$t_{SU(2)}$	20			ns
D(7-0) data hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	5.0			ns
$\overline{SEL}\downarrow$ set-up time to $\overline{WR}\downarrow$	$t_{SU(3)}$	10			ns
$\overline{WR}$ pulse width	$t_{PW(1)}$	40			ns
RDY$\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(1)}$			12	ns
RDY$\downarrow$ delay after $\overline{WR}\downarrow$	$t_{D(2)}$			13	ns
RDY pulse width (register access)	$t_{PW(2)}$	0.0	0.0	5.0	ns
RDY pulse width (RAM access)	$t_{PW(2)}$	0.0	14 RAMCI cycles	24 RAMCI cycles	ns
RDY float time after $\overline{SEL}\uparrow$	t_F			5.0	ns
RAM cycle D(7-0) valid set-up time to $\overline{WR}\downarrow$	$t_{SU(4)}$	0.0			ns

Notes 1: If the address, A(9-0), is valid 20 nanoseconds before $\overline{WR}$ becomes active low, and if the SOT-3 is the only device on the bus, then $\overline{SEL}$ can be grounded.

2: RDY goes low when the address being written to corresponds to a RAM location but remains high during status or control register access.

Figure 16. Microprocessor Interface Bus Timing: Read Cycle - Motorola Mode

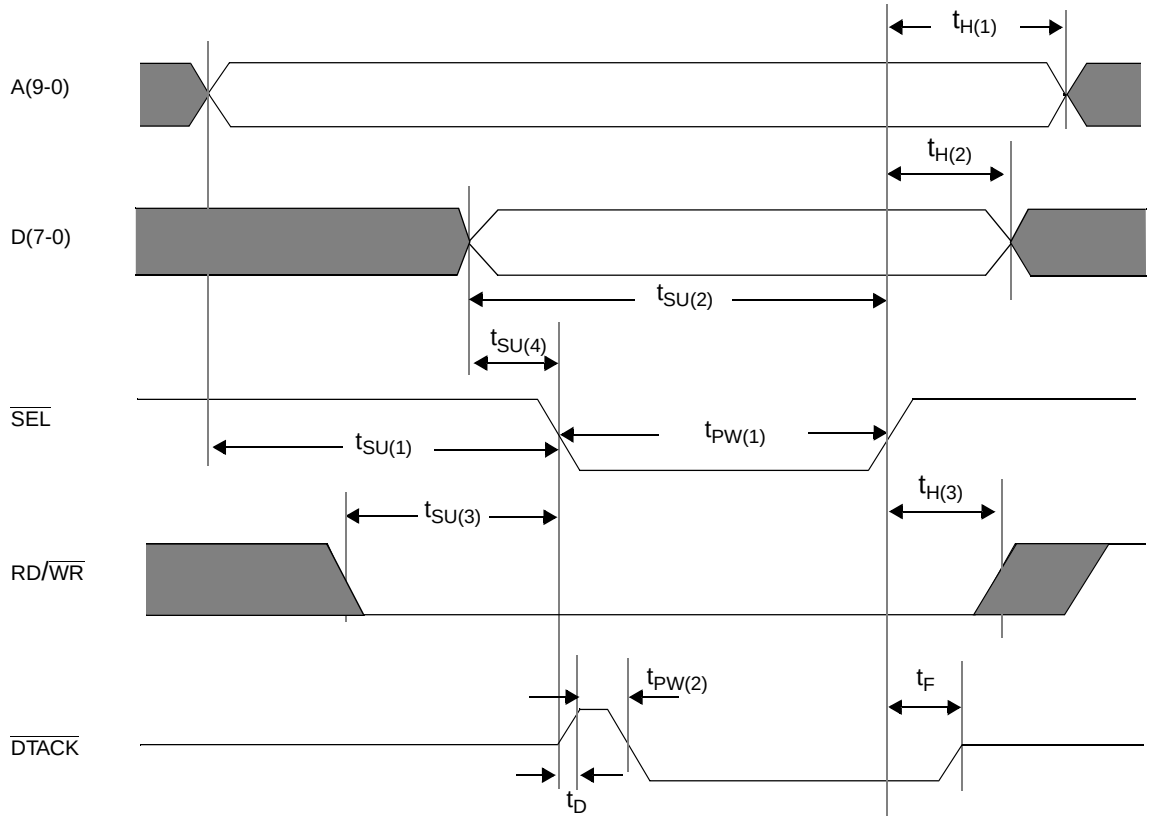


Parameter	Symbol	Min	Typ	Max	Unit
A(9-0) address valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	10			ns
A(9-0) address hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0.0			ns
D(7-0) data output delay after $\overline{DTACK}\downarrow$	$t_{D(1)}$	0.0		15*	ns
D(7-0) data output hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	5.0			ns
RD/$\overline{WR}$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	5.0			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	40			ns
RD/$\overline{WR}$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0.0			ns
$\overline{DTACK}\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$			5.0	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F			5.0	ns
$\overline{DTACK}$ pulse width (register access) **	$t_{PW(2)}$	0.0	0.0	3.0	ns
$\overline{DTACK}$ pulse width (RAM access)	$t_{PW(2)}$		14 RAMCI cycles		ns

* With maximum output load of 80 pF.

** This is a very short pulse, and is not necessary for register access.

Figure 17. Microprocessor Interface Bus Timing: Write Cycle - Motorola Mode



Parameter	Symbol	Min	Typ	Max	Unit
A(9-0) address hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0.0			ns
A(9-0) address valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	10			ns
D(7-0) data valid set-up time to $\overline{SEL}\uparrow$	$t_{SU(2)}$	20			ns
D(7-0) data hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	5.0			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	40			ns
RD/$\overline{WR}\downarrow$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(3)}$	5.0			ns
RD/$\overline{WR}\downarrow$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0.0			ns
$\overline{DTACK}\uparrow$ delay after $\overline{SEL}\downarrow$	t_D			5.0	ns
$\overline{DTACK}$ pulse width (register access) *	$t_{PW(2)}$	0.0	0.0	3.0	ns
$\overline{DTACK}$ pulse width (RAM access)	$t_{PW(2)}$	0.0	14 RAMCI cycles	24 RAMCI cycles	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F			5.0	ns
RAM cycle D(7-0) valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(4)}$	0			ns

* This is a very short pulse, and is not necessary for register access.

OPERATION

The Operation section provides additional detailed information on the operation of the functional units and processes of the SOT-3 device.

RECEIVE TRANSPORT OVERHEAD BYTE PROCESSING

All incoming SDH Section Overhead Bytes, or SONET Transport Overhead Bytes, are written into SOT-3 RAM locations. All 81 Overhead bytes are provided at the Transport Overhead Byte (TOH) Serial Access Port for external access, as required. All TOH bytes are terminated within the SOT-3 device. The receive terminal side framing bytes may be either A1=F6H and A2=28H or microprocessor-written bytes. The SOT-3 does not perform descrambling. The SYN155 device, to which the SOT-3 device is normally connected, performs that function. The B1 byte in the SYN155 device is used to convey B1 BIP-8 errors, which are accumulated in a 16-bit counter on either a bit basis or a block basis. In the block counting mode, the counter is incremented by one for any number of bit errors between 1 and 8, while in the bit counting mode it is incremented by the actual number of bits in error.

The SOT-3 device also performs a B2 BIP-24 parity check. Bit or block errors are counted in a 16-bit performance counter. The BIP-24 error count is optionally provided for transmission as line FEBE in the third Z2 byte. The source is either local, or from the mate SOT-3 in a ring configuration via the Alarm Indication Port.

The K1 byte is monitored for an inconsistent APS byte. The K1 byte and the first five bits of the K2 byte are monitored for changes in the APS status. In addition, bits 6, 7, and 8 of the K2 byte are monitored for a line RDI and a line AIS indication. Alarm status is provided, along with interrupt mask bits. Line RDI status is also provided for a mate SOT-3 in a ring configuration (see Alarm Indication Port Serial Data Interface subsection).

The H1 and H2 bytes for an STM-1 VC-4/STS-3c format and the three H1 and H2 pointer bytes for STS-3 are processed by pointer tracking state machines to determine the location of the J1 byte in the VC-4 format, or each of the three J1 bytes in the STS-3 STS-1 formats. The pointer tracking state machine is designed to meet the current ETSI and Bellcore standards (see Pointer Tracking Interpretation subsection below). In addition, when operating with the STS-3c/STS-3 formats, the AIS to LOP transition and the ss-bit checks can be disabled to conform to Bellcore/ANSI standards. Upon device reset, the pointer tracking state machines are forced to the AIS state. Pointer increments, pointer decrements, and New Data Flag (NDF) indications are counted in their corresponding 8-bit counters. The pointer is also monitored for AIS and LOP, and alarm indications are provided.

The third Z2 byte can also be monitored for a line FEBE count. When enabled by control bit Z2FEBE, a received line FEBE count is accumulated in a 16-bit performance counter.

RECEIVE PATH OVERHEAD BYTE PROCESSING

For each incoming frame, all received POH bytes are written into RAM locations for later access via a microprocessor read cycle, and they are also forwarded to the receive terminal interface after being retimed. In addition, the B3, C2, and H4 bytes are processed by the SOT-3 device, whether or not it is in the path terminating mode. The received J1 byte, either as a 16-byte message or as a 64-byte message, is written into RAM for microprocessor access via a read cycle. A 16-byte message is written as four identical 16-byte messages in a 64-byte segment. The B3 byte is checked for BIP-8 parity errors, and bit or block errors are counted in a 16-bit performance counter. The C2 byte is checked for a mismatch indication against a microprocessor-written value[1], and this byte is also checked for an Unequipped status indication. The SOT-3 device can perform H4 multiframe alignment and it provides a loss of multiframe indication. If it is enabled, the

1. Note that equipment using PDI codes may trigger C2 Mismatch because that feature is not included in the device.

H4 multiframe detector also synchronizes an H4 multiframe pattern generator whose output replaces the incoming H4 byte at the receive terminal interface (See ELOMn bit descriptions in the Memory Map Descriptions Section for details). The H4 multiframe generator can also generate optional V1 pulses that are in the correct alignment with the output H4 byte sequence. The V1 pulses are combined with the received terminal interface C1J1 indicator signal, as shown in Figure 22. This allows VT/TU add/drop multiplexer devices to use either the receive terminal side H4 byte, or the V1 pulse in the C1J1 signal, to determine the location of the V1 byte within the VT/TUs. The G1 byte is processed for a path FEBE count and a path RDI indication. The path FEBE is counted as bit or block errors in a 16-bit performance counter.

RECEIVE RETIMING

The VC-4 or the three STS-3:STS-1 signals are justified to the receive reference clock and framing signal. For the VC-4/STS-3c format, a single SPE (POH bytes and payload bytes) is justified. For the STS-3:STS-1 format, three SPEs are independently justified. One or more new pointer values are calculated and provided as H1 and H2 bytes at the receive terminal interface. The FIFOs are also monitored for overflow and underflow conditions, with either manual or automatic reset capability. If no RLCI or RRCI clock input is applied, the FIFOs cannot be reset, written or read. The result is that the receive terminal data (RTDO(7-0)), the POH pulse (RPOH) and the C1J1 signal (RC1J1) do not contain valid information and RTCO does not toggle. The outgoing pointer is generated either with the ss-bits equal to 10 for the STM-1 VC-4 format or with the ss-bits equal to 00 for the STS-3/STS-3c format.

VTAIS AND PATH AIS INSERTION AT RECEIVE TERMINAL INTERFACE

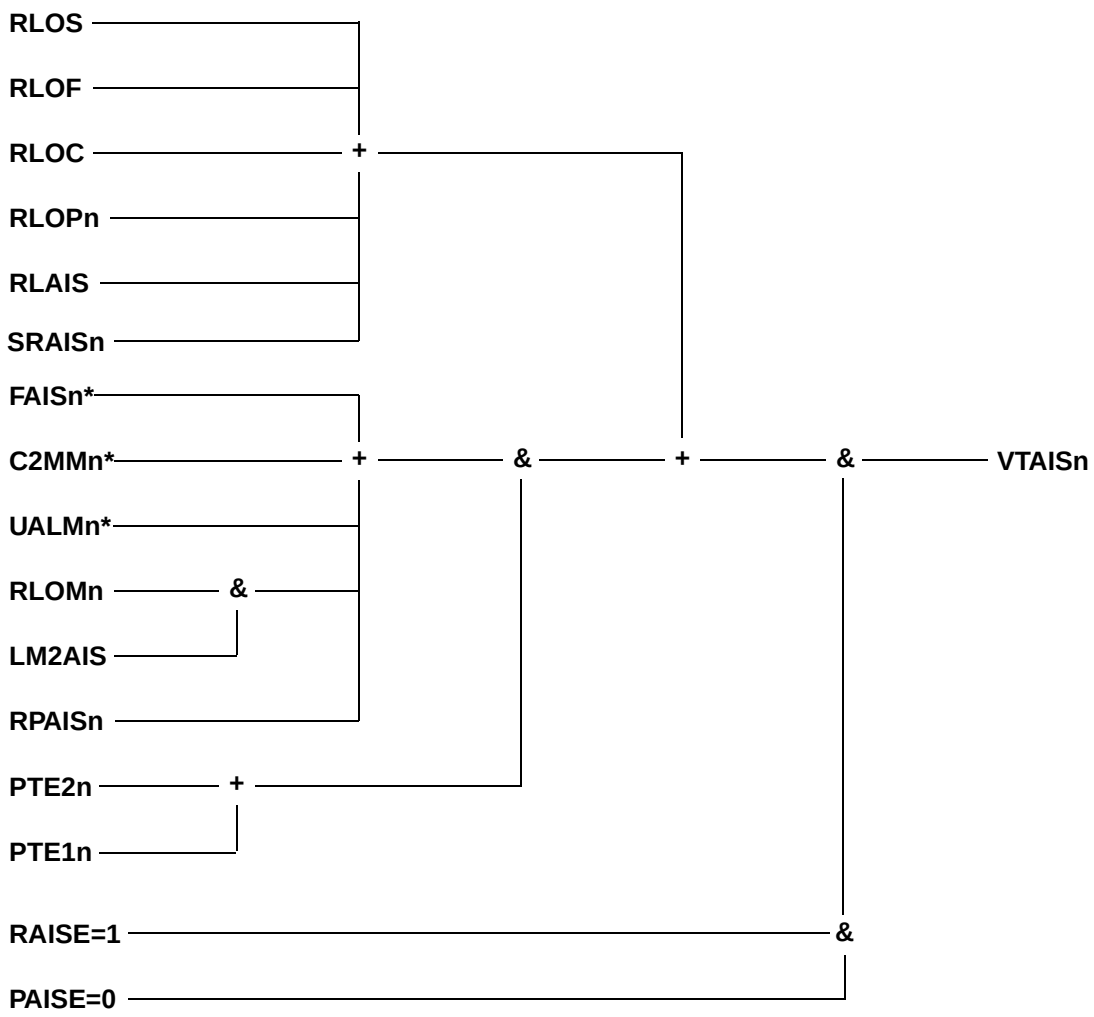
The SOT-3 device has the ability to generate and insert two types of Alarm Indication Signals (AIS), VTAIS and path AIS, when local alarms occur in the receive direction for either the VC-4/STS-3c SPE or each of the three STS-3:STS-1 signals.

A VTAIS consists of an H1/H2 pointer value equal to 522 (Decimal), zeros in the H3 byte, and all ones in the payload bytes, including the POH bytes, except the H4 byte. The H4 byte multiframe indication is the 2-bit sequence generated by the received H4 multiframe generator. During VTAIS the RPOH output will not be active. The conditions for generation of VTAISn, where n=1-3, are illustrated in the logic diagram of Figure 18. Please note that the J1 pulse will go to a position corresponding to the pointer value of 522.

Path AIS (PAIS) can also be generated as a result of local alarms. Path AIS consists of all ones in the POH bytes and payload bytes, as well as in the H1, H2 and H3 bytes. During path AIS the RPOH output will continue to pulse at times where the receive pointer tracking state machines identify POH bytes. The conditions for generation of PAISn, where n=1-3, are illustrated in the logic diagram of Figure 19. Please note that the J1 pulse may not remain frozen to the position corresponding to the last valid pointer value prior to the path AIS condition. This may cause an erratic condition during AIS-causing conditions (i.e., LOS, LOF, $\overline{\text{FAIS}}$n and SRAISn).

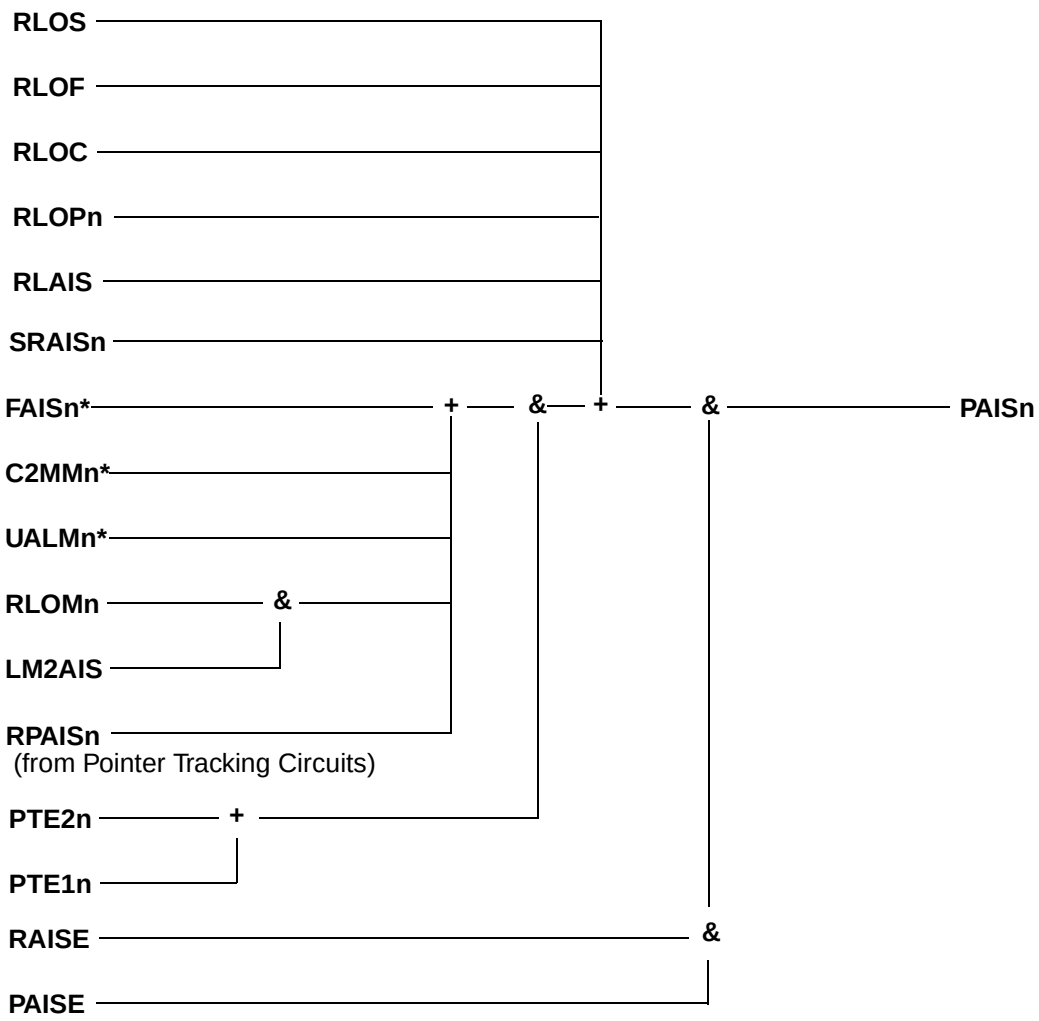
Recovery from an AIS condition causes a New Data Flag (NDF) to be generated, followed by a disabled NDF and the same pointer value, provided that there was no change in the incoming pointer value during the AIS condition.

Figure 18. Logic Diagram for Generation of VTAISn



Note: + represents a logical OR of inputs from the left, & represents a logical AND. n=1-3. Signals marked with * also require MODE0 tied low since they are enhanced features.

Figure 19. Logic Diagram for Generation of PAISn



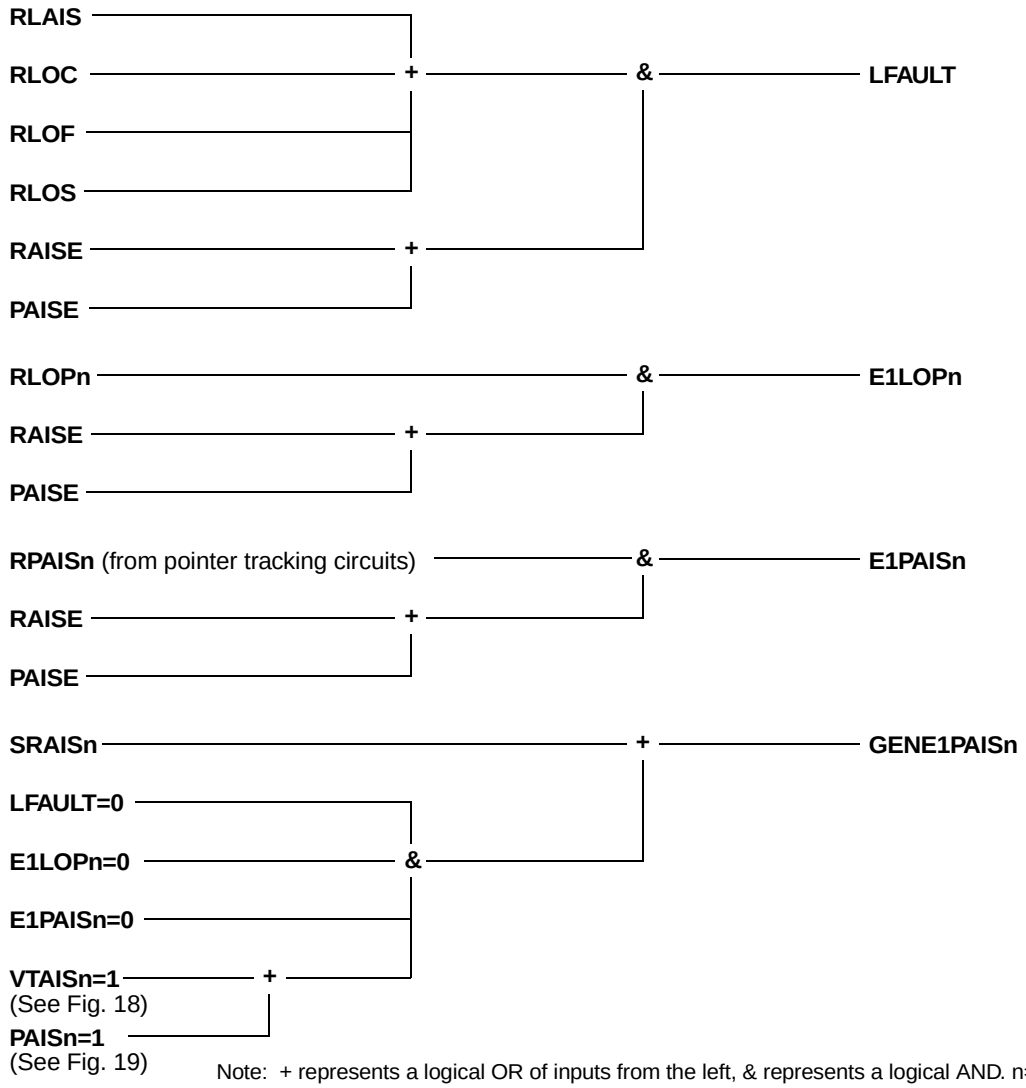
Note: + represents a logical OR of inputs from the left, & represents a logical AND. n=1-3. Signals marked with * also require MODE0 tied low since they are enhanced features.

E1 BYTE AIS INDICATION

The receive terminal side E1 bytes can be enabled, by setting the MODE0 pin either low or high, to provide either detailed alarm status information or an all ones (FFH) indication during an AIS condition for the VC-4/ STS-3c format or for the three STS-3 STS-1 signals. The format of the E1n byte (where n=1-3), and the logic diagrams for the generation of its detailed alarm status information content, are provided in Figure 20. Faults which are not a function of n are coded into all three E1n bytes. When MODE0 is tied high, either RLOC, RLOPn, RLAIS, RLOS or RLOF cause a GENE1PAIS condition. No other conditions are active in this mode.

Transmission Sequence *	Bit 1	Bit 2	Bit 3	Bit 4	Bits 5-8
E1n Byte Content	LFAULT or GENE1PAISn	E1LOPn or GENE1PAISn	E1PAISn or GENE1PAISn	LRDI or GENE1PAISn	LFAULT or E1LOPn or E1PAISn or GENE1PAISn
Data Output Pin	RTDO7 (MSB)	RTDO6	RTDO5	RTDO4	RTDO(3-0)

* Note: Bit 1 corresponds to the first bit of the byte in the STM/STS serial bit stream.



Note: + represents a logical OR of inputs from the left, & represents a logical AND. n=1-3.

Figure 20. Format of E1n Byte AIS Indication and Logic Diagram for its Content

POINTER TRACKING INTERPRETATION

The pointer tracking algorithm implemented in the SOT-3 device is illustrated in Figure 21. The pointer tracking state machine is based on the pointer tracking state machine found in the latest ETSI requirements, and is also valid for both Bellcore and ANSI.

For AU-4/STS-3c operation, a single pointer tracking state machine is employed for pointer tracking using the H11 and H21 bytes. For AU-3/STS-3 operation there are three pointer tracking state machines, one for each AU-3/STS-1 signal, using the H11/H21, H12/H22, and H13/H23 byte pairs, respectively. The pointer is extracted from the concatenation of the H1n and H2n bytes, and is interpreted as follows:

H1n Byte								H2n Byte							
1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
N	N	N	N	ss-bits		I	D	I	D	I	D	I	D	I	D

NNNN = New Data Flag Bits. This is interpreted as enabled = 1001 or 0001/1101/1011/1000, and normal or disabled = 0110 or 1110/0010/0100/0111 (i.e., a single bit error is tolerated).

ss = Size bits used in pointer tracking state machine interpretation if enabled by CCITT control bit = 1

I = Increment Bits defined as bits 1, 3, 5, 7 and 9 of the 10-bit pointer field.

D = Decrement Bits defined as bits 0, 2, 4, 6 and 8 of the 10-bit pointer field.

Negative Justification: Inverted 5 D-bits and accept majority rule.

Positive Justification: Inverted 5 I-bits and accept majority rule.

The pointer is a binary number with the range of 0 to 782. It is a 10-bit value derived from the two least significant bits of the H1 byte, with the H2 byte concatenated, to form an offset in 3-byte counts from the H3 byte location. For example, for an STM-1 signal, a pointer value of 0 indicates that the VC-4 starts in the byte location 3 bytes after the H3 byte, whereas an offset of 87 indicates that the VC-4 starts three bytes after the K2 byte.

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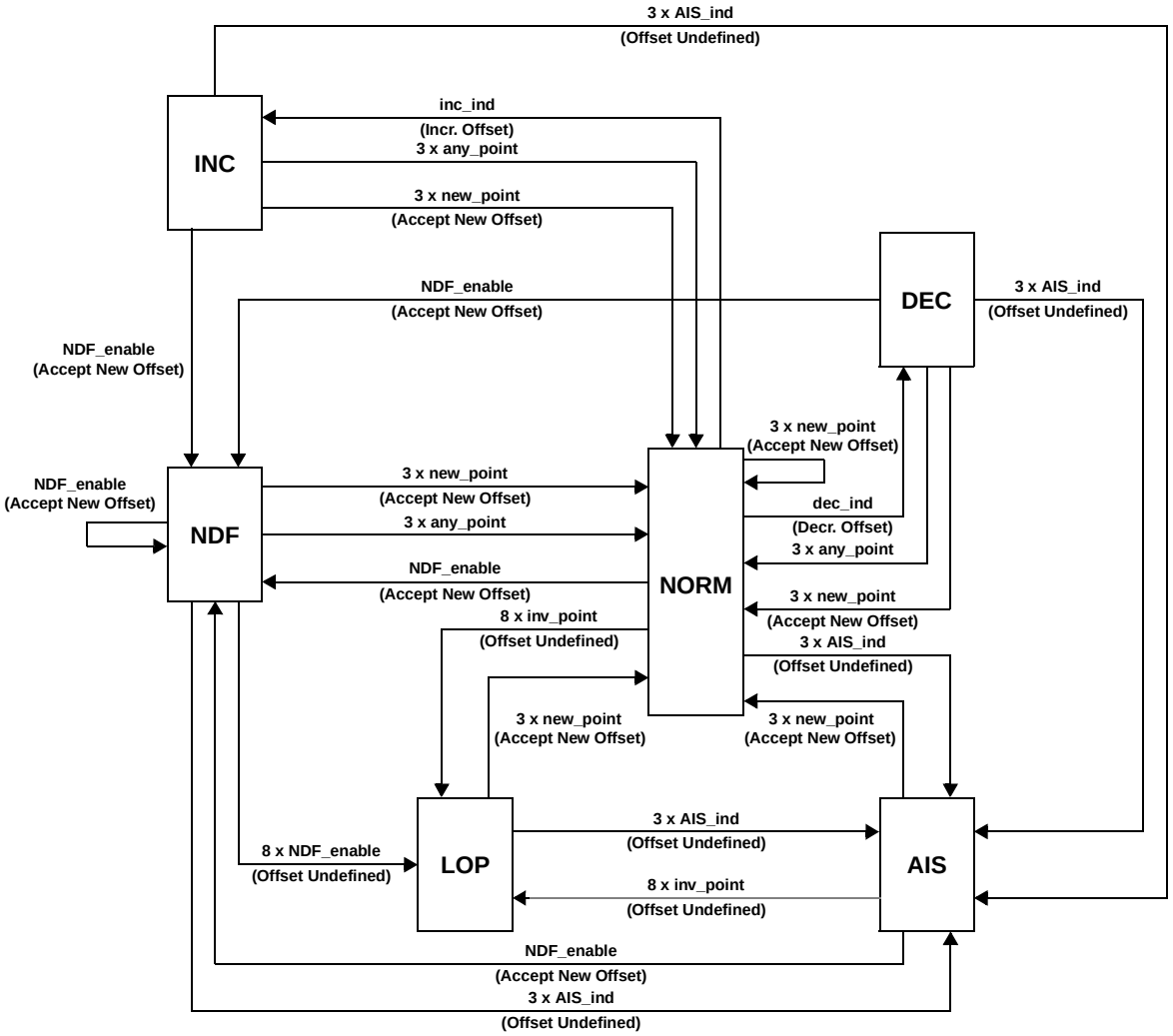

Figure 21. STS Pointer Tracking State Machine

TRANSMIT TERMINAL INTERFACE OPERATING MODES

The transmit terminal interface may be operated in the normal mode, data communication mode, or source timing mode. For the normal mode of operation, the clock, data, C1J1 and SPE signals are inputs to the SOT-3 device. The SOT-3 device can also be configured to accept a V1 pulse in the C1J1 signal. If a V1 pulse is provided, it can be used to synchronize an H4 multiframe generator. The SOT-3 device assumes that the H4 multiframe sequence is aligned to the location of the V1 byte. These signals may be derived from drop bus timing signals. Control bits are provided to enable the H4 byte from the terminal to be passed through to the line.

The data communication mode enables the SOT-3 device to operate with the TranSwitch HDLC device, or other similar devices, in a VC-4/STS-3c format. In this mode, the clock, C1J1, SPE, and POH indicator signals are outputs from the SOT-3 device. The SPE signal is active only for the payload byte times. The POH indication signal is provided to identify the location of the POH bytes. It is assumed that, in this mode, the POH bytes will be multiplexed into the bit stream by the SOT-3 device. POH byte multiplexing control bits are provided in registers 3E1H and 3E5H.

The source timing mode enables the SOT-3 device to provide transmit timing (sometimes referred to as add bus timing) for add/drop multiplexer and mapper devices operating with a VC-4 or STS-1 format. In this mode, the clock, C1J1, SPE, and POH indicator signals are outputs from the SOT-3 device. The SPE signal will be high during the POH and payload byte times. The SOT-3 H4 multiframe sequence generator may be enabled to provide one or more V1 pulses. The V1 pulses will be combined with the C1J1 signal. This allows the add/drop multiplexer device to identify the starting location of the V1 byte based on the transmitted H4 byte multiframe sequence. The relationship between the transmitted H4 byte and the generated V1 pulse is shown in the table below:

H4 Bit	1	2	3	4	5	6	7	8	V1 Pulse	Comment
Frame 1	1	1	1	1	1	1	0	0	0	
Frame 2	1	1	1	1	1	1	0	1	1	Starting location for V1 byte
Frame 3	1	1	1	1	1	1	1	0	0	
Frame 4	1	1	1	1	1	1	1	1	0	

The composite C1J1V1 signal is used in conjunction with the SPE signal to determine the location of various bytes, as illustrated in Figure 22.

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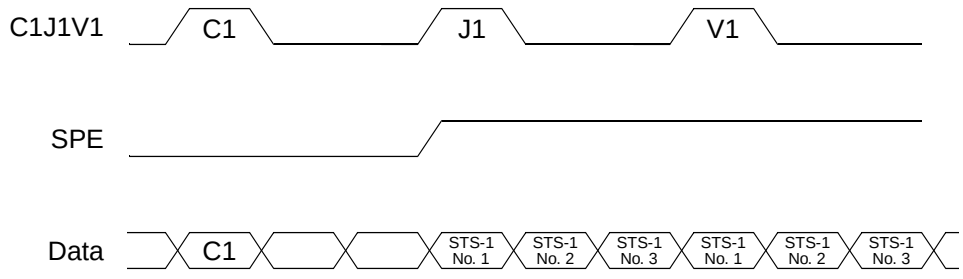


Note: The pointer value is 522 Decimal.

Figure 22. Transmit Terminal Interface C1J1V1 Signal Format

The pulse on C1J1V1 when the SPE signal is low is a C1 pulse. The C1 pulse identifies the location of the C1 byte. When the SPE signal is high, a pulse on the C1J1 pin is either a J1 or a V1. A single J1 pulse identifies the starting location of the J1 byte in the VC-4 format. Three J1 pulses are provided for the AU-3/STS-3 format, each identifying the starting location of the J1 byte in one of the three AU-3/STS-1 signals.

For the STM-1 VC-4 format, a single V1 pulse will occur once every four frames, three clock cycles after the J1 pulse. For STS-3:STS-1 format, three V1 pulses will be present every four frames. Each V1 pulse will occur three clock cycles after the corresponding J1 pulse. For example, in a VC-4 signal, the J1 pulse identifies the J1 byte location (defined as the starting location for the VC-4) in the POH bytes. In the next column (first clock cycle) all the rows are assigned as fixed stuff. Similarly, in the next column (second clock cycle) all the rows are assigned as fixed stuff. The next column (third clock cycle) defines the start of TUG-3 “A”. This column is where the V1 pulse occurs every four frames. However, the actual V1 byte will occur six clock cycles after the V1 pulse.

BUS PARITY

The SOT-3 device uses a common control bit (TPLEV) for determining if the parity should be even or odd at the receive and transmit terminal interfaces. In the receive direction, parity is generated for data, SPE, and the C1J1 signals. In the transmit direction, an enable bit (PDAT) permits parity to be calculated for the data signal only, or for the data, C1J1 and the SPE signals together. In the transmit direction, a parity error, other than providing an alarm indication, will not disable the data bit stream. The transmit parity checking mechanism is disabled in the data communication and source timing modes of operation.

TRANSMIT RETIMING

The incoming payload is justified to the transmit reference clock and framing signal. For the VC-4/STS-3c format, a single SPE (POH bytes and payload bytes) is justified. For the STS-3:STS-1 format, three SPEs are independently justified. Three separate FIFOs are used. The FIFOs are also monitored for overflow and underflow conditions, with either manual or automatic reset capability. If no TTCI or TRCI clocks are applied, the FIFOs cannot be reset. The result is that the transmit line data (TLDO), frame (TLFO) and clock (TLCO) are not valid. The pointer is either generated with the ss-bits equal to 10 for the STM-1 VC-4 format or with the ss-bits equal to 00 for the STS-3/STS-3c format.

TRANSMIT TRANSPORT (SECTION) OVERHEAD BYTE PROCESSING

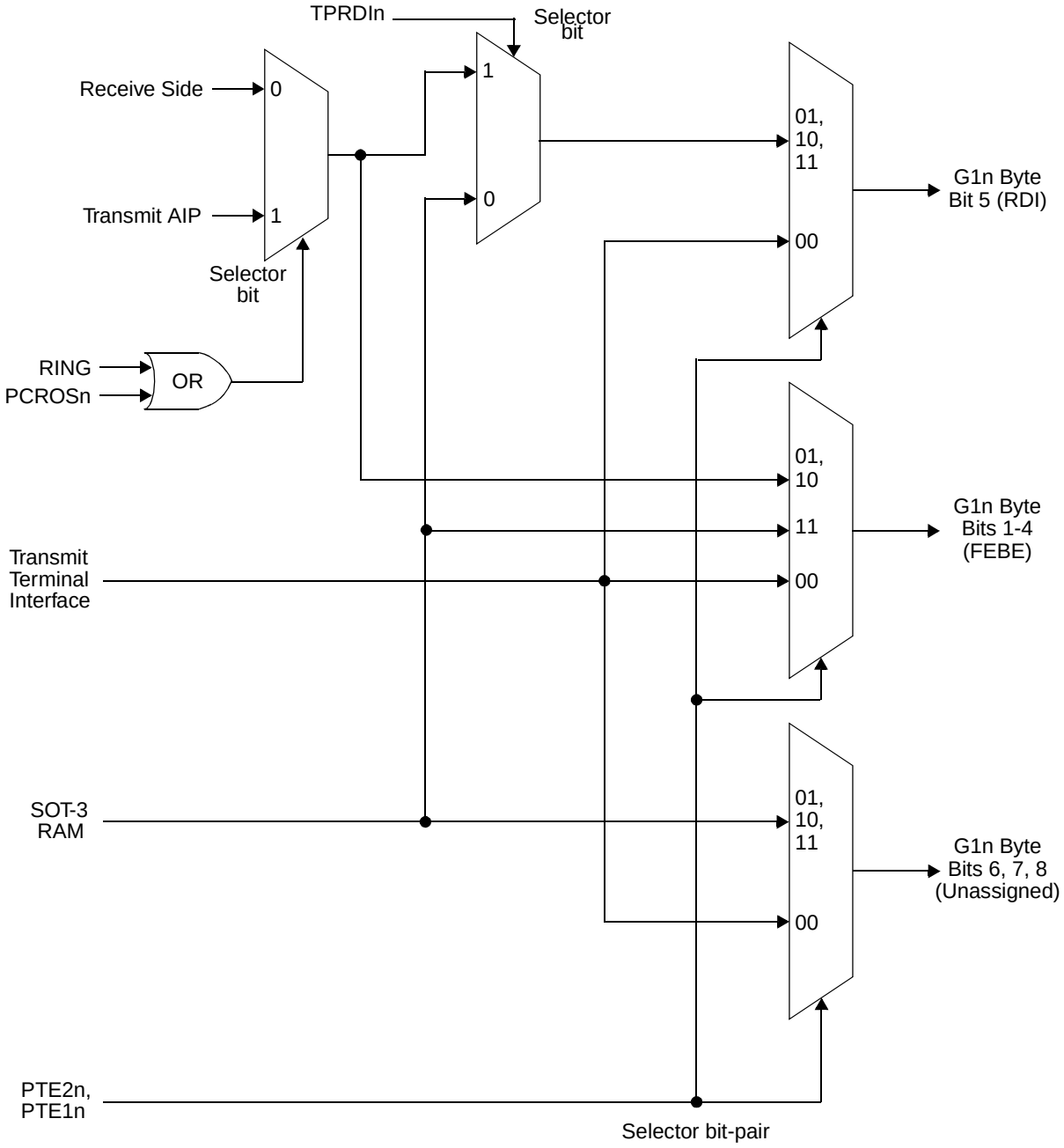
The transmit TOH bytes are multiplexed into the bit stream from RAM locations, except for the H1/H2 pointer bytes. The RAM locations may be written by the microprocessor or by the TOH Serial Access Port. TOH bytes may also be internally generated (for example, the A1 and A2 framing bytes). Although a BIP-8 is not calculated for the B1 byte, the contents of the RAM location or the external B1 byte received via the TOH Serial Access Port may be used as an error mask for generating BIP-8 errors in an upstream device, such as the TranSwitch SYN155. The SOT-3 device also performs a BIP-24 for the three B2 bytes, and an option is provided for inserting the line FEBE count into the third Z2 byte. A control bit is provided that enables a microprocessor-written pointer byte, or the TOH Serial Access Port H1/H2 byte value, to be transmitted. However, the SPE is actually aligned to the external clock and frame reference signals TRCI and TRFI.

TRANSMIT PATH OVERHEAD BYTE PROCESSING

Control bits are provided that enable the SOT-3 device to operate in a non-path terminating mode or a path terminating mode for the STM-1 VC-4/STS-3c signal, or independently for each of the three STS-3:STS-1 signals. In the non-path terminating mode, the POH bytes must accompany the payload bytes at the transmit terminal interface. In this mode, the SOT-3 device will not recalculate the B3 byte, nor will it insert the FEBE count or path RDI status into the G1 byte. This mode assumes that the downstream device, such as a TranSwitch L3M or L4M device, will perform these operations. In the path terminating mode, the SOT-3 device can insert the POH bytes from RAM locations written by the microprocessor, calculate the B3 BIP-8, insert the FEBE count and control the path RDI state. When operating in a ring configuration, the FEBE count inserted and the path RDI state are controlled from the mate SOT-3 device via the Alarm Indication Port. Figure 23 shows how the G1 byte multiplex is created for the transmit output. Figure 24 defines the sources of the path overhead bytes in each of the three transmit operating modes.

In addition, the SOT-3 device has control bits which enable it to generate an Unequipped status or Supervisory Unequipped status for the STM-1 VC-4/STS-3c, or independently for each of the three STS-3:STS-1 signals. An Unequipped status is defined as all zeros in the POH and payload bytes. A Supervisory Unequipped status is defined as all zeros in the payload bytes with valid information in the POH bytes.

Figure 23. G1 Byte Multiplex for Transmit Line Output



Operating Mode	PTE2n, PTE1n	STM-1/STS-3 POH Byte Sources J1n	B3n	C2n	G1n	F2n	H4n	Z3n	Z4n	Z5n
Normal or Source Timing	00	T	T	T	T	T	T	T	T	T
	01	R	C	R	M	T	T/H	T	T	T
	10	R	C	R	M	R	R	R	R	R
	11	R	C	R	M	R	T/H	R	R	R
Datacom	XX	R	C	R	M	R	R	R	R	R

Legend for Source of POH Bytes

T = Terminal

R = SOT-3 RAM

C = Calculated by SOT-3

AM = Multiplexed from Transmit Alarm Indication Port

RM = Multiplexed from Receive side

M = Multiplexed from above two sources based on states of RING and PCROSn bits (n=1-3). See Figure 23.

X = Don't care

H = Sourced from internal H4 multiframe generator if enabled by H4INS

Notes:

1. Changing PTE2n, PTE1n to/from 00 resets J1n counter to 0 (where n=1-3).
2. $\overline{\text{J1SYNC}}$ and RESET reset all J1 counters to 0.
3. See Figure 23 for additional information on G1n byte sourcing.

Figure 24. Sourcing of Line Side Transmit Path Overhead Bytes

THROUGHPUT DELAY

Throughput delay is the difference between the input and output pointers, under the conditions listed in the table below. The delay characteristics are a function of the pointer value, pointer movements, and jitter. These factors affect the internal FIFO fill characteristics.

Direction	Minimum Bytes (Typ - 14)	Typical Bytes	Maximum Bytes (Typ + 15)
Receive, line to terminal (see Note 1)	4	18	33
Transmit, terminal to line (see Note 2)	3	17	32

Notes 1: Typical delay is measured with:
1. FIFO depth of 14
2. RLCI clock same as RRCI
   RLFI framing input same as RRFI
3. STS-3 mode

2: Typical delay is measured with:
1. FIFO depth of 14
2. TTCI clock same as TRCI
   Transmit terminal device framing reference is TRFI
3. Normal operating mode (i.e., not datacom)
4. STS-3 mode

ALARM INDICATION PORT SERIAL DATA INTERFACE

The RAIDO output pin provides the status of receive alarms for ring applications. It is connected to the TAIDI input pin of the mate SOT-3 device. The data format is a serial stream of 40 bits that is transmitted once per frame. Data is clocked out on the falling edge of the Receive TOH Clock (RSACO). The receive TOH framing signal (RSAFO) occurs during the first bit (No. 39) of the Alarm Indication Port data stream. The output has the format shown in Figure 25.

Bit No.	Indication
39	Send path RDI (yellow) for STM-1/STS-3c AU-4 or STS-3:STS-1 No. 1
38	Send line RDI (FERF)
37	New APS byte alarm indication (see status bit RNAPS)
36-21	Debounced K1 and K2 bytes. Bit 1 of K1 is transmitted first (No. 36) and bit 8 of K2 last (No. 21).
20-17	Sum of B3 Parity Error Count for STM-1/STS-3c AU-4 or STS-3:STS-1 No. 1. Bit No. 20 is MSB.
16	Line FEBE. Bit No. 16 corresponds to bit 4 in the Z23 byte.
15	Send path RDI (yellow) for STS-3:STS-1 No. 2
14	Send line RDI (FERF). Same value as bit No. 38.
13	Line FEBE. Bit No. 13 corresponds to bit 5 in the Z23 byte.
12	Line FEBE. Bit No. 12 corresponds to bit 6 in the Z23 byte.
11-8	Sum of B3 Parity Error Count for STS-3:STS-1 No. 2. Bit No. 11 is MSB.
7	Send path RDI (yellow) for STS-3:STS-1 No. 3
6	Send line RDI (FERF). Same value as bit No. 38.
5	Line FEBE. Bit No. 5 corresponds to bit 7 in the Z23 byte.
4	Line FEBE. Bit No. 4 corresponds to bit 8 in the Z23 byte.
3-0	Sum of B3 Parity Error Count for STS-3:STS-1 No. 3. Bit No. 3 is MSB.

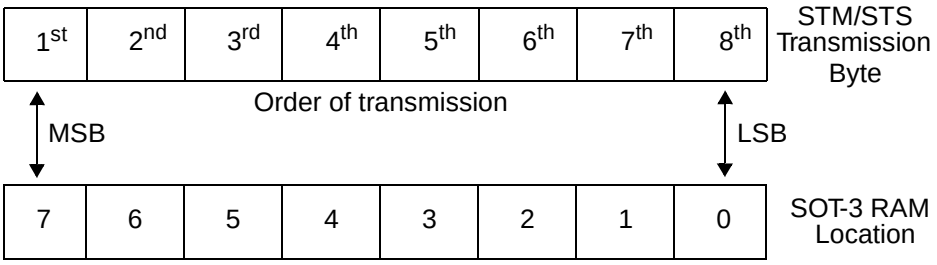
Notes:

1. Send path RDI (yellow) is inserted into the transmit line signal if any one of several conditions occurs. Refer to the description of the Transmit Path RDI Enable (1-3) control bits (TPRDIn) in the Control Register Descriptions section (n=1-3).
2. Line RDI (FERF) is inserted into the transmit line signal under the conditions detailed in the description of the Transmit Line RDI control bit (TRLRDI) in the Control Register Descriptions section.
3. New APS is an indication that the same new value of the K1 and K2 bytes has been received for three consecutive frames. K1 and K2 (bits 36-21) are the latest bytes persisting for at least three frames.

Figure 25. Format of Serial Data Stream on Receive Alarm Indication Port Data Out (RAIDO) Pin

RANDOM ACCESS MEMORY (RAM)

The random access memory (RAM) of the SOT-3 device is partitioned into the following segments: Receive Overhead Bytes, Transmit Overhead Bytes, Control, Status, Interrupt Mask Bits, and Performance Counters, as shown in the Memory Map for RAM Locations section. All address locations are stated in Hexadecimal (H). The bit placement relationship between a receive and transmit serial SDH/SONET (STM/STS) byte (e.g., C1) and its corresponding storage location in a RAM segment is shown below:



The SOT-3 device requires an asynchronous clock with a frequency in the range from 16 to 20 MHz. The clock of the external microprocessor may be used if it falls within this range.

PERFORMANCE COUNTERS

All performance counters roll over from all-ones to all-zeros, and they are not cleared on a microprocessor read cycle. During a read operation on a counter, an incoming count is held until the read cycle is complete, then the counter is updated. The 8-bit increment (INC) and decrement (DEC) pointer justification counters and New Data Flag (NDF) counters are set to the value FE Hexadecimal (FEH) during a device reset. The B1, B2 and three B3 error counters, the three receive path FEBE counters, and the receive line FEBE counter are all 16-bit counters. These are reset to FFE0H during a device reset. A shared high order byte location is used to provide temporary storage of the high order byte while the low order byte is being read.

A special 16-bit read operation is used to allow uninterrupted microprocessor access and avoid the risk of one 16-bit counter segment (byte) changing while the other segment is being read. To perform a 16-bit read, the low order byte is read first. This automatically transfers the high order byte count to the common storage location, 3FFH. This location must be read before the next 16-bit read is initiated, to avoid loss of the high order byte due to over-writing by another 16-bit read. The 3FFH location is used as the temporary high order byte storage location for all 16-bit performance counters and the two 16-bit locations for debounced K1-K2 byte storage.

ALARMS AND INTERRUPTS

Each alarm bit position in memory is indicated as having either an unlatched or a latched mode of operation. An unlatched alarm bit position remains set only for the duration of the alarm condition. A latched alarm bit position latches on the positive level of the alarm and will remain latched after the alarm clears, until it is read by the microprocessor, when it will automatically be reset. However, if the corresponding alarm persists during the microprocessor read cycle, the latched alarm bit position will remain set after the cycle is completed. A newly-active alarm condition will be held until the read cycle is complete before action is taken. It should be noted that the RNAPS (bit 7 in 3D4H) and BERR (bit 4 in 3D6H) alarm indications have short pulse durations, which may not be read successfully by the microprocessor. The corresponding latched alarm bit position in the next address will indicate that an alarm has taken place.

A global software interrupt indication bit (SINT, addresses 3D6H and 3D7H, bit 7) is provided, as well as a hardware interrupt pin (INT/$\overline{IRQ}$, pin 45). A hardware interrupt enable bit (HINT, address 3F3H, bit 7) is provided. When HINT is set to 1, a hardware interrupt is activated when SINT becomes set to 1 due to activation of one or more of the latched alarms for which the corresponding interrupt mask bit has been set to 1 (in memory locations 3F0H through 3F4H). Interrupt mask bits are provided for each of the latched alarms. The interrupt will be maintained after the alarm bit read cycle if the alarm persists. The interrupt can be disabled by writing a 0 to the corresponding mask bit.

The SOT-3 status bits and interrupt mask bits have sets of three error bits for the following alarms (where n=1-3):

RPAISn	Receive Path AIS
RLOPn	Receive Loss of Pointer
RLOMn	Receive Loss of Multiframe
RPRDIn	Receive Path RDI
SPRDIn	Transmit AIP Send Path RDI
UALMn	Receive Unequipped Status
C2MMn	C2 Mismatch

Since the STS-1 No. 2 and No. 3 bits for STS-3 are unused in STM-1/STS-3c they could be employed for other purposes or retain a default value, so they must be masked by writing zeros in the interrupt mask bits table in order to avoid unwarranted interrupts. The masked bits are those with a 2 or 3 as the designator number. If the SOT-3 is used for STS-3, these mask bits can be set to one to enable the interrupt.

The SOT-3 device is not sensitive to payload contents. Therefore, for bulk STM-1 or STS-3c payloads where there is no need for a multiframe indicator, all RLOMn interrupt mask bits must be set to zero to avoid a spurious interrupt.

MEMORY MAP FOR RAM LOCATIONS

STM-1/STS-3/STS-3C RECEIVE OVERHEAD BYTE RAM LOCATIONS

Transport (Section) Overhead (Note 2)										Path Overhead (Note 3)		
A1 000	**A1** 01B	**A1** 036	**A2** 001	**A2** 01C	**A2** 037	**C11** 002	**C12/N1** 01D	**C13/N2** 038		**J11** 080-0BF	**J12** 0C0-0FF	**J13** 100-13F
B1 003	**M1** 01E	**M2** 039	**E1** 004	**M3** 01F	**U1** 03A	**F1** 005	**N3** 020	**N4** 03B		**B31** 060	**B32** 068	**B33** 070
D1 006	**M4** 021	**M5** 03C	**D2** 007	**M6** 022	**U2** 03D	**D3** 008	**U3** 023	**U4** 03E		**C21** 061	**C22** 069	**C23** 071
H11 009	**H12** 024	**H13** 03F	**H21** 00A	**H22** 025	**H23** 040	**H31** 00B	**H32** 026	**H33** 041		**G11** 062	**G12** 06A	**G13** 072
B21 00C	**B22** 027	**B23** 042	**K1** 00D	**U5** 028	**U6** 043	**K2** 00E	**U7** 029	**U8** 044		**F21** 063	**F22** 06B	**F23** 073
D4 00F	**U9** 02A	**U10** 045	**D5** 010	**U11** 02B	**U12** 046	**D6** 011	**U13** 02C	**U14** 047		**H41** 064	**H42** 06C	**H43** 074
D7 012	**U15** 02D	**U16** 048	**D8** 013	**U17** 02E	**U18** 049	**D9** 014	**U19** 02F	**U20** 04A		**Z31** 065	**Z32** 06D	**Z33** 075
D10 015	**U21** 030	**U22** 04B	**D11** 016	**U23** 031	**U24** 04C	**D12** 017	**U25** 032	**U26** 04D		**Z41** 066	**Z42** 06E	**Z43** 076
Z11 018	**Z12** 033	**Z13** 04E	**Z21** 019	**Z22** 034	**Z23** 04F	**E2** 01A	**N5** 035	**N6** 050		**Z51** 067	**Z52** 06F	**Z53** 077

Notes:

1. These locations are all read-only.
2. The TOH bytes are all terminated in the SOT-3 device, and they are provided at the receive output of its TOH Serial Access Port.
3. POH bytes which have 2 or 3 as the final character of their symbol are unused for STM-1/STS-3c.

STM-1/STS-3/STS-3C TRANSMIT OVERHEAD BYTE RAM LOCATIONS

Transport (Section) Overhead										Path Overhead (Note 2)		
A1 140	**A1** 15B	**A1** 176	**A2** 141	**A2** 15C	**A2** 177	**C11** 142	**C12/N1** 15D	**C13/N2** 178		**J11** 1C0-1FF	**J12** 200-23F	**J13** 240-27F
B1 143	**M1** 15E	**M2** 179	**E1** 144	**M3** 15F	**U1** 17A	**F1** 145	**N3** 160	**N4** 17B		**B31** 1A8	**B32** 1B0	**B33** 1B8
D1 146	**M4** 161	**M5** 17C	**D2** 147	**M6** 162	**U2** 17D	**D3** 148	**U3** 163	**U4** 17E		**C21** 1A9	**C22** 1B1	**C23** 1B9
H11 149	**H12** 164	**H13** 17F	**H21** 14A	**H22** 165	**H23** 180	**H31** 14B	**H32** 166	**H33** 181		**G11** 1AA	**G12** 1B2	**G13** 1BA
B21 14C	**B22** 167	**B23** 182	**K1** 14D	**U5** 168	**U6** 183	**K2** 14E	**U7** 169	**U8** 184		**F21** 1AB	**F22** 1B3	**F23** 1BB
D4 14F	**U9** 16A	**U10** 185	**D5** 150	**U11** 16B	**U12** 186	**D6** 151	**U13** 16C	**U14** 187		**H41** 1AC	**H42** 1B4	**H43** 1BC
D7 152	**U15** 16D	**U16** 188	**D8** 153	**U17** 16E	**U18** 189	**D9** 154	**U19** 16F	**U20** 18A		**Z31** 1AD	**Z32** 1B5	**Z33** 1BD
D10 155	**U21** 170	**U22** 18B	**D11** 156	**U23** 171	**U24** 18C	**D12** 157	**U25** 172	**U26** 18D		**Z41** 1AE	**Z42** 1B6	**Z43** 1BE
Z11 158	**Z12** 173	**Z13** 18E	**Z21** 159	**Z22** 174	**Z23** 18F	**E2** 15A	**N5** 175	**N6** 190		**Z51** 1AF	**Z52** 1B7	**Z53** 1BF

Notes:

1. These locations are all read/write, except when sourced by the TOH Serial Access Port. However, the microprocessor is not prohibited from writing to these locations.
2. POH bytes which have 2 or 3 as the final character of their symbol are unused for STM-1/STS-3c.

CONTROL BITS

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3E0	R/W	EXDCOW	EXAPS	EXF1Z	EXUN	EXABH	TRPAISE	TRLRDI	TRLAISE
3E1	R/W	RTLOOP	TAIS1	CCITT	PTE21	PTE11	RING	RAISE	TRLOOP
3E2	R/W	TLB	TCAT3	TCAT2	TCAT1	FLB	LCAT3	LCAT2	LCAT1
3E3	R/W	TRPTR	E12AIS	TPRDI1	FRENB	LM2AIS	SRAIS1	FIFORST	0
3E4	R/W	RTA1A2E	Z2FEBE	PDAT	TPLEV	H4INS	PAISE	RV1EN	BLOCK
3E5	R/W	TLA1A2E	PCROS3	PCROS2	PCROS1	PTE23	PTE13	PTE22	PTE12
3E6	R/W	TPRDI3	TPRDI2	UNEQ3	UQPOH3	UNEQ2	UQPOH2	UNEQ1	UQPOH1
3E7	R/W	STIME	TAIS3	TAIS2	SRAIS3	SRAIS2	ELOM3	ELOM2	ELOM1
3E8	R/W	C2R1: C2 Microprocessor-Written Mismatch Value For STS-3 STS No. 1 (Bit 7 is MSB)							
3E9	R/W	C2R2: C2 Microprocessor-Written Mismatch Value For STS-3 STS No. 2 (Bit 7 is MSB)							
3EA	R/W	C2R3: C2 Microprocessor-Written Mismatch Value For STS-3 STS No. 3 (Bit 7 is MSB)							
3EB	R/W	RTA1: Receive Terminal Interface A1 Byte Value (Bit 7 is MSB)							
3EC	R/W	RTA2: Receive Terminal Interface A2 Byte Value (Bit 7 is MSB)							
3ED	R/W	0	0	0	INVCI	RDPAR	0	0	0

Notes: 1.R/W=Read/Write 2.Bits marked as 0 must be set to zero.

STATUS BITS

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3D0	R	RLOC	RLOS	ROOF	RLOF	RLAIS	RPAIS3	RPAIS2	RPAIS1
3D1	R/W(L)	RLOC	RLOS	ROOF	RLOF	RLAIS	RPAIS3	RPAIS2	RPAIS1
3D2	R	RAPS	RLOP3	RLOP2	RLOP1	RLRDI	RLOM3	RLOM2	RLOM1
3D3	R/W(L)	RAPS	RLOP3	RLOP2	RLOP1	RLRDI	RLOM3	RLOM2	RLOM1
3D4	R	RNAPS*	RPRDI3	RPRDI2	RPRDI1	RFIFO	TFIFO	Reserved	APNAPS
3D5	R/W(L)	RNAPS	RPRDI3	RPRDI2	RPRDI1	RFIFO	TFIFO	Reserved	APNAPS
3D6	R	SINT	TLOC	TLOS	BERR*	RAMLOC	SPRDI3	SPRDI2	SPRDI1
3D7	R/W(L)	SINT	TLOC	TLOS	BERR	RAMLOC	SPRDI3	SPRDI2	SPRDI1
3D8	R	TAIPLOC	Reserved	UALM3	UALM2	UALM1	C2MM3	C2MM2	C2MM1
3D9	R/W(L)	TAIPLOC	Reserved	UALM3	UALM2	UALM1	C2MM3	C2MM2	C2MM1
3DA	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
3DB	R/W(L)	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
3DC	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
3DD	R/W(L)	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Notes:

1. R=Read-Only; R/W=Read/Write; R/W(L)=Read/Write Latched Register (latched bits are cleared on read).
2. Bits marked as Reserved are designated for internal diagnostics.
3. *Short duration alarm indications of RNAPS and BERR may not be read successfully by the microprocessor, but the latched bit in the next address will be set for reading.

INTERRUPT MASK BITS

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3F0	R/W	RLOC	RLOS	ROOF	RLOF	RLAIS	RPAIS3	RPAIS2	RPAIS1
3F1	R/W	RAPS	RLOP3	RLOP2	RLOP1	RLRDI	RLOM3	RLOM2	RLOM1
3F2	R/W	RNAPS	RPRDI3	RPRDI2	RPRDI1	RFIFO	TFIFO	0	APNAPS
3F3	R/W	HINT	TLOC	TLOS	BERR	RAMLOC	SPRDI3	SPRDI2	SPRDI1
3F4	R/W	TAIPLOC	0	UALM3	UALM2	UALM1	C2MM3	C2MM2	C2MM1
3F5	R/W	0	0	0	0	0	0	0	0
3F6	R/W	0	0	0	0	0	0	0	0

Notes:

1. R/W=Read/Write.
2. Bits marked as 0 must be set to 0.
3. Setting the interrupt mask bit to 1 enables the interrupt for the corresponding latched alarm bit in the status bit segment.

PERFORMANCE COUNTERS AND K1-K2 BYTE REGISTERS

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
051	R	Positive Justification (Increment) Counter for STM-1/STS-3c, STS-3:STS-1 No. 1							
054	R	Positive Justification (Increment) Counter for STS-3:STS-1 No. 2							
057	R	Positive Justification (Increment) Counter for STS-3:STS-1 No. 3							
052	R	Negative Justification (Decrement) Counter for STM-1/STS-3c, STS-3:STS-1 No. 1							
055	R	Negative Justification (Decrement) Counter for STS-3:STS-1 No. 2							
058	R	Negative Justification (Decrement) Counter for STS-3:STS-1 No. 3							
053	R	NDF Counter for STM-1/STS-3c, STS-3:STS-1 No. 1							
056	R	NDF Counter for STS-3:STS-1 No. 2							
059	R	NDF Counter for STS-3:STS-1 No. 3							
192	R	B1 Error Counter Low Order Byte							
194	R	B2 Error Counter Low Order Byte							
196	R	Received Debounced K1-K2 Bytes (K1 location)							
198	R	B31 Error Counter for STM-1/STS-3c, STS-3:STS-1 No. 1 Low Order Byte							
19A	R	B32 Error Counter for STS-3:STS-1 No. 2 Low Order Byte							
19C	R	B33 Error Counter for STS-3:STS-1 No. 3 Low Order Byte							
19E	R	Receive path FEBE Counter for STM-1/STS-3c, STS-3:STS-1 No. 1 Low Order Byte							
1A0	R	Receive path FEBE Counter for STS-3:STS-1 No. 2 Low Order Byte							
1A2	R	Receive path FEBE Counter for STS-3:STS-1 No. 3 Low Order Byte							
1A4	R	Debounced K1-K2 Bytes from Alarm Indication Port (K1 location)							
1A6	R	Receive Line FEBE Counter Low Order Byte							
3FF	R	Shared High Byte, used for reading high order byte of 16-bit counters and debounced K2 Byte. This byte must be read before the next 16-bit read is initiated.							

Note: Mode R=Read-Only

MEMORY MAP DESCRIPTIONS

DESCRIPTIONS OF OVERHEAD IN RAM

Receive Transport (Section) Overhead Byte RAM Locations

Address*	Bit	Symbol	Description **
000 01B 036	7-0	A1	**A1 Byte Receive Line Framing Pattern:** The first six bytes in the SDH Section Overhead byte locations or SONET Transport Overhead byte locations are dedicated to carrying the SDH/SONET framing pattern. The A1 byte framing pattern is F6H, and is carried in the first three bytes. The received framing pattern is not checked by the SOT-3.
001 01C 037	7-0	A2	**A2 Byte Receive Line Framing Pattern:** The first six bytes in the SDH Section Overhead byte locations or SONET Transport Overhead byte locations are dedicated to carrying the SDH/SONET framing pattern. The A2 byte framing pattern is 28H, and is carried in the last three bytes. The received framing pattern is not checked by the SOT-3.
002	7-0	C11	**STM-1/STS-3:STS-1 No. 1 Identifier:** The number written into this location identifies the STM-1 position relative to the higher order multiplex signal. For an STS-3 signal, the number in this location represents the STS-1 No. 1 signal in its order of appearance in the higher order demultiplexed signal.
01D	7-0	C12/N1	**STS-3:STS-1 No. 2 Identifier:** The number written into this location represents the STS-1 No. 2 signal in its order of appearance in the higher order demultiplexed signal. For an STM-1 format, this signal is assigned for national use (N1).
038	7-0	C13/N2	**STS-3:STS-1 No. 3 Identifier:** The number written into this location represents the STS-1 No. 3 signal in its order of appearance in the higher order demultiplexed signal. For an STM-1 format, this signal is assigned for national use (N2).
003	7-0	B1	**Upstream B1 Error Indication:** In most applications the SOT-3 will be connected to a SYN155 device. The SYN155 maps B1 bit errors into the received B1 byte. Any bit that is 1 represents a BIP-8 error in that particular bit location. The error indications (up to eight received per frame) are added to the 16-bit B1 error counter (low order byte in 192H), either as a bit error count or as a single block count.
004	7-0	E1	**Order Wire Channel:** This byte provides a voice communication channel for SDH/SONET applications. For an STM-n signal, the order wire channel is assigned to STM-1 No. 1. For an STS-n signal, the order wire channel is assigned to STS-1 No. 1.
005	7-0	F1	**User Wire Channel:** This byte is reserved for user applications.
006 007 008	7-0	D1 D2 D3	**Serial Data Communication Channel:** For an STM-n signal, the data communication channel is designated for STM-1 No. 1. For an STS-3/STS-3c signal, these bytes are designated for a 192 kbit/s data communication channel, which may carry alarm or maintenance information. For an STS-3 signal, these bytes are designated for STS-1 No. 1.

* All address locations in these tables are identified in Hexadecimal and referred to as ###H (e.g., 000H).

** See Memory Map for RAM Locations section for important notes which are generally applicable to all address locations in a section of memory.

Address*	Bit	Symbol	Description **
009 00A 00B	7-0	H11 H21 H31	**Pointer and Action Bytes for STM-1 AU-4/STS-3c or STS-3:STS-1 No. 1:** The information carried in the H11 and H21 bytes identifies the location of the J1 byte in the VC-4 format, or the J1 byte in the STS-3: STS-1 No. 1 signal. The format of these two bytes is shown below: Bits of H11 Byte — Bits of H21 Byte 1 2 3 4 5 6 7 8 — 1 2 3 4 5 6 7 8 — VC-4/STS-3 pointer 7 6 5 4 3 2 1 0 — 7 6 5 4 3 2 1 0 — SOT-3 RAM N N N N s s I D — I D I D I D I D — Content The pointer range is 0 to 782 Decimal. For an AU-4 pointer, the ss-bits are defined as 10 and are checked by the pointer tracking state machine. For SONET STS-3c and STS-3:STS-1 signals the ss-bits are assigned as 00 and these bits are not checked by the SOT-3 pointer tracking state machine. The N bits are defined as the New Data Flag bits and normally carry the value 0110. An NDF is indicated by receiving a 1001 pattern (see Note 1). The I and D bits are used for justification. As a result of retiming, new pointer byte values in H11 and H21 are provided at the receive terminal interface.
024 025 026	7-0	H12 H22 H32	**Pointer and Action Bytes for STS-3:STS-1 No. 2:** The information carried in the H12 and H22 bytes identifies the location of the J1 byte in the STS-3:STS-1 No. 2 signal. The format of these two bytes for an STM-1/ STS-3c signal is shown below: Bits of H12 Byte — Bits of H22 Byte 1 2 3 4 5 6 7 8 — 1 2 3 4 5 6 7 8 — STM-1/STS-3c pointer 7 6 5 4 3 2 1 0 — 7 6 5 4 3 2 1 0 — SOT-3 RAM 1 0 0 1 0 0 1 1 — 1 1 1 1 1 1 1 1 — Content For STM-1/STS-3c, these bytes are not checked. The format of these two bytes for an STS-3 signal is shown below: Bits of H12 Byte — Bits of H22 Byte 1 2 3 4 5 6 7 8 — 1 2 3 4 5 6 7 8 — STS-3 Pointer 7 6 5 4 3 2 1 0 — 7 6 5 4 3 2 1 0 — SOT-3 RAM N N N N s s I D — I D I D I D I D — Content The pointer range is 0 to 782 Decimal. For SONET STS-3c and STS-3:STS-1 signals the ss-bits are assigned as 00 and these bits are not checked by the SOT-3 pointer tracking state machine. The N bits are defined as the New Data Flag bits and normally carry the value 0110. An NDF is indicated by receiving a 1001 pattern (see Note 1). The I and D bits are used for justification. As a result of retiming, new pointer values in H12 and H22 are provided for STS-3:STS-1 No. 2 at the receive terminal interface.

Note 1: NDF is reported for the following values: 1001 (the specified value for a New Data Flag) and the following single bit error values: 0001, 1101, 1011, 1000. The normal value for NDF is 0110 or any of the following single-bit error values: 1110, 0010, 0100, 0111.

Address*	Bit	Symbol	Description **
03F 040 041	7-0	H13 H23 H33	**Pointer and Action Bytes for STS-3:STS-1 No. 3:** The information carried in the H13 and H23 bytes identifies the location of the J1 byte in the STS-3:STS-1 No. 3 signal. The format of these two bytes for an STM-1/ STS-3c signal is shown below: Bits of H13 Byte / Bits of H23 Byte 1 2 3 4 5 6 7 8 / 1 2 3 4 5 6 7 8 STM-1/STS-3c pointer 7 6 5 4 3 2 1 0 / 7 6 5 4 3 2 1 0 SOT-3 RAM 1 0 0 1 0 0 1 1 / 1 1 1 1 1 1 1 1 Content For STM-1/STS-3c, these bytes are not checked. The format of these two bytes for an STS-3 signal is shown below: Bits of H13 Byte / Bits of H23 Byte 1 2 3 4 5 6 7 8 / 1 2 3 4 5 6 7 8 STS-3 Pointer 7 6 5 4 3 2 1 0 / 7 6 5 4 3 2 1 0 SOT-3 RAM N N N N s s I D / I D I D I D I D Content The pointer range is 0 to 782 Decimal. For SONET STS-3c and STS-3:STS-1 signals the ss-bits are assigned as 00 and these bits are not checked by the SOT-3 pointer tracking state machine. The N bits are defined as the New Data Flag bits and normally carry the value 0110. An NDF is indicated by receiving a 1001 pattern (see Note 1). The I and D bits are used for justification. As a result of retiming, new pointer byte values in H13 and H23 are provided for STS-3:STS-1 No. 3 at the receive terminal interface.
00C 027 042	7-0	B21 B22 B23	**Line Parity BIP-24:** The three received bytes are assigned to carry a BIP-24. The three B2 bytes are written into these locations and compared with the calculated BIP-24 value. The number of valid errors detected (0 through 24, with higher values treated as 0) is added to a single 16-bit B2 error counter as either bit or block errors (low order byte in location 194H). The number of valid errors is also sent to the Alarm Indication Port for ring operation.
00D 00E	7-0	K1 K2	**Automatic Protection Switching (APS) Bytes:** The K1 byte is monitored for inconsistent APS bytes. The K1 byte and the first five bits of the K2 byte are monitored for a change in APS byte status. A value that persists for three or more frames is written into locations 196H (K1 byte) and 197H (K2 byte). In addition, the K2 byte is monitored for a line AIS indication and a line RDI indication.

Note 1: NDF is reported for the following values: 1001 (the specified value for a New Data Flag) and the following single bit error values: 0001, 1101, 1011, 1000. The normal value for NDF is 0110 or any of the following single-bit error values: 1110, 0010, 0100, 0111.

Address*	Bit	Symbol	Description **
00F 010 011 012 013 014 015 016 017	7-0	D4 D5 D6 D7 D8 D9 D10 D11 D12	**Line Data Communication Channel:** For an STM-n signal, the data communication channel is designated for STM-1 No. 1. For an STS-3/STS-3c signal, these bytes are designated for a 576 kbit/s data communication channel, which may carry alarm or maintenance information. For an STS-3 signal, these bytes are designated for STS-1 No. 1.
01A	7-0	E2	**Order Wire Channel:** This byte provides a voice communication channel for SDH/SONET applications. For an STM-n signal, the order wire channel is assigned to STM-1 No. 1. For an STS-n signal, the order wire channel is assigned to STS-1 No. 1.
018 033 04E 019 034	7-0	Z11 Z12 Z13 Z21 Z22	**Growth Bytes:** These five bytes are allocated for functions not yet fully defined.
04F	7-0	Z23	**Optional Line FEBE Byte:** The last five bits in this byte may carry a line FEBE value. Binary values between 0 and 24 (Decimal) are the only accepted values for a line FEBE (however, higher values may be received if the transmitting device is a not a SOT-3 or it is a SOT-3 that sources the B2 FEBE Count from a mate device in RING mode via the AIP). The line FEBE count is assigned to the bits as shown below: 1 2 3 4 5 6 7 8 Received SDH/SONET byte 7 6 5 4 3 2 1 0 SOT-3 RAM bit 0 0 0 MSB .. Count .. LSB Content When control bit Z2FEBE (bit 6 in 3E4H) is set to 1, a received binary value between 0 and 24 is counted. Counts other than 0-24 are counted as a value equal to 0. The count is added to a 16-bit line FEBE counter (low order byte at location 1A6H). The count is also sent to the Alarm Indication Port for ring operation. When control bit Z2FEBE is set to 0, the contents of this byte are ignored.[
020 03B 035 050	7-0	N3 N4 N5 N6	**National Use:** These bytes are assigned for national use. The N1 and N2 bytes are located at addresses 01DH and 038H.
01E 039 01F 021 03C 022	7-0	M1 M2 M3 M4 M5 M6	**Media Specific Use:**

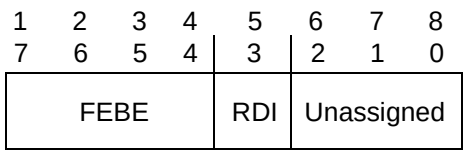
Address*	Bit	Symbol	Description **
03A 03D 023 03E 028 043 029 044 02A 045 02B 046 02C 047 02D 048 02E 049 02F 04A 030 04B 031 04C 032 04D	7-0	U1 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 U26	**Unused bytes:** These bytes are not assigned in STM/STS signals but are still available in RAM.

Receive Path Overhead Byte RAM Locations for STM-1/STS-3c/STS-3:STS-1 No. 1

Address	Bit	Symbol	Description
080-0BF	7-0	J11	**Path Trace Message for STM-1 VC-4/STS-3c, STS-3:STS-1 No. 1:** The path trace message is a repetitive 64-byte or 16-byte message. When control bit CCITT is 1, four 16-byte messages are written into four 16-byte RAM segments. The incoming messages are written into the next sequential RAM segments in a rotating fashion, without a defined starting address location.
060	7-0	B31	**Path BIP-8 for STM-1 VC-4/STS-3c, STS-3:STS-1 No. 1:** The value in this location is the received B3 parity byte. For error monitoring, parity is checked by computing even parity over all bits of the STM-1 AU-4 (261 columns), the STS-3c SPE (261 columns) or the STS-1 SPE (87 columns), and comparing the calculated value with the B31 value received in the next frame. Errors (up to eight per frame) are added to a 16-bit B31 error counter as individual bits or a single block (low order byte in location 198H). The detection of B31 errors causes a Far End Block Error (FEBE) to be sent when its transmission is selected by the PTE control bits. The errors are sent to the Alarm Indication Port for ring operation.

Address	Bit	Symbol	Description
061	7-0	C21	**Path Signal Label for STM-1 VC-4/STS-3c, STS-3:STS-1 No. 1:** This byte is used to indicate the construction of the VC-4 (STM) or SPE (STS). Internally, the SOT-3 checks for a signal label mismatch against a micro-processor-written value (3EAH) and Unequipped.
062	7-0	G11	**Path Status Byte for STM-1 VC-4/STS-3c, STS-3:STS-1 No. 1:** This location provides the received FEBE value (bits 7-4), path RDI status (bit 3), and the value of the unassigned bits (bits 2-0), from the received G1 byte, as shown below: 1 2 3 4 5 6 7 8 Received G1 byte 7 6 5 4 3 2 1 0 RAM location FEBE | RDI | Unassigned The FEBE count, a value from 0 to 8, is added to a 16-bit FEBE counter as bit or block errors (low order byte in 19EH). Values other than 0-8 are counted as 0.
063	7-0	F21	**Path User Channel for STM-1 VC-4/STS-3c, STS-3:STS-1 No. 1:** This byte provides user information between path elements, if required.
064	7-0	H41	**Multiframe Indicator for STM-1 VC-4/STS-3c, STS-3:STS-1 No. 1:** The H4 byte is assigned to carry a multiframe indicator sequence for identifying the location of the V1 byte in a 1544 or 2048 kbit/s VT/TU. For other mappings, such as mapping a DS3 signal into SONET, the H4 byte is unassigned. The H4 byte multiframe sequence for a VT/TU is shown below: 1 2 3 4 5 6 7 8 Received H4 byte 7 6 5 4 3 2 1 0 RAM location X X X X X X 0 0 X X X X X X 0 1 Synchronized to V1 byte X X X X X X 1 0 X X X X X X 1 1 Repeated Four-Step Sequence (where X = don't care) The received H4 pattern is monitored for a loss of multiframe. When enabled (by ELOM1), the SOT-3 generates the H4 value based on the incoming value. If a loss of multiframe occurs, the sequence is maintained while searching for a new multiframe pattern. If a new sequence is detected, the generator updates its sequence to match. Whenever the ELOM1 bit is set, the 6 most significant bits are generated as all 1's.
065 066 067	7-0	Z31 Z41 Z51	**Growth Bytes for STM-1 VC-4/STS-3c, STS-3:STS-1 No. 1:** These bytes are reserved for future path growth.

Receive Path Overhead Byte RAM Locations for STS-3:STS-1 No. 2 (See Note 1)

Address	Bit	Symbol	Description
0C0-0FF	7-0	J12	**Path Trace Message for STS-3:STS-1 No. 2:** The path trace message is a repetitive 64-byte message for STS-3:STS-1 signals. The incoming messages are written into the next sequential RAM segments in a rotating fashion, without a defined starting address location.
068	7-0	B32	**Path BIP-8 for STS-3:STS-1 No. 2:** The value in this location is the received B3 parity byte. For error monitoring, parity is checked by computing even parity over all bits of the STS-1 SPE (87 columns), and comparing the calculated value with the B32 value received in the next frame. Errors (up to eight per frame) are added to a 16-bit B32 error counter as individual bits or a single block (low order byte in location 19AH). The detection of B32 errors causes a Far End Block Error (FEBE) to be sent when its transmission is selected by the PTE control bits. The errors are sent to the Alarm Indication Port for ring operation.
069	7-0	C22	**Path Signal Label for STS-3:STS-1 No. 2:** This byte is used to indicate the construction of the SPE. Internally, the SOT-3 checks for a signal label mismatch against a microprocessor-written value (3EAH) and Unequipped.
06A	7-0	G12	**Path Status Byte for STS-3:STS-1 No. 2**: This location provides the received FEBE value (bits 7-4), path RDI status (bit 3), and the value of the unassigned bits (bits 2-0), from the received G1 byte, as shown below:  The FEBE count, a value from 0 to 8, is added to a 16-bit FEBE counter as bit or block errors (low order byte in 1A0H). Values other than 0-8 are counted as 0.
06B	7-0	F22	**Path User Channel for STS-3:STS-1 No. 2:** This byte provides user information between path elements, if required.

Note 1: These bytes are unused for STM-1/STS-3c.

Address	Bit	Symbol	Description
06C	7-0	H42	**Multiframe Indicator for STS-3:STS-1 No. 2:** The H4 byte is assigned to carry a multiframe indicator sequence for identifying the location of the V1 byte in a 1544 or 2048 kbit/s VT/TU. For other mappings, such as mapping a DS3 signal into SONET, the H4 byte is unassigned. The H4 byte multiframe sequence for a VT/TU is shown below: 1 2 3 4 5 6 7 8 — Received H4 byte 7 6 5 4 3 2 1 0 — RAM location X X X X X X 0 0 X X X X X X 0 1 — Synchronized to V1 byte X X X X X X 1 0 X X X X X X 1 1 Repeated Four-Step Sequence (where X = don't care) The received H4 pattern is monitored for a loss of multiframe. When enabled (by ELOM2), the SOT-3 generates the H4 value based on the incoming value. If a loss of multiframe occurs, the sequence is maintained while searching for a new multiframe pattern. If a new sequence is detected, the generator updates its sequence to match. Whenever the ELOM2 bit is set, the 6 most significant bits are generated as all 1's.
06D 06E 06F	7-0	Z32 Z42 Z52	**Growth Bytes for STS-3:STS-1 No. 2:** These bytes are reserved for future path growth.

Receive Path Overhead Byte RAM Locations for STS-3:STS-1 No. 3 (See Note 1)

Address	Bit	Symbol	Description
100-13F	7-0	J13	**Path Trace Message for STS-3:STS-1 No. 3:** The path trace message is a repetitive 64-byte message for STS-3:STS-1 signals. The incoming messages are written into the next sequential RAM segments in a rotating fashion, without a defined starting address location.
070	7-0	B33	**Path BIP-8 for STS-3:STS-1 No. 3:** The value in this location is the received B3 parity byte. For error monitoring, parity is checked by computing even parity over all bits of the STS-1 SPE (87 columns), and comparing the calculated value with the B33 value received in the next frame. Errors (up to eight per frame) are added to a 16-bit B33 error counter as individual bits or a single block (low order byte in location 19CH). The detection of B3 errors causes a Far End Block Error (FEBE) to be sent when its transmission is selected by the PTE control bits. The errors are sent to the Alarm Indication Port for ring operation.
071	7-0	C23	**Path Signal Label for STS-3:STS-1 No. 3:** This byte is used to indicate the construction of the SPE. Internally, the SOT-3 checks for a signal label mismatch against a microprocessor-written value (3EAH) and Unequipped.

Note 1: These bytes are unused for STM-1/STS-3c.

Address	Bit	Symbol	Description
072	7-0	G13	**Path Status Byte for STS-3:STS-1 No. 3**: This location provides the received FEBE value (bits 7-4), path RDI status (bit 3), and the value of the unassigned bits (bits 2-0), from the received G1 byte, as shown below. 1 2 3 4 5 6 7 8 Received G1 byte 7 6 5 4 3 2 1 0 RAM location FEBE | RDI | Unassigned The FEBE count, a value from 0 to 8, is added to a 16-bit FEBE counter as bit or block errors (low order byte in 1A2H). Values other than 0-8 are counted as 0.
073	7-0	F23	**Path User Channel for STS-3:STS-1 No. 3:** This byte provides user information between path elements, if required.
074	7-0	H43	**Multiframe Indicator for STS-3:STS-1 No. 3:** The H4 byte is assigned to carry a multiframe indicator sequence for identifying the location of the V1 byte in a 1544 or 2048 kbit/s VT/TU. For other mappings, such as mapping a DS3 signal into SONET, the H4 byte is unassigned. The H4 byte multiframe sequence for a VT/TU is shown below: 1 2 3 4 5 6 7 8 Received H4 byte 7 6 5 4 3 2 1 0 RAM location X X X X X X 0 0 X X X X X X 0 1 Synchronized to V1 byte X X X X X X 1 0 X X X X X X 1 1 Repeated Four-Step Sequence (where X = don't care) The received H4 pattern is monitored for a loss of multiframe. When enabled (by ELOM3), the SOT-3 generates the H4 value based on the incoming value. If a loss of multiframe occurs, the sequence is maintained while searching for a new multiframe pattern. If a new sequence is detected, the generator updates its sequence to match. Whenever the ELOM3 bit is set, the 6 most significant bits are generated as all 1's.
075 076 077	7-0	Z33 Z43 Z53	**Growth Bytes for STS-3:STS-1 No. 3:** These bytes are reserved for future path growth.

Transmit Transport (Section) Overhead Byte RAM Locations

Address	Bit	Symbol	Description
140 15B 176	7-0	A1	**A1 Byte Transmit Line Framing Pattern:** The first six bytes in the SDH Section Overhead byte locations (or SONET Transport Overhead byte locations) are dedicated to carrying the SDH/SONET framing pattern. The A1 byte framing pattern is normally F6H, and it is carried in the first three bytes. The first bit (bit 1) of the SDH/SONET serial byte is written into bit 7. The source of the A1 framing pattern is determined by two control bits according to the following table: TLA1A2E / EXABH / Action 0 / 0 / Internal F6H pattern transmitted for A1. (The transmitted A1 value is provided in these RAM locations.) 1 / 0 / Microprocessor-written value transmitted. (The microprocessor writes the value to be transmitted to these RAM locations.) X / 1 / Transmit Serial Access Port A1 bytes transmitted. (TOH Serial Access Port values are written to these RAM locations for a microprocessor read cycle).
141 15C 177	7-0	A2	**A2 Byte Transmit Line Framing Pattern:** The first six bytes in the SDH Section Overhead byte locations (or SONET Transport Overhead byte locations) are dedicated to carrying the SDH/SONET framing pattern. The A2 byte framing pattern is normally equal to 28H, and is carried in the last three bytes. The first bit (bit 1) of the SDH/SONET serial byte is written into bit 7. The source of the A2 framing pattern is determined by two control bits according to the following table: TLA1A2E / EXABH / Action 0 / 0 / Internal 28H pattern transmitted for A2. (The transmitted A2 value is provided in these RAM locations.) 1 / 0 / Microprocessor-written value is transmitted. (The microprocessor writes the value to be transmitted to these RAM locations.) X / 1 / Transmit Serial Access Port A2 bytes transmitted. (TOH Serial Access Port Values are written to these RAM locations for a microprocessor read cycle.)
142 15D 178	7-0	C11 C12/N1 C13/N2	**STM-1/STS-3:STS-1 Identifiers:** The multiplexing of the C1 bytes is controlled by control bit EXF1Z (bit 5 in 3E0H). When EXF1Z is 0, the microprocessor writes the values of the C1 bytes to be transmitted into these three locations. When EXF1Z is 1, the C1 bytes from the TOH Serial Access Port are written into these RAM locations prior to transmission. The first bit (bit 1) of the SDH/SONET serial byte is written into bit 7. For an STM-1 format, the second and third bytes are assigned for national use.

Address	Bit	Symbol	Description
143	7-0	B1	**B1 Error Insertion Mask:** In most applications, the SOT-3 will be connected to a SYN155 device. The SYN155 calculates the B1 byte and also performs the scrambling function. The bits in this byte may be used to generate an error in the transmitted B1 byte. This byte is exclusive-OR gated with the calculated B1 byte prior to transmission. Any bit that is 1 represents a parity error in that bit location. The multiplexing of the B1 byte is controlled by EXABH (bit 3 in 3E0H). When EXABH is 0, the microprocessor writes the error mask value into this location. A 00H value indicates no errors are to be inserted into the B1 byte. When EXABH is 1, the B1 error mask is provided via the TOH Serial Access Port, and its value is also written into this RAM location for microprocessor access.
144	7-0	E1	**Order Wire Channel:** The multiplexing of the E1 byte is controlled by EXDCOW (bit 7 in 3E0H). When EXDCOW is 0, the microprocessor writes the value of the E1 byte to be transmitted into this location. When EXDCOW is 1, the E1 byte from the TOH Serial Access Port is written into this RAM location prior to transmission. The first bit (bit 1) of the SDH/SONET serial byte is written into bit 7.
145	7-0	F1	**User Wire Channel:** The multiplexing of the F1 byte is controlled by EXF1Z (bit 5 in 3E0H). When EXF1Z is 0 the microprocessor writes the value of the F1 byte to be transmitted into this location. When EXF1Z is 1, the F1 byte from the TOH Serial Access Port is written into this RAM location prior to transmission. The first bit (bit 1) of the SDH/SONET serial byte is written into bit 7.
146 147 148	7-0	D1 D2 D3	**Serial Data Communication Channel:** The multiplexing of the three data communication bytes is controlled by EXDCOW (bit 7 in 3E0H). When EXDCOW is 0, the microprocessor writes the value of the three bytes to be transmitted into these locations. When EXDCOW is 1, the bytes from the TOH Serial Access Port are written into this RAM location prior to transmission.

Address	Bit	Symbol	Description
149 14A 14B	7-0	H11 H21 H31	**Pointer and Action Bytes for STM-1 AU-4/STS-3c or STS-3:STS-1 No. 1:** The information carried in the H11 and H21 bytes identifies the location of the J1 byte in the VC-4 format, or the J1 byte in the STS-1 No. 1 signal. The format of these two bytes is shown below: H11 Byte H21 Byte 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 VC-4/STS-3 Pointer 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 SOT-3 RAM N N N N s s I D I D I D I D I D Content The pointer range is 0 to 782 Decimal. The transmitted value is normally calculated by the retiming block, which compares the transmit terminal side VC-4/SPE with the reference timing signals. For an STM-1 AU-4 pointer, the ss-bits are defined and transmitted as 10. For SONET STS-3c and STS-3:STS-1 signals the ss-bits are transmitted as 00. The N bits are defined as the New Data Flag bits and normally carry the value 0110. An NDF is indicated by sending a 1001 pattern. The I and D bits are used for justification. The transmitted H1/H2 pointer values are determined by two control bits, according to the table shown below: TRPTR EXABH Action 0 X Normal operation. The pointer value calculated in retiming is transmitted. This location is unused. 1 0 The pointer byte values written into these RAM locations by the microprocessor are transmitted. However, retiming is still performed, and the pointer value written into these locations will not affect the starting location of the VC-4/STS-1 SPE. 1 1 The pointer byte values from the TOH Serial Access Port are transmitted and are also written into these RAM locations. However, retiming is still performed, and the pointer value written into these locations will not affect the starting location of the VC-4/STS-1 SPE.

Address	Bit	Symbol	Description
164 165 166	7-0	H12 H22 H32	**Pointer and Action Bytes for STS-3:STS-1 No. 2:** The information carried in the H12 and H22 bytes identifies the location of the J1 byte in the STS-1 No. 2 signal. The format of these two bytes is shown below: H12 Byte H22 Byte 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 SDH/SONET byte 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 SOT-3 RAM N N N N s s I D I D I D I D I D Content The pointer range is 0 to 782 Decimal. The transmitted value is normally calculated by the retiming block, which compares the transmit terminal side STS-1 SPE with the reference timing signals. For the SONET STS-3:STS-1 signal the ss-bits are transmitted as 00. The N bits are defined as the New Data Flag bits and normally carry the value 0110. An NDF is indicated by sending a 1001 pattern. The I and D bits are used for justification. For the STM-1 signal, the H12 byte is assigned as the Y byte and carries the value 93H. The H22 byte carries the value FFH. The transmitted H1/H2 pointer values are determined by two control bits, according to the table shown below: TRPTR EXABH Action 0 X Normal operation. The pointer value calculated in retiming is transmitted. This location is unused. 1 0 The pointer byte values written into these RAM locations by the microprocessor are transmitted. However, retiming is still performed, and the pointer value written into these locations will not affect the starting location of the STS-1 SPE. 1 1 The pointer byte values from the TOH Serial Access Port are transmitted and are also written into these RAM locations. However, retiming is still performed, and the pointer value written into these locations will not affect the starting location of the STS-1 SPE.

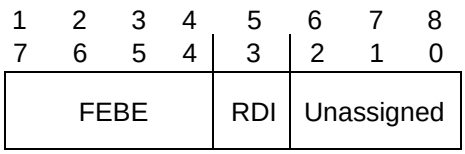
Address	Bit	Symbol	Description
17F 180 181	7-0	H13 H23 H33	**Pointer and Action Bytes for STS-3:STS-1 No. 3:** The information carried in the H13 and H23 bytes identifies the location of the J1 byte in the STS-1 No. 3 signal. The format of these two bytes is shown below: H13 Byte H23 Byte 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 SDH/SONET byte 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 SOT-3 RAM N N N N s s I D I D I D I D I D Content The pointer range is 0 to 782 Decimal. The transmitted value is normally calculated by the retiming block, which compares the transmit terminal side STS-1 SPE with the reference timing signals. For the SONET STS-3:STS-1 signal the ss-bits are transmitted as 00. The N bits are defined as the New Data Flag bits and normally carry the value 0110. An NDF is indicated by sending a 1001 pattern. The I and D bits are used for justification. For the STM-1 signal, the H13 byte is assigned as the Y byte and carries the value 93H. The H23 byte carries the value FFH. The transmitted H1/H2 pointer values are determined by two control bits, according to the table shown below: TRPTR EXABH Action 0 X Normal operation. The pointer value calculated in retiming is transmitted. This location is unused. 1 0 The pointer byte values written into these RAM locations by the microprocessor are transmitted. However, retiming is still performed, and the pointer value written into these locations will not affect the starting location of the STS-1 SPE. 1 1 The pointer byte values from the TOH Serial Access Port are transmitted and are also written into these RAM locations. However, retiming is still performed, and the pointer value written into these locations will not affect the starting location of the STS-1 SPE.
14C 167 182	7-0	B21 B22 B23	**Line Parity BIP-24 Error Mask:** These three bytes are assigned to carry a BIP-24. When control bit EXABH (bit 3 in 3E0H) is 0, the three bytes written into these locations by the microprocessor are normally 00H. These RAM locations are exclusive-OR gated with the corresponding internally calculated B2 value. Thus, if a 1 is written into a bit location, the corresponding column is transmitted in error until the microprocessor writes a 0 into the bit location. When control bit EXABH is 1, the error mask for the three bytes is taken from the TOH Serial Access Port. The TOH Serial Access Port bytes are also written into these byte locations for microprocessor access.

Address	Bit	Symbol	Description
14D 14E	7-0	K1 K2	**Automatic Protection Switching (APS) Bytes:** When control bit EXAPS (bit 6 in 3E0H) is set to 0, the microprocessor writes the value of the K1 and K2 bytes to be transmitted into these locations. When EXAPS is set to 1, the K1 and K2 bytes from the TOH Serial Access Port are written into these RAM locations prior to transmission. When enabled by TRLRDI (bit 1 in 3E0H) the SOT-3 conditionally modifies bits 6, 7 and 8 of the K2 byte to 110. See the description of this control register bit for the conditions that cause this modification.
14F 150 151 152 153 154 155 156 157	7-0	D4 D5 D6 D7 D8 D9 D10 D11 D12	**Line Data Communication Channel:** The multiplexing of the nine data communication bytes is controlled by EXDCOW (bit 7 in 3E0H). When EXDCOW is 0, the microprocessor writes the value of the nine bytes to be transmitted into these locations. When EXDCOW is 1, the bytes from the TOH Serial Access Port are written into these RAM locations prior to transmission. The first bit (bit 1) of the SDH/SONET serial byte is written into bit 7.
15A	7-0	E2	**Order Wire Channel**: The multiplexing of the E2 byte is controlled by EXDCOW (bit 7 in 3E0H). When EXDCOW is 0, the microprocessor writes the value of the E2 byte to transmitted into this location. When EXDCOW is 1, the E2 byte from the TOH Serial Access Port is written into this RAM location prior to transmission. The first bit (bit 1) of the SDH/SONET serial byte is written into bit 7.
158 173 18E	7-0	Z11 Z12 Z13	**Growth Bytes:** The multiplexing of the Z1 bytes is controlled by EXF1Z (bit 5 in 3E0H). When EXF1Z is 0 the microprocessor writes the value of the Z1 bytes to be transmitted into these locations. When EXF1Z is 1, the Z1 bytes from the TOH Serial Access Port are written into these RAM locations prior to transmission. The first bit (bit 1) of the SDH/SONET serial byte is written into bit 7.

Address	Bit	Symbol	Description
159 174 18F	7-0	Z21 Z22 Z23	**Growth Bytes and Optional Line FEBE Byte:** The Z21 and Z22 bytes are designated as growth bytes. The Z23 byte may be used to carry a line FEBE count in its last five bits. The line FEBE count is derived from the received B2 bytes. Binary values between 0 and 24 are the only accepted values for a line FEBE count. The line FEBE count is assigned to the bits as shown below: 1 2 3 4 5 6 7 8 Transmitted Z23 byte 7 6 5 4 3 2 1 0 SOT-3 RAM Location 18FH 0 0 0 MSB .. Count .. LSB Content The multiplexing of the Z2n bytes is controlled by three control bits, according to the table below: EXF1Z / Z2FEBE / RING / Action 0 / 0 / 0 — The microprocessor writes the transmitted values for Z21, Z22, and Z23 into these RAM locations. 1 / 0 / 0 — The transmitted values for Z21, Z22, Z23 are taken from the TOH Serial Access Port. These bytes are also written into these RAM locations for microprocessor access. X / 1 / 0 — The transmitted Z23 value is equal to the number of parity errors detected in the received B2 bytes (BIP-24) for the previous frame(s). The SOT-3 will accumulate the actual count received, but will only transmit in the Z23 byte a value of up to 24 at a time. Z21 and Z22 are controlled by EXF1Z, as described above. X / X / 1 — The transmitted Z23 value is the number of parity errors detected in the received B2 bytes from the mate SOT-3 reported via the Alarm Indication Port. The AIP is not limited in the value that it transmits or receives, so a value up to 31 errors could be reported in the five FEBE bits. Z21 and Z22 are controlled by EXF1Z, as described above.
160 17B 175 190	7-0	N3 N4 N5 N6	**National Use:** The multiplexing of these four N bytes is controlled by control bit EXUN (bit 4 in 3E0H). When EXUN is 0, the microprocessor writes the values of the four N bytes to be transmitted into these locations. When EXUN is 1, the four N bytes from the TOH Serial Access Port are written into these RAM locations prior to transmission. The first bit (bit 1) of the SDH/SONET serial byte is written into bit 7. The N1 and N2 bytes are located in 15DH and 178H.

Address	Bit	Symbol	Description
15E 179 15F 161 17C 162	7-0	M1 M2 M3 M4 M5 M6	**Media Specific Use:** The multiplexing of the six M bytes is controlled by EXUN (bit 4 in 3E0H). When EXUN is 0, the microprocessor writes the values of the six M bytes to be transmitted into these locations. When EXUN is 1, the six M bytes from the TOH Serial Access Port are written into these RAM locations prior to transmission. The first bit (bit 1) of the SDH/SONET serial byte is written into bit 7.
17A 17D 163 17E 168 183 169 184 16A 185 16B 186 16C 187 16D 188 16E 189 16F 18A 170 18B 171 18C 172 18D	7-0	U1 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 U26	**Unused Bytes:** The multiplexing of the 26 U bytes is controlled by EXUN (bit 4 in 3E0H). When EXUN is 0, the microprocessor writes the values of the 26 U bytes to be transmitted into these locations. When EXUN is 1, the 26 U bytes from the TOH Serial Access Port are written into these RAM locations prior to transmission. The first bit (bit 1) of the SDH/SONET serial byte is written into bit 7.

Transmit Path Overhead Byte RAM Locations for STM-1 VC-4/STS-3c, STS-3:STS-1 No. 1 (See Note 1)

Address	Bit	Symbol	Description
1C0-1FF	7-0	J11	**Path Trace Message for STM-1 VC-4/STS-3c, STS-3:STS-1 No. 1:** The path trace message is a repetitive 64-byte or 16-byte message. When control bits PTE21 and PTE11 are not equal to 00, the J1 transmitted message is from these RAM locations. When control bit CCITT is 1, four 16-byte messages must be written into four 16-byte RAM segments (1C0H - 1CFH, 1D0H - 1DFH, 1E0H - 1EFH and 1F0H - 1FFH). The starting address for the 64-byte or 16-byte message is arbitrary, unless a sync pulse is applied to the J1SYNC pin or a device reset is applied. When a sync pulse is applied, the starting address will be 1C0H. For a 16-byte message, after one segment is transmitted, the next segment is transmitted. When control bits PTE21 and PT11 are equal to 00, the J1 message bytes transmitted come from the transmit terminal interface. The transmit terminal interface J1 bytes are not written into these RAM locations.
1A8	7-0	B31	**Path BIP-8 Error Mask for STM-1 VC-4/STS-3c, STS-3:STS-1 No. 1:** When control bits PTE21 and PTE11 are not equal to 00, this byte location can be used as an error mask. The byte value written into this location by the microprocessor is normally 00H. This RAM location is exclusive-OR gated with the corresponding internally calculated B3 value. Thus, if a 1 is written into a bit location, the corresponding column is transmitted in error until the microprocessor writes a 0 into the bit location. When control bits PT21 and PTE11 are equal to 00, the transmitted B3 byte comes from the transmit terminal interface and the error mask capability is disabled.
1A9	7-0	C21	**Path Signal Label for STM-1 VC-4/STS-3c, STS-3:STS-1 No. 1:** When control bits PTE21 and PTE11 are not equal to 00, the value written into this RAM location by the microprocessor is transmitted. When control bits PT21 and PTE11 are equal to 00, the transmitted C21 byte comes from the transmit terminal interface. The transmit terminal interface C21 byte is not written into this RAM location.
1AA	7-0	G11	**Path Status Byte for STM-1 VC-4/STS-3c, STS-3:STS-1 No. 1:** When control bits PTE21 and PTE11 are equal to 11, the FEBE and path RDI values written into this RAM location by the microprocessor are transmitted. When the PTE21 and PTE11 bits are not equal to 00, the unassigned bits are transmitted from the RAM location. See Figure 23 for additional information. The RAM bit assignment is shown below: 
1AB	7-0	F21	**Path User Channel for STM-1 VC-4/STS-3c, STS-3:STS-1 No. 1:** When control bits PTE21 and PTE11 are equal to 1X, the value written into this RAM location by the microprocessor is transmitted (the X represents any value). When control bits PT21 and PTE11 are equal to 0X, the transmitted F21 byte comes from the transmit terminal interface. The transmit terminal interface F21 byte is not written into this RAM location.

Address	Bit	Symbol	Description
1AC	7-0	H41	**Multiframe Indicator for STM-1 VC-4/STS-3c, STS-3:STS-1 No. 1:** The H4 byte can carry a multiframe indicator sequence for identifying the location of the V1 byte for VT/TU 1544 or 2048 kbit/s asynchronous mappings. When control bits PTE21 and PTE11 are equal to 10, the H4 value written into this location by the microprocessor is transmitted. For other PTE21 and PTE11 states, in conjunction with the H4INS and STIME control bits, the H4 byte that is transmitted may be from the transmit terminal interface or from an internal H4 multiframe generator. (See H4INS bit description for location 3E4H, bit 3.)
1AD 1AE 1AF	7-0	Z31 Z41 Z51	**Growth Bytes for STM-1 VC-4/STS-3c, STS-3:STS-1 No. 1:** When control bits PTE21 and PTE11 are equal to 1X, the values written into these RAM locations by the microprocessor are transmitted (the X represents any value). When control bits PT21 and PTE11 are equal to 0X, the transmitted bytes come from the transmit terminal interface. The transmit terminal interface bytes are not written into these RAM locations.

Note 1: See Figure 24.

Transmit Path Overhead Byte RAM Locations for STS-3:STS-1 No. 2 (See Note 1)

Address	Bit	Symbol	Description
200- 23F	7-0	J12	**Path Trace Message for STS-3:STS-1 No. 2:** The path trace message is a repetitive 64-byte or 16-byte message. When control bits PTE22 and PTE12 are not equal to 00, the J1 transmitted message is from these RAM locations. When control bit CCITT is 1, four 16-byte messages must be written into four 16-byte RAM segments (200H - 20FH, 210H -21FH, 220H - 22FH and 230H - 23FH). The starting address for the 64-byte or 16-byte message is arbitrary, unless a sync pulse is applied to the J1SYNC pin or a device reset is applied. When a sync pulse is applied, the starting address will be 200H. For a 16-byte message, after one segment is transmitted, the next segment is transmitted. When control bits PTE22 and PT12 are equal to 00, the J1 message bytes transmitted come from the transmit terminal interface. The transmit terminal interface J1 bytes are not written into these RAM locations.
1B0	7-0	B32	**Path BIP-8 Error Mask for STS-3:STS-1 No. 2:** When control bits PTE22 and PTE12 are not equal to 00, this byte location can be used as an error mask. The byte value written into this location by the microprocessor is normally 00H. This RAM location is exclusive-OR gated with the corresponding internally calculated B3 value. Thus, if a 1 is written into a bit location, the corresponding column is transmitted in error until the microprocessor writes a 0 into the bit location. When control bits PT22 and PTE12 are equal to 00, the transmitted B3 byte comes from the transmit terminal interface and the error mask capability is disabled.

Address	Bit	Symbol	Description
1B1	7-0	C22	**Path Signal Label for STS-3:STS-1 No. 2:** When control bits PTE22 and PTE12 are not equal to 00, the value written into this RAM location by the microprocessor is transmitted. When control bits PT22 and PTE12 are equal to 00, the transmitted C22 byte comes from the transmit terminal interface. The transmit terminal interface C22 byte is not written into this RAM location.
1B2	7-0	G12	**Path Status Byte for STS-3:STS-1 No. 2:** When control bits PTE22 and PTE12 are equal to 11, the FEBE and path RDI values written into this RAM location by the microprocessor are transmitted. When the PTE22 and PTE12 bits are not equal to 00, the unassigned bits are transmitted from the RAM location. See Figure 23 for additional information. The RAM bit assignment is shown below: 1 2 3 4 5 6 7 8 Received G1 byte 7 6 5 4 3 2 1 0 RAM location FEBE | RDI | Unassigned
1B3	7-0	F22	**Path User Channel for STS-3:STS-1 No. 2:** When control bits PTE22 and PTE12 are equal to 1X, the value written into this RAM location by the microprocessor is transmitted (the X represents any value). When control bits PT22 and PTE12 are equal to 0X, the transmitted F22 byte comes from the transmit terminal interface. The transmit terminal interface F22 byte is not written into this RAM location.
1B4	7-0	H42	**Multiframe Indicator for STS-3:STS-1 No. 2:** The H4 byte can carry a multiframe indicator sequence for identifying the location of the V1 byte for VT/TU 1544 or 2048 kbit/s asynchronous mappings. When control bits PTE22 and PTE12 are equal to 10, the H4 value written into this location by the microprocessor is transmitted. For other PTE22 and PTE12 states, in conjunction with the H4INS and STIME control bits, the H4 byte that is transmitted may be from the transmit terminal interface or from an internal H4 multiframe generator. (See H4INS bit description for location 3E4H, bit 3)
1B5 1B6 1B7	7-0	Z32 Z42 Z52	**Growth Bytes for STS-3:STS-1 No. 2:** When control bits PTE22 and PTE12 are equal to 1X, the values written into these RAM locations by the microprocessor are transmitted (the X represents any value). When control bits PT22 and PTE12 are equal to 0X, the transmitted bytes come from the transmit terminal interface. The transmit terminal interface bytes are not written into these RAM locations.

Note 1: These bytes are unused for STM-1/STS-3c. See Figure 24.

Transmit Path Overhead Byte RAM Locations for STS-3:STS-1 No. 3 (See Note 1)

Address	Bit	Symbol	Description
240-27F	7-0	J13	**Path Trace Message for STS-3:STS-1 No. 3:** The path trace message is a repetitive 64-byte or 16-byte message. When control bits PTE23 and PTE13 are not equal to 00, the J1 transmitted message is from these RAM locations. When control bit CCITT is 1, four 16-byte messages must be written into four 16-byte RAM segments (240H - 24FH, 250H -25FH, 260H - 26FH and 270H - 27FH). The starting address for the 64-byte or 16-byte message is arbitrary, unless a sync pulse is applied to the J1SYNC pin or a device reset is applied. When a sync pulse is applied, the starting address will be 240H. For a 16-byte message, after one segment is transmitted, the next segment is transmitted. When control bits PTE23 and PT13 are equal to 00, the J1 message bytes transmitted come from the transmit terminal interface. The transmit terminal interface J1 bytes are not written into these RAM locations.
1B8	7-0	B33	**Path BIP-8 Error Mask for STS-3:STS-1 No. 3:** When control bits PTE23 and PTE13 are not equal to 00, this byte location can be used as an error mask. The byte value written into this location by the microprocessor is normally 00H. This RAM location is exclusive-OR gated with the corresponding internally calculated B3 value. Thus, if a 1 is written into a bit location, the corresponding column is transmitted in error until the microprocessor writes a 0 into the bit location. When control bits PT23 and PTE13 are equal to 00, the transmitted B3 byte comes from the transmit terminal interface and the error mask capability is disabled.
1B9	7-0	C23	**Path Signal Label for STS-3:STS-1 No. 3:** When control bits PTE23 and PTE13 are not equal to 00, the value written into this RAM location by the microprocessor is transmitted. When control bits PT23 and PTE13 are equal to 00, the transmitted C23 byte comes from the transmit terminal interface. The transmit terminal interface C23 byte is not written into this RAM location.
1BA	7-0	G13	**Path Status Byte for STS-3:STS-1 No. 3:** When control bits PTE23 and PTE13 are equal to 11, the FEBE and path RDI values written into this RAM location by the microprocessor are transmitted. When the PTE23 and PTE13 bits are not equal to 00, the unassigned bits are transmitted from the RAM location. See Figure 23 for additional information. The RAM bit assignment is shown below: 1 2 3 4 5 6 7 8 Received G1 byte 7 6 5 4 3 2 1 0 RAM location FEBE | RDI | Unassigned
1BB	7-0	F23	**Path User Channel for STS-3:STS-1 No. 3:** When control bits PTE23 and PTE13 are equal to 1X, the value written into this RAM location by the microprocessor is transmitted (the X represents any value). When control bits PT23 and PTE13 are equal to 0X, the transmitted F23 byte comes from the transmit terminal interface. The transmit terminal interface F23 byte is not written into this RAM location.

Address	Bit	Symbol	Description
1BC	7-0	H43	**Multiframe Indicator for STS-3:STS-1 No. 3:** The H4 byte can carry a multiframe indicator sequence for identifying the location of the V1 byte for VT/TU 1544 or 2048 kbit/s asynchronous mappings. When control bits PTE23 and PTE13 are equal to 10, the H4 value written into this location by the microprocessor is transmitted. For other PTE23 and PTE13 states, in conjunction with the H4INS and STIME control bits, the H4 byte that is transmitted may be from the transmit terminal interface or from an internal H4 multiframe generator. (See H4INS bit description for location 3E4H, bit 3.)
1BD 1BE 1BF	7-0	Z33 Z43 Z53	**Growth Bytes for STS-3:STS-1 No. 3:** When control bits PTE23 and PTE13 are equal to 1X, the values written into these RAM locations by the microprocessor are transmitted (the X represents any value). When control bits PT23 and PTE13 are equal to 0X, the transmitted bytes come from the transmit terminal interface. The transmit terminal interface bytes are not written into these RAM locations.

Note 1: These bytes are unused for STM-1/STS-3c. See Figure 24

CONTROL REGISTER DESCRIPTIONS

Control Register 0

Address	Bit	Symbol	Description
3E0	7	EXDCOW	**External Data Communication and Orderwire Byte Select:** A 1 enables the transmit TOH RAM locations for data communication bytes (D1-D12) and orderwire bytes (E1-E2) to be written by the TOH Serial Access Port once every 125 microseconds. See Note 1. A 0 enables the transmit TOH RAM locations D1-D12 and E1-E2 to be written by the microprocessor.
	6	EXAPS	**External APS Byte Select:** A 1 enables the transmit TOH RAM locations for APS bytes (K1-K2) to be written by the TOH Serial Access Port once every 125 microseconds. See Note 1. A 0 enables the transmit TOH RAM locations K1-K2 to be written by the microprocessor.
	5	EXF1Z	**External F1, C1 and Z Byte Select:** A 1 enables the transmit TOH RAM locations for the F1, three C1n (n=1-3) and six Zmn (m=1-2) bytes to be written by the TOH Serial Access Port once every 125 microseconds. See Note 1. A 0 enables the transmit TOH RAM locations for the F1, C1n and Zmn bytes to be written by the microprocessor.
	4	EXUN	**External Unused Byte Select:** A 1 enables the transmit TOH RAM locations for the National Use (N3-N6), Media Specific Use (M1-M6) and Unused (U1-U26) bytes to be written by the TOH Serial Access Port once every 125 microseconds. These bytes should be initialized by the microprocessor when EXUN is set to 0. See Note 1. A 0 enables the transmit TOH RAM locations for the N, M and U bytes to be written by the microprocessor.

Note 1: Refer to the STM-1/STS-3/STS-3c Transmit Overhead Byte RAM Locations table in the Memory Map for RAM Locations section. The microprocessor is not prohibited from writing to these locations when the control bit is 1.

Address	Bit	Symbol	Description
3E0 (cont.)	3	EXABH	**External A1, A2, B1, B2, H1, H2 and H3 Byte Select:** This bit controls whether the Transmit TOH RAM locations for the A1, A2, B1, B2, H1, H2 and H3 bytes are written by the TOH Serial Access Port once every 125 microseconds (when EXABH is 1) or by the microprocessor (when EXABH is 0). See Note 1. This control bit works in conjunction with the TLA1A2E and TRPTR control bits for controlling the multiplexing of the A1 and A2 bytes, and the H1 and H2 pointer bytes, towards the line. The following table indicates the controls for the A1 and A2 bytes: EXABH / TLA1A2E / Action 0 / 0 / Internally generated A1 and A2 bytes transmitted (F6H for A1 and 28H for A2). 0 / 1 / Microprocessor-written A1 and A2 bytes transmitted. 1 / X / TOH Serial Access Port A1 and A2 bytes are written to RAM, and transmitted. When EXABH is 1, the Transmit TOH RAM locations for the B1 and B2 bytes are written by the TOH Serial Access Port. The contents of the B1 and B2 bytes are used as masks. The B1 byte in RAM is transmitted directly for use as a B1 mask by the connected SYN155. For B2, the actual transmitted byte is the calculated BIP-8 parity, exclusive-OR gated with the content of the B2 byte in RAM. When EXABH is 0, the B1 and B2 bytes are written by the microprocessor. The following table indicates the controls associated with the H1and H2 bytes: EXABH / TRPTR / Action 0 / 0 / H1 and H2 are recalculated according to their payload location, and transmitted. 0 / 1 / Microprocessor-written H1 and H2 bytes are transmitted. See Note 1. 1 / 0 / H1 and H2 are recalculated according to their payload location, and transmitted. However, the TOH Serial Access Port H1 and H2 bytes are written into RAM locations for microprocessor access. 1 / 1 / The TOH Access port H1 and H2 bytes are written into RAM and are also transmitted. See Note 1.

Note 1: The transmitted value will have no effect on the location of the payload, which is recalculated based on the reference clock and framing pulse.

Address	Bit	Symbol	Description
3E0 (cont.)	2	TRPAISE	**Transmit Path AIS Enable:** A 1 enables local alarms or the microprocessor to generate and transmit path AIS for the VC-4 and STS-1 signals. Path AIS is defined as all ones in the pointer bytes (H1 and H2), and ones in the SPE (POH bytes and payload bytes). See Note 1 for additional detail. A 0 disables the introduction of path AIS by the local alarms and the microprocessor. Path AIS is disabled when an Unequipped status is enabled by writing a 1 to control bit UNEQn. The following conditions enable a path AIS, when TRPAISE is 1. The n designates the STS-3:STS-1 number, and for a VC-4/STS-3c, n is 1. - When a 1 is written to the TAISn control bit (n is 1, 2 or 3) - A Transmit Loss Of Signal alarm (TLOS) - A Transmit Loss Of Clock alarm (TLOC) - When a high is placed on the TXAISn pin - When enabled by writing a 1 to control bit E12AIS (bit 6 in 3E3H) and a majority of ones is detected in the E1n byte at the terminal interface.
	1	TRLRDI	**Transmit Line RDI Control:** A 1 enables internal alarms to generate a Line RDI. Line RDI is defined as 110 in bits 6, 7 and 8 of the K2 byte. A 0 enables the RAM location content for bits 6, 7 and 8 of the K2 byte to be transmitted. The following conditions generate and transmit a Line RDI when this bit is 1: - A Receive Loss Of Signal (RLOS) alarm, when the RING bit is 0. - A Receive Loss Of frame (RLOF) alarm, when the RING bit is 0. - A Receive Loss Of Clock (RLOC) alarm, when the RING bit is 0. - A Receive Line AIS (RLAIS) alarm, when the RING bit is 0. - Alarm Indication Port RDI Indication in bit 38, when the RING bit is 1 (see Figure 25).
	0	TRLAISE	**Transmit Line AIS Enable:** A 1 enables local alarms or the microprocessor to generate and transmit a line AIS. Line AIS is defined as all ones in the TOH bytes, except the A1, A2, C1, B1, E1, F1, and D1-D3 bytes, and SPE (VC-4 or STS-1 signals). A 1 also overrides control bit TRPAISE. A 0 disables the introduction of line AIS by the local alarms and the microprocessor. Line AIS overrides an Unequipped status when it is enabled by writing a 1 to control bit UNEQn. See Note 1. The following conditions enable a line AIS, when TRLAISE is 1: - When a 1 is written to control bit TAIS1 - A Transmit Loss Of Signal alarm (TLOS) - A Transmit Loss Of Clock alarm (TLOC) - When a high is placed on the TXAIS1 pin - When enabled by writing a 1 to control bit E12AIS (bit 6 in 3E3H), and a majority of ones is detected in the transmit terminal E11 byte.

Note 1: During a path AIS condition, the H1, H2 pointer bytes for the path are set to FFFFH. During a line AIS condition, all three H1, H2 byte pairs are set to FFFFH, overriding any individual path indications. When exit from a line and/or path condition causes an H1, H2 byte pair to leave the FFFFH state, then a New Data Flag (NDF=1001) is sent in byte H1 with the first new pointer (9NNNH) and a normal NDF (0110) is sent with subsequent repetitions of this new pointer (6NNNH), where the first pointer number nibble (N) includes the two ss-bits.

Control Register 1

Address	Bit	Symbol	Description
3E1	7	RTLOOP	**Terminal Side Receive-to-Transmit Loopback Enable:** A 1 disables the terminal data input (TTDI) signals, and enables the receive terminal output clock, data, SPE, and C1J1 signals to be internally connected to the transmit input. The receive terminal output signals are provided while this loopback is enabled. This control is not valid when the data communication or source timing operating mode is selected.
	6	TAIS1	**Transmit AIS for STM-1 AU-4/STS-3c or STS-3:STS-1 No. 1:** A 1 written into this bit position generates a transmit path AIS for STM-1 AU-4/STS-3c, or STS-3:STS-1 No. 1, when control bit TRPAISE is 1. When control bit TRLAISE is 1, a 1 written into this bit generates and transmits a line AIS. Line AIS overrides the generation of path AIS. The states associated with these three control bits are described in the table below: TAIS1 / TRLAISE / TRPAISE / Action X / 0 / 0 / The generation of transmit path AIS or line AIS is disabled for STM-1 AU-4/STS-3c or STS-3: STS-1 No. 1. 0 / 0 / 1 / The generation of transmit path AIS is enabled for STM-1 AU-4/STS-3c or STS-3: STS-1 No. 1. Path AIS is generated when a transmit alarm occurs (see TRPAISE above). 0 / 1 / X / The generation of transmit line AIS is enabled for STM-1 AU-4/STS-3c or STS-3: STS-1 No. 1. Line AIS is generated when a transmit alarm occurs (see TRLAISE above). 1 / 0 / 1 / Transmit path AIS is generated for STM-1 AU-4/STS-3c or STS-3: STS-1 No. 1. 1 / 1 / X / Transmit line AIS is generated for STM-1 AU-4/STS-3c or STS-3: STS-1 No. 1.
	5	CCITT	**CCITT Control Bit:** A 1 enables the AIS to LOP transition in the pointer tracking state machine, the ss-bits (fifth and sixth) in the H1 byte to be checked, the receive terminal output ss-bits and the transmit line output ss-bits in the H1 byte to be set to 10, and path RDI detection and recovery to be based on five consecutive events. See Note 1.

Note 1: The former CCITT organization is now known as ITU-T (see Standards Documentation Sources section).

Address	Bit	Symbol	Description
3E1 (cont.)	4 3	PTE21 PTE11	**Path Termination Mode Control for STM-1 VC-4/STS-3c or STS-3:** **STS-1 No. 1:** These two control bits determine the multiplexing (termination) of the path overhead bytes for the STM-1 VC-4/STS-3c or STS-3:STS-1 No. 1 transmit (receive) paths, according to the following table, assuming normal operation (DATACOM pin is low). See also Figures 23 and 24. They also control the transmission of VTAIS1, as shown in Figure 18. PTE21 PTE11 Action 0 0 The nine overhead bytes are transmitted intact from the terminal interface without processing. The ability to insert path FEBE and RDI, and have the SOT-3 function in the ring mode, is disabled. Receive side is not terminated. 0 1 J1 message transmitted from RAM. B3 BIP-8 value calculated internally. C2 byte transmitted from RAM. G1 FEBE value from received BIP-8 and RDI controlled by local alarms when RING control bit is 0. When RING or PCROS1 is 1, FEBE and RDI are controlled by mate SOT-3 using the Alarm Indication Port (see Figure 23). Bits 2, 1 and 0 of byte are from RAM. F2, Z3, Z4 and Z5 bytes taken from terminal side. H4 byte from the terminal interface when H4INS bit is 0 or from multiframe generator when H4INS is 1. H4 multiframe generator locked to terminal side V1 pulse when H4INS is 1. Receive side path termination enabled. 1 0 J1 message transmitted from RAM. B3 BIP-8 value calculated internally. C2 byte transmitted from RAM. G1 FEBE value from received BIP-8 and RDI controlled by local alarms when RING control bit is 0. When RING or PCROS1 is 1, FEBE and RDI controlled by mate SOT-3 using the Alarm Indication Port (see Figure 23). Bits 2, 1 and 0 are from RAM. F2, Z3, Z4 and Z5 bytes transmitted from RAM. H4 RAM value transmitted. Receive side path termination enabled. 1 1 J1 message transmitted from RAM. B3 BIP-8 value calculated internally. C2 byte transmitted from RAM. G1 byte transmitted from RAM. RING and PCROS1 control bits disabled. F2, Z3, Z4 and Z5 bytes transmitted from RAM. H4 byte from terminal interface when H4INS bit is 0 or multiframe generator when H4INS is 1. H4 multiframe generator locked to terminal side V1 pulse when H4INS is 1. Receive side path termination enabled.
	2	RING	**Ring Mode Enable:** A 1 enables the FEBE count and the RDI state in the G1 byte to be controlled by the mate SOT-3 via the Alarm Indication Port interface. A 0 enables the local FEBE count and enables local alarms to control the RDI state. The ring mode is disabled when operating in data communication or source timing modes. The RING bit is disabled from G1n byte multiplexing when PTE2n and PTE1n are either 00 or 11 (where n=1-3). See Figure 23.

Address	Bit	Symbol	Description
3E1 (cont.)	1	RAISE	**Receive AIS Enable**: This bit works in conjunction with control bits PAISE and SRAISn, and pin MODE0, according to the following table. The n represents the STS-3:STS-1 number (n=1-3). For a VC-4/STS-3c format, n is equal to 1. Pin MODE0 is low for all rows of the table. RAISE / PAISE / SRAISn / Action 0 / 0 / 0 / No AIS generation on local alarms, E1n bytes are 00H. 0 / 0 / 1 / No AIS generation on local alarms, E1n bytes are FFH. 0 / 1 / 0 / No AIS generation on local alarms, E1n bytes provide detailed alarm status information. See Figure 20. 0 / 1 / 1 / No AIS generation on local alarms, E1n bytes are FFH. 1 / 0 / 0 / VTAIS generated for local alarms. VTAIS consists of N20AH (522 Decimal) in the H1 and H2 bytes, zeros in the H3 byte, and ones in entire payload, including the POH bytes, except for the H4 byte (where N is the NDF nibble). When VTAIS is released, NDF is sent once, followed by a normal pointer (same if no pointer movement took place). E1n bytes provide detailed alarm status information. See Figure 20. 1 / 0 / 1 / VTAIS sent, E1n bytes equal to FFH. 1 / 1 / 0 / Path AIS generated for local alarms. Path AIS consists of FFH in the H1, H2 and H3 bytes, and ones in entire payload, including the POH bytes. When path AIS is released, NDF is sent once, followed by a normal pointer (same if no pointer movement took place). E1n bytes provide detailed alarm status information. See Figure 20. 1 / 1 / 1 / Path AIS sent, E1n bytes are FFH.
	0	TRLOOP	**Line Side Transmit-to-Receive Loopback Enable:** A 1 disables the line side receive data and clock input signals, and enables the transmit line clock and data output signals to be internally connected to the receive line input. The transmit line output signals are provided while this loopback is enabled.

Control Register 2

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="4">3E2</td><td>7</td><td>TLB</td><td>External Terminal Loopback Output Control: This bit is provided for controlling the Terminal Loopback feature in the SYN155 via the SOT-3. A 1 causes a high to be generated at the TLB pin, while a 0 causes a low to generated at the TLB pin.</td></tr>
<tr><td>6
5
4</td><td>TCAT3
TCAT2
TCAT1</td><td>Terminal Side Concatenation Mode Controls: The following are valid states of the TCATn bits, where n=1-3. (See Note 1, below):
<table><tr><th>Operating Mode</th><th>TCAT3</th><th>TCAT2</th><th>TCAT1</th></tr><tr><td>STM-1 AU-4/STS-3c</td><td>1</td><td>1</td><td>0</td></tr><tr><td>STM-1 AU-3/STS-3</td><td>0</td><td>0</td><td>0</td></tr></table>Other combinations of the TCATn bits are not supported.</td></tr>
<tr><td>3</td><td>FLB</td><td>External Facility Loopback Output Control: This bit is provided for controlling the Facility Loopback feature in the SYN155 via the SOT-3. A 1 causes a high to be generated at the FLB pin, while a 0 causes a low to generated at the FLB pin.</td></tr>
<tr><td>2
1
0</td><td>LCAT3
LCAT2
LCAT1</td><td>Line Side Concatenation Mode Controls: The following are valid states of the LCATn bits, where n=1-3. (See Note 1, below):
<table><tr><th>Operating Mode</th><th>LCAT3</th><th>LCAT2</th><th>LCAT1</th></tr><tr><td>STM-1 AU-4/STS-3c</td><td>1</td><td>1</td><td>0</td></tr><tr><td>STM-1 AU-3/STS-3</td><td>0</td><td>0</td><td>0</td></tr></table>Other combinations of the LCATn bits are not supported.</td></tr>
</table>

Note 1: The TCATn and LCATn control bits must be programmed for the same operating mode.

Control Register 3

Address	Bit	Symbol	Description
3E3	7	TRPTR	**Transmit Pointer Control:** This control bit works in conjunction with control bit EXABH for controlling the transmitted H1, H2 and H3 bytes. A table describing the effects of the four possible states is shown in the EXABH control bit description.
	6	E12AIS	**Terminal E1n Byte AIS Control:** A 1 enables transmit path AIS for an AU-3/STS-1 signal to be generated when control bit TRPAISE is 1 and a majority of ones is detected in the terminal side E1n byte. Line AIS is generated when control bit TRLAISE is 1 and a majority of ones is detected in the E1n byte. The n notation corresponds to the STS-1 number (n=1-3). A 0 disables the generation of either path AIS or line AIS when the E1n byte is carrying a majority of ones.

Address	Bit	Symbol	Description
3E3 (cont.)	5	TPRDI1	**Transmit Path RDI Enable for STM-1/STS-3c VC-4 or STS-3:STS-1 No. 1:** A 1 enables Path RDI (Bit 5 in G1 is 1) to be generated for the STM-1/STS-3c VC-4 signal or STS-3:STS-1 No. 1 signal for any of the following conditions (see Figure 23): When RING and PCROS1 are 0, and PTE21, PTE11 are 01, 10 or 11 with - Loss Of Signal (RLOS) when bit RAISE is 1 - Loss Of Frame (RLOF) when bit RAISE is 1 - Loss Of Clock (RLOC) when bit RAISE is 1 - Loss Of Pointer(RLOP1)when bit RAISE is 1 - Line AIS (RLAIS) (generated for the three STS-1s) when bit RAISE is 1 - Low on AIS pin ($\overline{\text{FAIS1}}$) when bit RAISE is 1 - C2 Mismatch (C2MM1) when bit RAISE is 1 - Unequipped Status (UNEQ1) when bit RAISE is 1 - Loss of Multiframe (RLOM1) when bits LM2AIS and RAISE are 1 - Path AIS (RPAIS1) when bit RAISE is 1 - Bit 5 in G11 RAM location (1AAH) is a 1 When RING or PCROS1 is 1, and PTE21, PTE11 are 01, 10 or 11 with - Alarm Indication Port (bit 39) RDI from mate SOT-3 Control bit TPRDI1 is disabled when PTE21, PTE11 are 00, and RDI is controlled via the G1 byte from the transmit terminal interface.
	4	FRENB	**FIFO Reset Enable:** A 1 enables the transmit and receive FIFOs to reset automatically upon underflow or overflow. The receive or transmit data path may be corrupted for a minimum of one frame and a maximum of two frames.
	3	LM2AIS	**Loss Of Multiframe to AIS Generation Control:** A 1 enables a receive loss of multiframe (RLOMn) alarm to generate an internal VTAIS or path AIS, and RDI. A 0 disables the generation of VTAIS or path AIS, and RDI, on loss of multiframe.
	2	SRAIS1	**Send Receive Internal VTAIS or Path AIS for STM-1/STS-3c VC-4 or STS-3:STS-1 No. 1:** A 1 causes VTAIS or path AIS (and path RDI) to be generated for the STM-1/STS-3c VC-4 or STS-3:STS-1 No. 1 when control bit RAISE is 1. Setting this bit can cause pointer movements at the receive terminal interface.
	1	FIFORST	**Receive and Transmit FIFO Reset:** A 1 resets both the receive and transmit FIFOs to approximately the half-full condition. This bit must then be written with a 0 to release the FIFO for operation.
	0	Reserved	This bit must be set to zero.

Control Register 4

Address	Bit	Symbol	Description
3E4	7	RTA1A2E	**Receive Terminal A1, A2 Enable:** A 1 enables the microprocessor-written framing pattern in locations 3EBH (RTA1) and 3ECH (RTA2) to be sent as the A1 and A2 bytes to the receive terminal interface. A 0 forces A1 to F6H and A2 to 28H.
	6	Z2FEBE	**Z2 FEBE Enable:** This bit works in conjunction with the EXF1Z control bit. Assuming that the RING bit is 0, the following are the possible states: EXF1Z / Z2FEBE / Action 0 / 0 / The microprocessor writes the Z23 byte to be transmitted. 1 / 0 / TOH Serial Access Port Z23 byte is written into RAM (location 18FH) and transmitted. X / 1 / The Z23 byte is used for transmitting a line FEBE count. The value sent in Z23 is equal to the number of bits found to be in error for the received bytes (BIP-24) for the previous frame. The error count (from 0 to 24) is inserted into bits 4 (MSB) through 8 (LSB). Only the values of 0 through 24 are valid. Other values are counted as 0 errors. Bits 1 through 3 are transmitted as zero. For example, a count of 24 is transmitted as 0001 1000. When the RING bit is 1, the FEBE value is taken from the Alarm Indication Port (see Figures 23 and 25). The AIP is not limited in the value that it transmits or receives, so a value up to 31 errors could be reported in the five FEBE bits.
	5	PDAT	**Parity Check Over Transmit Terminal Data Only Enable:** This bit works in conjunction with the TPLEV control bit for checking incoming terminal parity. It is valid only in the normal mode. It is ignored in the data communication and source timing modes. The following states are possible: PDAT / TPLEV / Action 0 / 1 / Even parity checked over the terminal side byte data (TTDI(7-0)), the C1J1 indication (TC1J1), and SPE indication (TSPE). 0 / 0 / Odd parity checked over the terminal side byte data (TTDI(7-0)), the C1J1 indication (TC1J1), and SPE indication (TSPE). 1 / 1 / Even parity checked over the terminal side byte data (TTDI(7-0)) only. 1 / 0 / Odd parity checked over the terminal side byte data (TTDI(7-0)) only.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>3E4
(cont.)</td><td>4</td><td>TPLEV</td><td>Bus Parity Even/Odd Selection: A 1 enables even bus parity to be generated for the terminal output signals (RTDO(7-0), RC1J1, and RSPE). A 0 enables odd bus parity to be generated for these signals. In the transmit direction, TPLEV works in conjunction with the PDAT control bit as described above. In the receive direction, TPLEV works in conjunction with the RDPAR Receive Data Parity Mode Selector bit, as described below for that bit.</td></tr>
<tr><td></td><td>3</td><td>H4INS</td><td>Transmit H4 Byte Insert Control: Enabled when control bits PTE2n, PTE1n are equal to 01 or 11. The n designates the STS-3:STS-1 number (n=1-3), and n is equal to 1 for an STM-1/STS-3c. Disabled when PTE2n, PTE1n are equal to 00 or 10. H4INS works in conjunction with the STIME (source timing mode) control bit and the PTE2n and PTE1n control bits according to the following tables (see also Figure 24):

Normal operation (DATACOM pin is low):

<table>
<tr><th>H4INS</th><th>STIME</th><th>PTE2n/PTE1n</th><th>Action</th></tr>
<tr><td>X</td><td>X</td><td>00</td><td>Terminal side H4 byte transmitted.</td></tr>
<tr><td>X</td><td>X</td><td>10</td><td>H4 byte transmitted from RAM.</td></tr>
<tr><td>0</td><td>X</td><td>01 or 11</td><td>Terminal side H4 byte transmitted.</td></tr>
<tr><td>1</td><td>X</td><td>01 or 11</td><td>Transmitted H4 byte is from the multiframe generator. The multiframe generator is synchronized to the V1 pulse, which is present in the TC1J1 signal from the terminal interface.</td></tr>
</table>

Data communication or source timing mode (DATACOM pin is high):

<table>
<tr><th>H4INS</th><th>STIME</th><th>PTE2n/PTE1n</th><th>Action</th></tr>
<tr><td>X</td><td>0</td><td>XX</td><td>Data communication mode. H4 byte transmitted from RAM.
Source timing mode:</td></tr>
<tr><td>X</td><td>1</td><td>00</td><td>Terminal side H4 byte transmitted.</td></tr>
<tr><td>X</td><td>1</td><td>10</td><td>H4 byte transmitted from RAM.</td></tr>
<tr><td>0</td><td>1</td><td>01 or 11</td><td>Terminal side H4 byte transmitted.</td></tr>
<tr><td>1</td><td>1</td><td>01 or 11</td><td>Transmitted H4 byte is from the multiframe generator. The multiframe generator also generates the V1 pulse for the terminal TC1J1 output signal. This enables add/drop multiplexer devices to synchronize and insert the V1 byte in the proper time slot based on the H4 byte value.</td></tr>
</table>
</td></tr>
</table>

Address	Bit	Symbol	Description
3E4 (cont.)	2	PAISE	**Path AIS Enable:** This bit works in conjunction with control bits RAISE and SRAISn, and pin MODE0, according to the following table. The n represents the STS-3:STS-1 number (n=1-3). For a VC-4/STS-3c format, n is equal to 1. Pin MODE0 is low for all rows of the table.

RAISE	PAISE	SRAISn	Action
0	0	0	No AIS generation on local alarms, E1n bytes are 00H.
0	0	1	No AIS generation on local alarms, E1n bytes are FFH.
0	1	0	No AIS generation on local alarms, E1n bytes provide detailed alarm status information. See Figure 20.
0	1	1	No AIS generation on local alarms, E1n bytes are FFH.
1	0	0	VTAIS generated for local alarms. VTAIS consists of N20AH (522 Decimal) in the H1 and H2 bytes, zeros in the H3 byte, and ones in entire payload, including the POH bytes, except for the H4 byte (N is the NDF nibble). When VTAIS is released, NDF is sent once, followed by a normal pointer (same if no pointer movement took place). E1n bytes provide detailed alarm status information. See Figure 20.
1	0	1	VTAIS sent, E1n bytes are FFH.
1	1	0	Path AIS generated for local alarms. Path AIS consists of FFH in the H1, H2 and H3 bytes, and ones in entire payload, including the POH bytes. When Path AIS is released, NDF is sent once, followed by a normal pointer (same if no pointer movement took place). E1n bytes provide detailed alarm status information. See Figure 20.
1	1	1	Path AIS sent, E1n bytes are FFH.

Address	Bit	Symbol	Description
3E4 (cont.)	1	RV1EN	**Receive V1 Pulse Enable**: A 1 applied when control bit ELOMn is 1 enables the insertion of the V1 pulse into the receive terminal side C1J1 signal to form the signal C1J1V1 (n=1-3 represents the STS3:STS-1 number, or n=1 for a VC-4/STS-3c format). The C1J1V1 signal is used in conjunction with the SPE signal to determine the location of the various pulses, as shown in Figure 22. The C1 pulse identifies the location of the C1 byte when the SPE signal is low. A single J1 pulse identifies the starting location of the J1 byte in the STM-1/STS-3c VC-4 format, when the SPE signal is high. Three J1 pulses are provided for the AU-3/STS-3 format, each identifying the starting location of the J1 byte in the AU-3/STS-1. For STM-1 VC-4 operation, a single V1 pulse occurs three clock cycles after the J1 pulse, once every four frames. For the STS-3:STS-1 AU-3 format, three V1 pulses will be present. Each V1 pulse will be present three clock cycles after the corresponding J1 pulse, when the SPE signal is high. For example, in a VC-4 signal, the J1 pulse identifies the J1 byte location (defined as the starting location for the VC-4) in the POH bytes. In the next column (first clock cycle), all the rows are assigned as fixed stuff. Similarly, in the next column (second clock cycle), all the rows are assigned as fixed stuff. The next column (third clock cycle) defines the start of TUG-3 “A”. This column is where the V1 pulse occurs once every four frames. However, the actual V1 byte will occur six clock cycles after the V1 pulse.
	0	BLOCK	**Block/Bit Counter Mode Selection:** A 1 configures the B1, B2, B3, and path FEBE performance counters to increment by one for any number of bit errors detected (block mode). A 0 configures the counter to increment by the actual number of bit errors detected (bit mode).

Control Register 5

Address	Bit	Symbol	Description
3E5	7	TLA1A2E	**Transmit Line A1, A2 Enable:** This bit works in conjunction with the EXABH control bit according to the following table: TLA1A2E / EXABH / Action 0 / 0 / Internal F6H and 28H pattern transmitted for A1 and A2. 1 / 0 / Microprocessor-written A1, A2 values are transmitted. A11 is in 140H, A12 is in 15BH, A13 is in 176H, A21 is in 141H, A22 is in 15CH, A23 is in 177H. X / 1 / A1 and A2 bytes from the TOH Serial Access Port are written to RAM, and transmitted.
	6	PCROS3	**G1 Path Cross Over Ring Operation for STS-3:STS-1 No. 3:** Enabled when control bits PTE23, PTE13 are equal to 01 or 10. Disabled when control bits PTE23, PTE13 are equal to 00 or 11. PCROS3 is disabled in data communication mode. See Figure 23 (Note: This bit should be set to 0 when the SOT-3 device is configured for STS-3c mode.) This bit works in conjunction with the RING control bit according to the following table: PCROS3 / RING / Action 0 / 0 / Transmitted line FEBE count and the RDI state in the G1 byte are controlled by receive side BIP-8 error count and local alarms for STS-3:STS-1 No. 3. 1 / 0 / Transmitted line FEBE count and the RDI state for STS-3:STS-1 No. 3 are controlled by the mate SOT-3 via the Alarm Indication Port. X / 1 / Global Ring operation. The VC-4 or the three STS-1 FEBE counts and RDI states are controlled by the mate SOT-3 via the Alarm Indication Port.
	5	PCROS2	**G1 Path Cross Over Ring Operation for STS-3:STS-1 No. 2:** Enabled when control bits PTE22, PTE12 are equal to 01 or 10. Disabled when control bits PTE22, PTE12 are equal to 00 or 11. PCROS2 is disabled in data communication mode. See Figure 23. (Note: This bit should be set to 0 when the SOT-3 device is configured for STS-3c mode.) This bit works in conjunction with the RING bit according to the following table: PCROS2 / RING / Action 0 / 0 / Transmitted line FEBE count and the RDI state in the G1 byte are controlled by receive side BIP-8 error count and local alarms for the STS-3:STS-1 No. 2. 1 / 0 / Transmitted line FEBE count and the RDI state for the STS-3:STS-1 No. 2 are controlled by the mate SOT-3 via the Alarm Indication Port. X / 1 / Global Ring operation. The VC-4 or the three STS-1 FEBE counts and RDI states are controlled by the mate SOT-3 via the Alarm Indication Port.

Address	Bit	Symbol	Description
3E5 (cont.)	4	PCROS1	**G1 Path Cross Over Ring Operation for STM-1 VC-4 or STS-3:STS-1 No. 1:** Enabled when control bits PTE21, PTE11 are equal to 01 or 10. Disabled when control bits PTE21, PTE11 are equal to 00 or 11. PCROS1 is disabled in data communication mode. See Figure 23. (Note: This bit should be set to 0 when the SOT-3 device is configured for STS-3c mode.) This bit works in conjunction with the RING bit according to the following table: PCROS1 / RING / Action 0 / 0 / Transmitted line FEBE count and the RDI state in the G1 byte are controlled by receive side BIP-8 error count and local alarms for the STM-1 VC-4 or STS-3:STS-1 No. 1. 1 / 0 / Transmitted line FEBE count and the RDI state for the STM-1 VC-4 or STS-3:STS-1 No. 1 are controlled by the mate SOT-3 via the Alarm Indication Port. X / 1 / Global Ring operation. The VC-4 or the three STS-1 FEBE counts and RDI states are controlled by the mate SOT-3 via the Alarm Indication Port.

Address	Bit	Symbol	Description
3E5 (cont.)	3 2	PTE23 PTE13	**Path Termination Mode Control for STS-3:STS-1 No. 3:** These two control bits determine the multiplexing (termination) of the path overhead bytes for the STS-3:STS-1 No. 3 transmit (receive) paths, according to the following table, assuming normal operation (DATACOM pin is low). See also Figures 23 and 24. (Note: These bits should be set to 0 when the SOT-3 device is configured for STS-3c mode.) They also control the transmission of VTAIS3, as shown in Figure 18. PTE23 PTE13 Action 0 0 The nine overhead bytes are transmitted intact from the terminal interface without processing. The ability to insert path FEBE and RDI, and have the SOT-3 function in the ring mode, is disabled. Receive side not terminated. 0 1 J1 message transmitted from RAM. B3 BIP-8 value calculated internally. C2 byte transmitted from RAM. G1 FEBE value from received BIP-8 and RDI controlled by local alarms when RING control bit is 0. When RING or PCROS3 is 1, FEBE and RDI are controlled by mate SOT-3 using the Alarm Indication Port (see Figure 23). Bits 2, 1 and 0 of byte are from RAM. F2, Z3, Z4 and Z5 bytes taken from terminal side. H4 byte from the terminal interface when H4INS bit is 0 or from multiframe generator when H4INS is 1. H4 multiframe generator locked to terminal side V1 pulse when H4INS is 1. Receive side path termination enabled. 1 0 J1 message transmitted from RAM. B3 BIP-8 value calculated internally. C2 byte transmitted from RAM. G1 FEBE value from received BIP-8 and RDI controlled by local alarms when RING control bit is 0. When RING or PCROS3 is 1, FEBE and RDI controlled by mate SOT-3 using the Alarm Indication Port (see Figure 23). Bits 2, 1 and 0 are from RAM. F2, Z3, Z4 and Z5 bytes transmitted from RAM. H4 RAM value transmitted. Receive side path termination enabled. 1 1 J1 message transmitted from RAM. B3 BIP-8 value calculated internally. C2 byte transmitted from RAM. G1 byte transmitted from RAM. RING and PCROS3 control bits disabled. F2, Z3, Z4 and Z5 bytes transmitted from RAM. H4 byte from terminal interface when H4INS bit is 0 or multiframe generator when H4INS is 1. H4 multiframe generator locked to terminal side V1 pulse when H4INS is 1. Receive side path termination enabled.

Address	Bit	Symbol	Description
3E5 (cont.)	1 0	PTE22 PTE12	**Path Termination Mode Control for STS-3:STS-1 No. 2:** These two control bits determine the multiplexing (termination) of the path overhead bytes for the STS-3:STS-1 No. 2 transmit (receive) paths, according to the following table, assuming normal operation (DATACOM pin is low). See also Figure 23 and 24. (Note: These bits should be set to 0 when the SOT-3 device is configured for STS-3c mode.) They also control the transmission of VTAIS2, as shown in Figure 18. PTE22 PTE12 Action 0 0 The nine overhead bytes are transmitted intact from the terminal interface without processing. The ability to insert path FEBE and RDI, and have the SOT-3 function in the ring mode, is disabled. Receive side not terminated. 0 1 J1 message transmitted from RAM. B3 BIP-8 value calculated internally. C2 byte transmitted from RAM. G1 FEBE value from received BIP-8 and RDI controlled by local alarms when RING control bit is 0. When RING or PCROS2 is 1, FEBE and RDI are controlled by mate SOT-3 using the Alarm Indication Port (see Figure 23). Bits 2, 1 and 0 of byte are from RAM. F2, Z3, Z4 and Z5 bytes taken from terminal side. H4 byte from the terminal interface when H4INS bit is 0 or from multiframe generator when H4INS is 1. H4 multiframe generator locked to terminal side V1 pulse when H4INS is 1. Receive side path termination enabled. 1 0 J1 message transmitted from RAM. B3 BIP-8 value calculated internally. C2 byte transmitted from RAM. G1 FEBE value from received BIP-8 and RDI controlled by local alarms when RING control bit is 0. When RING or PCROS2 is 1, FEBE and RDI controlled by mate SOT-3 using the Alarm Indication Port (see Figure 23). Bits 2, 1 and 0 are from RAM. F2, Z3, Z4 and Z5 bytes transmitted from RAM. H4 RAM value transmitted. Receive side path termination enabled. 1 1 J1 message transmitted from RAM. B3 BIP-8 value calculated internally. C2 byte transmitted from RAM. G1 byte transmitted from RAM. RING and PCROS2 control bits disabled. F2, Z3, Z4 and Z5 bytes transmitted from RAM. H4 byte from terminal interface when H4INS bit is 0 or multiframe generator when H4INS is 1. H4 multiframe generator locked to terminal side V1 pulse when H4INS is 1. Receive side path termination enabled.

Control Register 6

Address	Bit	Symbol	Description
3E6	7	TPRDI3	**Transmit Path RDI Enable for STS-3:STS-1 No. 3:** A 1 enables Path RDI (Bit 5 in G1 byte is 1) to be generated for the STS-3:STS-1 No. 3 signal for any of the following conditions (see Figure 23): When RING and PCROS3 are 0 and control bits PTE23, PTE13 are 01, 10 or 11 with: - Loss Of Signal (RLOS) when bit RAISE is 1 - Loss Of Frame (RLOF) when bit RAISE is 1 - Loss Of Clock (RLOC) when bit RAISE is 1 - Loss Of Pointer(RLOP3) when bit RAISE is 1 - Line AIS (RLAIS) (generated for the three STS-1 signals) when bit RAISE is 1 - Low on AIS pin ($\overline{\text{FAIS3}}$) when bit RAISE is 1 - C2 Mismatch (C2MM3) when bit RAISE is 1 - Unequipped Status (UNEQ3) when bit RAISE is 1 - Loss of Multiframe (RLOM3) when LM2AIS and RAISE are 1 - Path AIS (RPAIS3) when RAISE is 1 - Control bit SRAIS3 is 1, when RAISE is 1 - Bit 5 in G13 RAM location (1BAH) is a 1 When RING or PCROS3 is 1 and control bits PTE23, PTE13 are 01, 10 or 11 with: - Alarm Indication Port (bit 7) RDI from mate SOT-3 Control bit TPRDI3 is disabled when PTE23, PTE13 are 00, and RDI is controlled via the G1 byte from the transmit terminal interface. (Note: This bit should be set to 0 when the SOT-3 device is configured for STS-3c mode.)
	6	TPRDI2	**Transmit Path RDI Enable for STS-3:STS-1 No. 2:** A 1 enables Path RDI (Bit 5 in G1 byte is 1) to be generated for the STS-3:STS-1 No. 2 signal for any of the following conditions (see Figure 23): When RING and PCROS2 are 0 and control bits PTE22, PTE12 are 01, 10 or 11 with: - Loss Of Signal (RLOS) when bit RAISE is 1 - Loss Of Frame (RLOF) when bit RAISE is 1 - Loss Of Clock (RLOC) when bit RAISE is 1 - Loss Of Pointer(RLOP2) when bit RAISE is 1 - Line AIS (RLAIS) (generated for the three STS-1 signals) when bit RAISE is 1 - Low on AIS pin ($\overline{\text{FAIS2}}$) when bit RAISE is 1 - C2 Mismatch (C2MM2) when bit RAISE is 1 - Unequipped Status (UNEQ2) when bit RAISE is 1 - Loss of Multiframe (RLOM2) when LM2AIS and RAISE are 1 - Path AIS (RPAIS2) when RAISE is 1 - Control bit SRAIS2 is 1, when RAISE is 1 - Bit 5 in G12 RAM location (1B2H) is a 1 When RING or PCROS2 is 1 and control bits PTE22, PTE12 are 01, 10 or 11 with: - Alarm Indication Port (bit 15) RDI from mate SOT-3 Control bit TPRDI2 is disabled when PTE22, PTE12 are 00, and RDI is controlled via the G1 byte from the transmit terminal interface. (Note: This bit should be set to 0 when the SOT-3 device is configured for STS-3c mode.)

Address	Bit	Symbol	Description
3E6 (cont.)	5	UNEQ3	**Force payload for AU-3/STS-1 No. 3 to Zeros:** This bit works in conjunction with the UQPOH3 control bit according to the table shown below: UNEQ3 UQPOH3 Action 0 X Normal operation 1 0 Transmit line output payload bytes forced to zero for AU-3/STS-1 No. 3. POH bytes inserted as required. See Figure 24. 1 1 Transmit line output payload and POH bytes all forced to zero for AU-3/STS-1 No. 3. (Note: This bit should be set to 0 when the SOT-3 device is configured for STS-3c mode.)
	4	UQPOH3	**Force POH bytes for AU-3/STS-1 No. 3 to Zeros:** This bit works in conjunction with the UNEQ3 control bit as indicated in the table for UNEQ3. (Note: This bit should be set to 0 when the SOT-3 device is configured for STS-3c mode.)
	3	UNEQ2	**Force payload for AU-3/STS-1 No. 2 to Zeros:** This bit works in conjunction with the UQPOH2 control bit according to the table shown below: UNEQ2 UQPOH2 Action 0 X Normal operation 1 0 Transmit line output payload bytes forced to zero for AU-3/STS-1 No. 2. POH bytes inserted as required. See Figure 24. 1 1 Transmit line output payload and POH bytes all forced to zero for AU-3/STS-1 No. 2 (Note: This bit should be set to 0 when the SOT-3 device is configured for STS-3c mode.)
	2	UQPOH2	**Force POH bytes for AU-3/STS-1 No. 2 to Zeros:** This bit works in conjunction with the UNEQ2 control bit as indicated in the table for UNEQ2. (Note: This bit should be set to 0 when the SOT-3 device is configured for STS-3c mode.)
	1	UNEQ1	**Force payload for AU-4/STS-3c or AU-3/STS-1 No. 1 to Zeros:** This bit works in conjunction with the UQPOH1 control bit according to the table shown below: UNEQ1 UQPOH1 Action 0 X Normal operation 1 0 Transmit line output payload bytes forced to zero for AU-4/STS-3c or AU-3/STS-1 No. 1. POH bytes inserted as required. See Figure 24. 1 1 Transmit line output payload and POH bytes all forced to zero for AU-4/STS-3c or AU-3/STS-1 No. 1
	0	UQPOH1	**Force POH bytes for AU-4/STS-3c or AU-3/STS-1 No. 1 to Zeros:** This bit works in conjunction with the UNEQ1 control bit as indicated in the table for UNEQ1.

Control Register 7

Address	Bit	Symbol	Description
3E7	7	STIME	**Source Timing Mode:** This bit works in conjunction with the DATACOM and MODE0 pins according to the following table (where X is "don't care"): STIME / MODE0 / DATACOM / Action X / X / Low / Transmit terminal TSPE and TC1J1 signals are inputs. X / High / High / Data communication operation for the AU-4/STS-3c format only. RSPE and TSPE output signals are high for 260 time slots and low for 10 time slots. In addition, a TPOH indicator (TPOH), clock (TTCI), and C1J1 (TC1J1) signals are provided as output signals at the transmit terminal interface. 0 / Low / High / Data communication operation for the AU-4/STS-3c format only. RSPE and TSPE outputs signals are high for 258 time slots and low for 12 time slots. In addition, a TPOH indicator (TPOH), clock (TTCI), and C1J1 (TC1J1) signals are provided as output signals at the transmit terminal interface 1 / Low / High / Source timing mode. TSPE, TPOH, TTCI and TC1J1 are output signals. Valid for AU-4/STS-3c and AU-3/STS-3 operation. The TSPE and RSPE signals are high for 261 time slots (POH plus payload). The SOT-3 can also generate the H4 bytes and one or more V1 pulses for the TC1J1 signal for AU-4/STS-3c and AU-3/STS-3 operation. Note: In data communication and source timing modes, the Transmit Terminal (TSPE, TTCI and TC1J1) signals lead the input data by one byte time because they are timing control signals.
	6	TAIS3	**Transmit AIS for STS-3:STS-1 No. 3:** A 1 written into this bit position generates a transmit path AIS for STS-3:STS-1 No. 3 when it is enabled by control bit TRPAISE (at 3E2H bit 2, see description). Line AIS overrides the generation of path AIS. A 0 disables the microprocessor from generating path AIS. (Note: This bit should be set to 0 when the SOT-3 device is configured for STS-3c mode.) The following table describes the states associated with this control bit: TAIS3 / TRPAISE / Action X / 0 / The generation of transmit path AIS is disabled for STS-3:STS-1 No. 3. 0 / 1 / The generation of transmit path AIS is enabled for STS-3:STS-1 No. 3. Path AIS is generated when a transmit alarm occurs. 1 / 1 / Transmit path AIS is generated for STS-3:STS-1 No. 3.

Address	Bit	Symbol	Description
3E7 (cont.)	5	TAIS2	**Transmit AIS for STS-3:STS-1 No. 2:** A 1 written into this bit position generates a transmit path AIS for STS-3:STS-1 No. 2 when it is enabled by control bit TRPAISE (at 3E2H bit 2, see description). Line AIS overrides the generation of path AIS. A 0 disables the microprocessor from generating path AIS. (Note: This bit should be set to 0 when the SOT-3 device is configured for STS-3c mode.) The following table describes the states associated with this control bit: TAIS2 / TRPAISE / Action X / 0 / The generation of transmit path AIS is disabled for STS-3:STS-1 No. 2. 0 / 1 / The generation of transmit path AIS is enabled for STS-3:STS-1 No. 2. Path AIS is generated when a transmit alarm occurs. 1 / 1 / Transmit path AIS is generated for STS-3:STS-1 No. 2.
	4	SRAIS3	**Send Receive Internal VTAIS or Path AIS for STS-3:STS-1 No. 3:** A 1 causes VTAIS or path AIS (and path RDI) to be generated for STS-3:STS-1 No. 3 when control bit RAISE is 1. A 0 disables the microprocessor from generating VTAIS or path AIS (and path RDI). Setting this bit can cause Pointer Movements at the receive terminal interface. (Note: This bit should be set to 0 when the SOT-3 device is configured for STS-3c mode.)
	3	SRAIS2	**Send Receive Internal VTAIS or Path AIS for STS-3:STS-1 No. 2:** A 1 causes VTAIS or path AIS (and path RDI) to be generated for STS-3:STS-1 No. 2 when control bit RAISE is 1. A 0 disables the microprocessor from generating VTAIS or path AIS (and path RDI). Setting this bit can cause pointer movements at the receive terminal interface. (Note: This bit should be set to 0 when the SOT-3 device is configured for STS-3c mode.)
	2	ELOM3	**Enable Loss Of Multiframe for AU-3/STS-1 No. 3:** A 1 enables the loss of multiframe alarm detection for the received H4 byte of the AU-3/STS-1 No. 3. If the PTE23, PTE13 bits are not equal to 00, the H4 byte provided at the terminal interface is from the multiframe generator (pattern = 111111xx, where xx= 00,01,10,11,00...). In non-PTE mode, only the two LSB's are inserted, with the upper 6-bits passed through. A 0 disables the H4 multiframe alarm status. The H4 byte provided at the terminal interface is the received H4 byte. (Note: This bit should be set to 0 when the SOT-3 device is configured for STS-3c mode.)
	1	ELOM2	**Enable Loss Of Multiframe for AU-3/STS-1 No. 2:** A 1 enables the loss of multiframe alarm detection for the received H4 byte of the AU-3/STS-1 No. 2. If the PTE22, PTE12 bits are not equal to 00, the H4 byte provided at the terminal interface is from the multiframe generator (pattern = 111111xx, where xx= 00,01,10,11,00...). In non-PTE mode, only the two LSB's are inserted, with the upper 6-bits passed through. A 0 disables the H4 multiframe alarm status. The H4 byte provided at the terminal interface is the received H4 byte. (Note: This bit should be set to 0 when the SOT-3 device is configured for STS-3c mode.)
	0	ELOM1	**Enable Loss Of Multiframe for STM-1 AU-4/STS-3c or AU-3/STS-1 No. 1:** A 1 enables the loss of multiframe alarm detection for the received H4 byte of the STM-1 AU-4/STS-3c or the AU-3/STS-1 No. 1. If the PTE21, PTE11 bits are not equal to 00, the H4 byte provided at the terminal interface is from the multiframe generator (pattern = 111111xx, where xx= 00,01,10,11,00...). In non-PTE mode, only the two LSB's are inserted, with the upper 6-bits passed through. A 0 disables the H4 multiframe alarm status. The H4 byte provided at the terminal interface is the received H4 byte.

Control Registers 8 through D (Hex)

Address	Bit	Symbol	Description
3E8	7-0	C2R1	**C2 Mismatch Comparison Value for STM-1 AU-4/STS-3c or STS-3: STS-1 No. 1:** This byte location is used for comparison with the received STM-1 AU-4/STS-3c C2 byte or the STS-3:STS-1 No. 1 C2 byte.
3E9	7-0	C2R2	**C2 Mismatch Comparison Value for STS-3:STS-1 No. 2:** This byte location is used for comparison with the received STS-3:STS-1 No. 2 C2 byte. (Note: This byte should be set to 00H when the SOT-3 device is configured for STS-3c mode.)
3EA	7-0	C2R3	**C2 Mismatch Comparison Value for STS-3:STS-1 No. 3:** This byte location is used for comparison with the received STS-3:STS-1 No. 3 C2 byte. (Note: This byte should be set to 00H when the SOT-3 device is configured for STS-3c mode.)
3EB	7-0	RTA1	**Receive Terminal A1 Byte Value:** The value written into this byte location is sent at the receive terminal interface for the three A1 bytes when control bit RTA1A2E is 1. When control bit RTA1A2E is 0, the three A1 bytes are sent with content F6H.
3EC	7-0	RTA2	**Receive Terminal A2 Byte Value:** The value written into this byte location is sent at the receive terminal interface for the three A2 bytes when control bit RTA1A2E is 1. When control bit RTA1A2E is 0, the three A2 bytes are sent with content 28H.
3ED	7-5	Reserved	These bits must be set to 0.
	4	INVCI	**Invert Transmit Terminal Clock in:** When this control bit is 1, Transmit Terminal Data In (TTDI) data signals are clocked in on the rising edge of the Transmit Terminal Clock In (TTCI) clock signal. When this control bit is 0, Transmit Terminal Data In (TTDI) data signals are clocked in on the falling edge of the Transmit Terminal Clock In (TTCI) clock signal. This bit is for use only in data communication or source timing modes. In normal mode, all transmit terminal interface inputs are clocked in on the rising edge of TTCI.
	3	RDPAR	**Receive Data Parity Mode Selector:** This bit works in conjunction with the TPLEV control bit for calculating the parity of the Receive Terminal Data signals. The following states are possible: RDPAR / TPLEV / Action 0 / 1 / Even parity generated over the terminal side byte data (RTDO(7-0)), the C1J1 indication (RC1J1), and SPE indication (RSPE). 0 / 0 / Odd parity generated over the terminal side byte data (RTDO(7-0)), the C1J1 indication (RC1J1), and SPE indication (RSPE). 1 / 1 / Even parity generated over the terminal side byte data (RTDO(7-0)) only. 1 / 0 / Odd parity generated over the terminal side byte data (RTDO(7-0)) only.
	2-0	Reserved	These bits must be set to 0.

STATUS REGISTER DESCRIPTIONS

Address	Bit	Symbol	Description
3D0	7	RLOC	**Receive Loss Of Clock:** A receive loss of clock alarm occurs when no transitions are detected in the RLCI clock for 1000 ± 500 ns. Recovery occurs on the first clock transition.
	6	RLOS	**Receive Loss Of Signal:** A receive loss of signal alarm occurs when either a high is detected on the RXLOS pin or no data transitions are detected in the byte-parallel RLDI data signal for 125 microseconds. Recovery then occurs when a low is detected on the RXLOS pin or a data transition is detected in the RLDI data, respectively.
	5	ROOF	**Receive Out Of Frame:** A receive out of frame alarm occurs when a high is detected on the RXOOF pin, and no RLOC or RLOS alarm is declared.
	4	RLOF	**Receive Loss Of Frame:** A receive loss of frame alarm occurs when a high is detected on the RXLOF pin, and no RLOC or RLOS alarm is declared.
	3	RLAIS	**Receive Line AIS:** A receive line AIS occurs when the 111 bit pattern is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames. Recovery occurs when bits 6, 7, and 8 are not equal to 111 for five consecutive frames. RLAIS will not be declared when a RLOC, RLOS, ROOF or RLOF alarm is active.
	2	RPAIS3	**Receive Path AIS for STS-3:STS-1 No. 3:** A receive path AIS alarm occurs when the H1/H2 pointer bytes are equal to all ones for three consecutive frames. Recovery occurs on a NDF transition, or when a new/consistent pointer is received for three consecutive frames. This alarm is disabled when the STM-1 AU4/STS-3c format is selected.
	1	RPAIS2	**Receive Path AIS for STS-3:STS-1 No. 2:** A receive path AIS alarm occurs when the H1/H2 pointer bytes are equal to all ones for three consecutive frames. Recovery occurs on a NDF transition, or when a new/consistent pointer is received for three consecutive frames. This alarm is disabled when the STM-1 AU4/STS-3c format is selected.
	0	RPAIS1	**Receive Path AIS for STM-1 AU-4/STS-3c or STS-3:STS-1 No. 1:** A receive path AIS alarm occurs when the H1/H2 pointer bytes are equal to all ones for three consecutive frames. Recovery occurs on a NDF transition, or when a new/consistent pointer is received for three consecutive frames.
3D1	7-0		The bits in this register are the same as those in the corresponding bit positions of the preceding register (3D0H), except that these bits latch on the positive level of an alarm. A latched bit position then remains set until it is cleared by a microprocessor read cycle of the register, but if the alarm for the bit is active at the time of the read cycle the latched bit will immediately relatch.

Address	Bit	Symbol	Description
3D2	7	RAPS	**Receive APS Byte Failure:** A receive APS alarm occurs when no three consecutive K1 bytes in any 12 consecutive frames are identical. Recovery occurs when three consecutive identical K1 bytes are received. There is no requirement placed on the K2 byte for this alarm.
	6	RLOP3	**Receive Loss Of Pointer for STS-3:STS-1 No. 3:** A receive loss of pointer alarm occurs when either an NDF, or an invalid pointer, is detected in the H13/H23 bytes for eight consecutive frames. (Note: In combination with INC/DEC/NDF or other conditions, a LOP may be declared in as few as six frames.) Recovery occurs when a consistent, valid pointer is received for three consecutive frames. This alarm is disabled when the STM-1 AU4/STS-3c format is selected.
	5	RLOP2	**Receive Loss Of Pointer for STS-3:STS-1 No. 2:** A receive loss of pointer alarm occurs when either an NDF, or an invalid pointer, is detected in the H12/H22 bytes for eight consecutive frames. (Note: In combination with INC/DEC/NDF or other conditions, a LOP may be declared in as few as six frames.) Recovery occurs when a consistent, valid pointer is received for three consecutive frames. This alarm is disabled when the STM-1 AU4/STS-3c format is selected.
	4	RLOP1	**Receive Loss Of Pointer for STM-1 AU4/STS-3c or STS-3:STS-1 No. 1:** A receive loss of pointer alarm occurs when either an NDF, or an invalid pointer, is detected in the H11/H21 bytes for eight consecutive frames. (Note: In combination with INC/DEC/NDF or other conditions, a LOP may be declared in as few as six frames.) Recovery occurs when a consistent, valid pointer is received for three consecutive frames.
	3	RLRDI	**Receive Line RDI:** A receive line RDI alarm occurs when five consecutive 110 bit patterns are detected in bits 6, 7 and 8 of the K2 byte. Recovery occurs when bits 6, 7 and 8 are not equal to 110 for five consecutive frames. RLRDI will not be declared when a RLOC, RLOS, ROOF, RLOF or RLAIS alarm is active.
	2	RLOM3	**Receive Loss Of Multiframe for STS-3:STS-1 No. 3:** When enabled by writing a 1 to control bit ELOM3 and when the MODE0 pin is low, a loss of multiframe alarm occurs if two or more consecutive H43 bytes are mismatched for two consecutive multiframes. RLOM3 can be declared within 6 frames. When the alarm occurs, the internal H4 multiframe detector will start a search for a multiframe pattern immediately. During the search, the multiframe generator will continue to generate the H4 byte. Recovery occurs when four consecutive sequential H4 byte values are detected. When the MODE0 pin is high, this alarm is active for the conditions above, but no further action takes place. This alarm is disabled when the STM-1 AU4/STS-3c format is selected.
	1	RLOM2	**Receive Loss Of Multiframe for STS-3:STS-1 No. 2:** When enabled by writing a 1 to control bit ELOM2 and when the MODE0 pin is low, a loss of multiframe alarm occurs if two or more consecutive H42 bytes are mismatched for two consecutive multiframes. RLOM2 can be declared within 6 frames. When the alarm occurs, the internal H4 multiframe detector will start a search for a multiframe pattern immediately. During the search, the multiframe generator will continue to generate the H4 byte. Recovery occurs when four consecutive sequential H4 byte values are detected. When the MODE0 pin is high, this alarm is active for the conditions above, but no further action takes place This alarm is disabled when the STM-1 AU4/STS-3c format is selected.

Address	Bit	Symbol	Description
3D2 (cont.)	0	RLOM1	**Receive Loss Of Multiframe for STM-1 AU-4/STS-3c or STS-3:STS-1 No. 1:** When enabled by writing a 1 to control bit ELOM1 and when the MODE0 pin is low, a loss of multiframe alarm occurs if two or more consecutive H41 bytes are mismatched for two consecutive multiframes. RLOM1 can be declared within 6 frames. When the alarm occurs, the internal H4 multiframe detector will start a search for a multiframe pattern immediately. During the search, the multiframe generator will continue to generate the H4 byte. Recovery occurs when four consecutive sequential H4 byte values are detected. When the MODE0 pin is high, this alarm is active for the conditions above, but no further action takes place.
3D3	7-0		The bits in this register are the same as those in the corresponding bit positions of the preceding register (3D2H), except that these bits latch on the positive level of an alarm. A latched bit position then remains set until it is cleared by a microprocessor read cycle of the register, but if the alarm for the bit is active at the time of the read cycle the latched bit will immediately relatch.
3D4	7	RNAPS	**Receive New APS Bytes:** A Receive New APS byte alarm occurs when three consecutive new values are detected in the K1 byte and the first five bits of the K2 byte, from the previous stable value or following an APS byte failure. Recovery occurs at the B1 byte time of the next frame.
	6	RPRDI3	**Receive Path RDI for STS-3:STS-1 No. 3:** A receive path RDI alarm occurs if bit 5 in the G1 byte for the STS-3:STS-1 No. 3 is equal to 1 for ten consecutive frames when control bit CCITT is 0. Recovery occurs when bit 5 is 0 for ten consecutive frames. When control bit CCITT is 1, the alarm occurs when bit 5 is 1 for five consecutive frames. Recovery then occurs when bit 5 is 0 for five consecutive frames. In both cases the RPRDI3 detection circuit is inhibited when a receive side RLOC, RLOS, ROOF, RLOF, RLAIS, RPAIS3 or RLOP3 is active. This alarm is disabled when the STM-1 AU4/STS-3c format is selected.
	5	RPRDI2	**Receive Path RDI for STS-3:STS-1 No. 2:** A receive path RDI alarm occurs if bit 5 in the G1 byte for the STS-3:STS-1 No. 2 is equal to 1 for ten consecutive frames when control bit CCITT is 0. Recovery occurs when bit 5 is 0 for ten consecutive frames. When control bit CCITT is 1, the alarm occurs when bit 5 is 1 for five consecutive frames. Recovery then occurs when bit 5 is 0 for five consecutive frames. In both cases the RPRDI2 detection circuit is inhibited when a receive side RLOC, RLOS, ROOF, RLOF, RLAIS, RPAIS2 or RLOP2 is active. This alarm is disabled when the STM-1 AU4/STS-3c format is selected.
	4	RPRDI1	**Receive Path RDI for STM-1 AU-4/STS-3c or STS-3:STS-1 No. 1:** A receive path RDI alarm occurs if bit 5 in the G1 byte for the STM-1 AU-4/STS-3c or the STS-3:STS-1 No. 1 is equal to 1 for ten consecutive frames when control bit CCITT is 0. Recovery occurs when bit 5 is 0 for ten consecutive frames. When control bit CCITT is 1, the alarm occurs when bit 5 is 1 for five consecutive frames. Recovery then occurs when bit 5 is 0 for five consecutive frames. In both cases the RPRDI1 detection circuit is inhibited when a receive side RLOC, RLOS, ROOF, RLOF, RLAIS, RPAIS1 or RLOP1 is active.

Address	Bit	Symbol	Description
3D4 (cont.)	3	RFIFO	**Receive FIFO Error:** A receive FIFO alarm occurs when the receive FIFO overflows or underflows. The FIFO will be reset automatically if a 1 has been written to bit 4 (FRENB) in register 3E3H, or it may be reset by the microprocessor by writing a 1 to bit 1 (FIFORST) in register 3E3H. The receive FIFO error alarm is valid for either an STM-1 AU-4/STS-3c or an STS-3 format.
	2	TFIFO	**Transmit FIFO Error:** A transmit FIFO alarm occurs when the transmit FIFO overflows or underflows. The FIFO will be reset automatically if a 1 has been written to bit 4 (FRENB) in register 3E3H, or it may be reset by the microprocessor by writing a 1 to bit 1 (FIFORST) in register 3E3H. The transmit FIFO error alarm is valid for either an STM-1 AU-4/STS-3c or an STS-3 format.
	1	Reserved	When it is read, this bit will be found to contain a 0.
	0	APNAPS	**Alarm Indication Port New APS Byte:** An alarm occurs when bit 37 (RNAPS alarm) in the Alarm Indication Port 40-bit format transitions from a 0 to a 1. A 1 indicates that a New APS alarm has been detected in the mate SOT-3. The alarm condition is exited when bit 37 (RNAPS alarm) in the Alarm Indication Port 40-bit format transitions back to a 0. See Figure 25.
3D5	7-0		The bits in this register are the same as those in the corresponding bit positions of the preceding register (3D4H), except that these bits latch on the positive level of an alarm. A latched bit position then remains set until it is cleared by a microprocessor read cycle of the register, but if the alarm for the bit is active at the time of the read cycle the latched bit will immediately relatch.
3D6	7	SINT	**Software Interrupt:** A software interrupt indication (SINT is 1) occurs when one or more of the alarm mask bits in the interrupt mask locations is set to 1 and a corresponding latched alarm is set to 1. The interrupt indication state is exited when any remaining latched alarm causing the interrupt clears or its corresponding bit in the interrupt mask is cleared. If bit 7 in 3F3H (HINT) is set to 1 to enable the hardware interrupt, the occurrence of SINT will cause a hardware interrupt at the INT/$\overline{\text{IRQ}}$ pin.
	6	TLOC	**Transmit Loss Of Clock:** A transmit loss of clock alarm occurs when no transitions are detected on the TTCI pin for 1000 $\pm$ 500 ns. This alarm is disabled when the data communication or source timing mode is selected. Recovery occurs on the first transition.
	5	TLOS	**Transmit Loss Of Signal:** A transmit loss of signal alarm occurs when no data transitions are detected in the byte-parallel TTDI data signal for 125 microseconds. Recovery occurs when a data transition is detected in the TTDI data.
	4	BERR	**Bus Parity Error:** This bit indicates when a data error is detected in the transmit direction. Other than providing an alarm indication, no action is taken by the SOT-3.
	3	RAMLOC	**RAM Loss Of Clock:** A RAM loss of clock alarm occurs when no transitions are detected on the RAMCI pin for 1000 $\pm$ 500 ns. Recovery occurs on the first transition.

Address	Bit	Symbol	Description
3D6 (cont.)	2	SPRDI3	**Transmit Alarm Indication Port Send Path RDI for STS-3:STS-1 No. 3:** An alarm occurs when bit 7 (send Path RDI3 alarm) in the Alarm Indication Port data bit stream is 1. A 1 indicates that a Path RDI indication has been generated in the mate SOT-3. The alarm condition is exited when bit 7 in the Alarm Indication Port data bit stream is 0. See Figure 25.
	1	SPRDI2	**Transmit Alarm Indication Port Send Path RDI for STS-3:STS-1 No. 2:** An alarm occurs when bit 15 (send Path RDI2 alarm) in the Alarm Indication Port data bit stream is 1. A 1 indicates that a Path RDI indication has been generated in the mate SOT-3. The alarm condition is exited when bit 15 in the Alarm Indication Port data bit stream is 0. See Figure 25.
	0	SPRDI1	**Transmit Alarm Indication Port Send Path RDI for STM-1 AU-4/STS-3c or STS-3:STS-1 No. 1:** An alarm occurs when bit 39 (send Path RDI1 alarm) in the Alarm Indication Port data bit stream is 1. A 1 indicates that a Path RDI indication has been generated in the mate SOT-3. The alarm condition is exited when bit 39 in the Alarm Indication Port data bit stream is 0. See Figure 25.
3D7	7-0		The bits in this register are the same as those in the corresponding bit positions of the preceding register (3D6H), except that these bits latch on the positive level of an alarm. A latched bit position then remains set until it is cleared by a microprocessor read cycle of the register, but if the alarm for the bit is active at the time of the read cycle the latched bit will immediately relatch.
3D8	7	TAIPLOC	**Transmit Alarm Indication Port Loss Of Clock:** A Transmit AIP loss of clock alarm occurs when no transitions are detected on the TAICI pin for 1000 $\pm$ 500 ns. Recovery occurs on the first transition.
	6	Reserved	When it is read, this bit will be found to contain a 0.
	5	UALM3	**Receive Unequipped Status Alarm for AU-3/STS-1 No. 3:** A receive unequipped alarm occurs when the C2 byte for STS-3:STS-1 No. 3 is equal to 00H for five consecutive frames. Recovery occurs when the C2 byte is not equal to 00H for five consecutive frames. An unequipped alarm inhibits the corresponding C2 mismatch alarm. This alarm is disabled when the STM-1 AU4/STS-3c format is selected.
	4	UALM2	**Receive Unequipped Status Alarm for AU-3/STS-1 No. 2:** A receive unequipped alarm occurs when the C2 byte for STS-3:STS-1 No. 2 is equal to 00H for five consecutive frames. Recovery occurs when the C2 byte is not equal to 00H for five consecutive frames. An unequipped alarm inhibits the corresponding C2 mismatch alarm. This alarm is disabled when the STM-1 AU4/STS-3c format is selected.
	3	UALM1	**Receive Unequipped Status Alarm for STM-1 AU-4/STS-3c or AU-3/STS-1 No. 1:** A receive unequipped alarm occurs when the C2 byte for STM-1 AU-4/STS-3c or STS-3:STS-1 No. 1 is equal to 00H for five consecutive frames. Recovery occurs when the C2 byte is not equal to 00H for five consecutive frames. An unequipped alarm inhibits the corresponding C2 mismatch alarm.

Address	Bit	Symbol	Description
3D8 (cont.)	2	C2MM3	**C2 Mismatch Alarm for STS-3:STS-1 No. 3:** A C2 mismatch alarm for STS-3:STS-1 No. 3 occurs when the C2 byte does not match the microprocessor-written value (location 3EAH) for five consecutive frames or 01H for five consecutive frames. The 01H value represents an earlier code for acceptance. Recovery occurs when the C2 byte is equal to the microprocessor-written value for five consecutive frames or 01H for five consecutive frames. This alarm is disabled when the STM-1 AU4/STS-3c format is selected.
	1	C2MM2	**C2 Mismatch Alarm for STS-3:STS-1 No. 2:** A C2 mismatch alarm for STS-3:STS-1 No. 2 occurs when the C2 byte does not match the microprocessor-written value (location 3E9H) for five consecutive frames or 01H for five consecutive frames. The 01H value represents an earlier code for acceptance. Recovery occurs when the C2 byte is equal to the microprocessor-written value for five consecutive frames or 01H for five consecutive frames. This alarm is disabled when the STM-1 AU4/STS-3c format is selected.
	0	C2MM1	**C2 Mismatch Alarm for STM-1 AU-4/STS-3c or STS-3:STS-1 No. 1:** A C2 mismatch alarm for STM-1 AU-4/STS-3c or STS-3:STS-1 No. 1 occurs when the C2 byte does not match the microprocessor-written value (location 3E8H) for five consecutive frames or 01H for five consecutive frames. The 01H value represents an earlier code for acceptance. Recovery occurs when the C2 byte is equal to the microprocessor-written value for five consecutive frames or 01H for five consecutive frames.
3D9	7-0		The bits in this register are the same as those in the corresponding bit positions of the preceding register (3D8H), except that these bits latch on the positive level of an alarm. A latched bit position then remains set until it is cleared by a microprocessor read cycle of the register, but if the alarm for the bit is active at the time of the read cycle the latched bit will immediately relatch.
3DA	7-0	Reserved	When they are read, each of these bits will be found to contain a 0.
3DB	7-0	Reserved	The bits in this register are the same as those in the corresponding bit positions of the preceding register (3DAH), except that these bits latch on the positive level of an alarm. A latched bit position then remains set until it is cleared by a microprocessor read cycle of the register, but if the alarm for the bit is active at the time of the read cycle the latched bit will immediately relatch.
3DC	7-0	Reserved	When they are read, each of these bits will be found to contain a 0.
3DD	7-0	Reserved	The bits in this register are the same as those in the corresponding bit positions of the preceding register (3DCH), except that these bits latch on the positive level of an alarm. A latched bit position then remains set until it is cleared by a microprocessor read cycle of the register, but if the alarm for the bit is active at the time of the read cycle the latched bit will immediately relatch.

INTERRUPT MASK REGISTER DESCRIPTIONS

When set to 1, each interrupt mask bit in the five registers 3F0H through 3F4H enables the occurrence of a 1 value in the corresponding latched alarm bit with the same Symbol and bit position in the five registers 3D1H, 3D3H, 3D5H, 3D7H and 3D9H, respectively, to set the software interrupt status bit SINT to 1 (bit 7 in register 3D6H). If the mask bit HINT (bit 7 in register 3F3H) is 1, then the hardware interrupt output at pin 45 (INT/$\overline{IRQ}$) is enabled to indicate an interrupt request to the microprocessor while the latched value of SINT in bit 7 of register 3D7H is 1. Otherwise, the SINT bit is 0 and pin 45 indicates no interrupt request.

PERFORMANCE COUNTER AND K1-K2 BYTE REGISTER DESCRIPTIONS

8-Bit Pointer Justification and NDF Counter Descriptions

Address	Bit	Symbol	**Description** (Note 1)
051 054 057	7-0	INC Count n (n=1-3)	**Positive Justification (INC) Counters:** Each RAM location is an eight-bit counter which counts the number of positive (increment) pointer movements in the receive line input for the SPE based on the H1 and H2 pointer bytes. Location 051H counts increments in the STM-1/STS-3c or STS-3:STS-1 No. 1 signal. Location 054H counts increments in STS-1 No. 2, and 057H counts increments in STS-1 No. 3. See Note 1.
052 055 058	7-0	DEC Count n (n=1-3)	**Negative Justification (DEC) Counters:** Each RAM location is an eight-bit counter which counts the number of negative (decrement) pointer movements in the receive line input for the SPE based on the H1 and H2 pointer bytes. Location 052H counts decrements in the STM-1/STS-3c or STS-3:STS-1 No. 1 signal. Location 055H counts decrements in STS-1 No. 2, and 058H counts decrements in STS-1 No. 3. See Note 1.
053 056 059	7-0	NDF Count n (n=1-3)	**New Data Flag (NDF) Counters:** Each RAM location is an eight-bit counter which counts the number of NDFs received in bits 1 to 4 of the H1 pointer byte in the receive line input. Location 053H counts NDFs in the STM-1/STS-3c or STS-3:STS-1 No. 1 signal. Location 056H counts NDFs in STS-1 No. 2, and 059H counts NDFs in STS-1 No. 3. See Notes 1 and 2.

Notes 1: Bit 0 is the least significant bit of each counter. Each counter is non-saturating (i.e., it rolls over from all ones to all zeros). Each counter is frozen during the following associated alarm conditions: RLOC, RLOS, RLOF, RLAIS, RLOPn or RPAISn, where n=1-3. Each counter is set to FEH during SOT-3 reset (pin 142) and is not reset on read.

2: NDF is reported for the following values: 1001 (the specified value for a New Data Flag) and the following single bit error values: 1000, 0001, 1101, 1011. All other values are not NDFs and are processed as normal pointer values.

16-Bit B1, B2, B3 and FEBE Counter and K1-K2 Byte Register Descriptions

Address	Bit	Symbol	Description
192	7-0	B1 Counter	**B1 Error Counter Low Order Byte:** This 16-bit counter is updated from the error indications received in the B1 byte of the receive line signal from the SYN155 or other device. Errors are represented by a one in one or more of the eight columns of the byte, with up to eight error indications per frame. When the low order byte is read from 192H, the high order byte is copied into 3FFH for reading next. See Note 1.
194	7-0	B2 Counter	**B2 Error Counter Low Order Byte:** This 16-bit counter counts the number of BIP-24 error indications detected in the three B2 bytes in the receive line signal. When the low order byte is read from 194H, the high order byte is copied into 3FFH for reading next. See Note 1.
198 19A 19C	7-0	B3n Count (n=1-3)	**B3 Error Counters Low Order Byte:** These three 16-bit counters count the number of B31, B32 and B33 BIP-8 error indications detected in the incoming B3 bytes of the receive line signal. Location 198H counts B31 errors in the STM-1 VC-4/STS-3c or STS-3:STS-1 No. 1 SPE. Location 19AH counts B32 errors in the STS-1 No. 2 SPE, and location 19CH counts B33 errors in the STS-1 No. 3 SPE. When the low order byte is read from 198H, 19AH or 19CH, the high order byte is copied into 3FFH for reading next. See Note 1 (in addition, these three counters are all frozen during RLAIS and individually during the corresponding RLOPn or RPAISn).
19E 1A0 1A2	7-0	FEBEn Count (n=1-3)	**FEBE Counters Low Order Byte:** These three 16-bit counters count the number of G11, G12 and G13 FEBE indications detected in the incoming G1 byte (received bits 1-4) of the receive line input. Only values between 1 and 8 are accepted, with the values of 0 and 9-15 counted as zero. Location 19EH counts the FEBEs from the STM-1 VC-4/STS-3c or STS-3:STS-1 No. 1 G11 byte. Location 1A0H counts the FEBEs from the STS-1 No. 2 G12 byte, and location 1A2H counts the FEBEs for the STS-1 No. 3 G13 byte. When the low order byte is read from 19EH, 1A0H or 1A2H, the high order byte is copied into 3FFH for reading next. See Note 1 (in addition, these three counters are all frozen during RLAIS and individually during the corresponding RLOPn or RPAISn)
196-197	7-0	dbK1K2	**Received Debounced K1-K2 Bytes:** After the same new K1-K2 value is received at the receive line input for three consecutive frames, a debounce indication occurs (RNAPS) and the new persistent K1 and K2 bytes are stored. The value is determined only by the K1 and 5 MSB's of the K2, which are the APS bits. Changes in the three LSB's of K2 are not used to determine APS debouncing. When the debounced K1 value is read from 196H, the debounced K2 value is copied into location 3FFH for reading next.

Note 1: Bit 0 of this low order byte is the least significant bit of each counter. Each 16-bit counter is non-saturating (i.e., it rolls over from all ones to all zeros). Each counter is frozen during the following associated alarm conditions: RLOC, RLOS, RLOF, or ROOF. Each counter is set to FFE0H during SOT-3 reset (pin 142) and is not reset on read. Each counter may be set to count block errors or individual bit errors by means of the control bit BLOCK, unless otherwise indicated.

Address	Bit	Symbol	Description
1A4-1A5	7-0	dbK1K2AP	**Debounced K1-K2 Bytes From Alarm Indication Port:** After the same new K1-K2 value is received at the mate SOT-3 for three consecutive frames, a debounce indication is sent over the Alarm Indication Port (APNAPS), together with the new K1-K2 bytes. The debounced K1-K2 continues to be sent until a new persistent value is detected. When the debounced K1 value is read from 1A4H, the debounced K2 value is copied into location 3FFH for reading next. The change in value is determined only by the APS bits: K1 and the 5 MSB's of K2.
1A6	7-0	Line FEBE Count	**Line FEBE Counter Low Order Byte:** This 16-bit counter is incremented with the number of line FEBE errors detected in the Z23 byte when control bit Z2FEBE is 1. Only a count between 1 and 24 is valid. Other counts are counted as zero errors. When the low order byte is read from 1A6H, the high order byte is copied into 3FFH for reading next. See Note 1 (block error counting is not available). In addition to the alarms listed in Note 1, this counter is frozen during RLAIS.
3FF	7-0	Shared High Byte	**Shared High Order Byte for 16-Bit Counters and Debounced K1-K2:** This RAM location is used on a shared basis for the high order byte in a 16-bit read operation. The B1, B2, B3 and FEBE counters, and the debounced K1-K2 values from both the receive side and the Alarm Indication Port, are accessed with 16-bit reads using this location for access to the high order byte value prevailing at the time of reading the low order byte. The high order byte must be read from this location before the next 16-bit read is initiated.

Note 1: Bit 0 of this low order byte is the least significant bit of each counter. Each 16-bit counter is non-saturating (i.e., it rolls over from all ones to all zeros). Each counter is frozen during the following associated alarm conditions: RLOC, RLOS, RLOF, or ROOF. Each counter is set to FFE0H during SOT-3 reset (pin 142) and is not reset on read. Each counter may be set to count block errors or individual bit errors by means of the control bit BLOCK, unless otherwise indicated.

PACKAGE INFORMATION

The SOT-3 device is packaged in a 160-pin plastic quad flat package (PQFP) suitable for surface mounting, as illustrated in Figure 26.

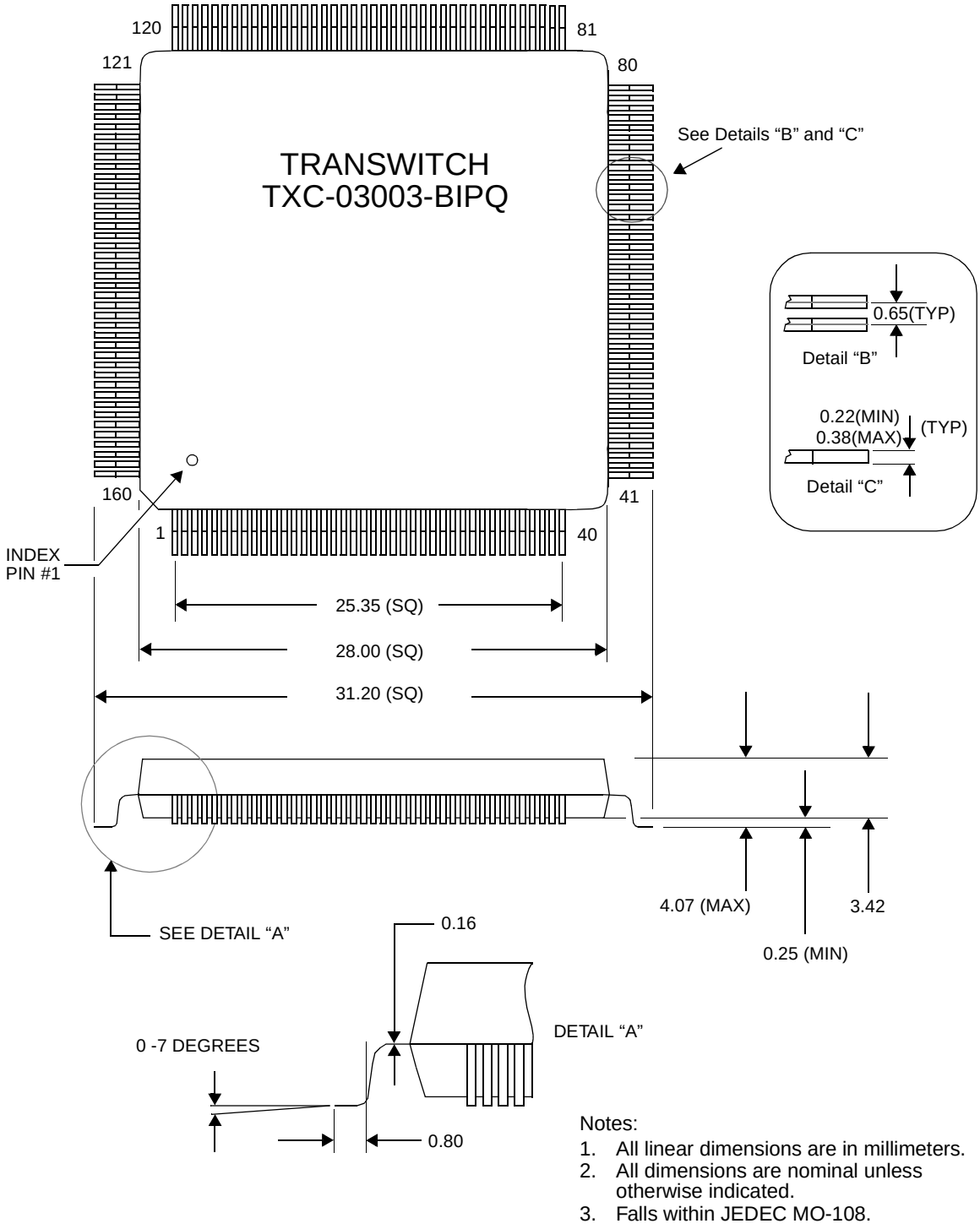


Figure 26. SOT-3 TXC-03003B 160-Pin Plastic Quad Flat Package

ORDERING INFORMATION

Part Number: TXC-03003-BIPQ	160-Pin Plastic Quad Flat Package

RELATED PRODUCTS

TXC-02301B, SYN155 VLSI Device (155-Mbit/s Synchronizer, Data Output). Provides complete STS-3/STM-1 frame synchronization on incoming 155 Mbit/s signals in a single low power CMOS unit.

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). This device is similar to the SYN155. It has both clock and data outputs on the line side.

TXC-03003, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This device performs section, line, and path overhead processing for a STS-3/STS-3c/STM-1 signal. Compliant with ANSI and ITU-T standards.

TXC-03452B, L3M VLSI Device (Level 3 Mapper). Maps a DS3 or E3 line signal into an SDH/SONET signal formatted for STM-1 (TUG-3) or STS-3/STS-1 (STS SPE).

TXC-04001B, ADMA-T1 VLSI Device (Dual DS1 to VT1.5 or TU-11 Async Mapper-Desync). Interconnects two DS1 signals with any two asynchronous mode VT1.5 or TU-11 tributaries carried in SONET STS-1 or SDH AU-3 rate payload interface.

TXC-04002, ADMA-E1 VLSI Device (2 Mbit/s to TU-12 Async Mapper-Desync). Designed for add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Connects with the SOT-3 to form an STM-1 add/drop or terminal system.

TXC-04011, ADMA-T1P VLSI Device (Dual T1 1.544 Mbit/s to VT1.5 or TU-11 Async Mapper-Desync). Interconnects two T1 signals with any two asynchronous mode VT1.5 or TU-11 tributaries carried in SONET STS-1 or SDH AU-3 rate payload interface. This is a ‘Plus’ version of the ADMA-T1 device that supports the add bus timing mode in addition to the drop bus timing mode and is packaged in a 120-pin PQFP.

TXC-05150, CDB VLSI Device (Cell Delineation Block). Provides cell delineation for ATM cells carried in a physical line at rates of 1.544 to 155 Mbit/s.

TXC-05501, SARA-S VLSI Device (ATM/SMDS Segmentation Controller). Simultaneously segments up to 8000 packets into ATM/SMDS cells.

TXC-05601, SARA-R VLSI Device (ATM/SMDS Reassembly Controller). Simultaneously reassembles ATM/SMDS cells back into up to 8000 packets.

TXC-21061, SOT-3/SYN155/ADMA-E1 Evaluation Board. A complete, ready-to-use single board test system that demonstrates the functions and features of the ADMA-E1, SOT-3, and SYN155 VLSI devices. Includes on-board microprocessor, RS-232 interface, and MS-DOS compatible PC software. The PC software provides full access to the ADMA-E1 and SOT-3 devices for control and monitoring.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

The ATM Forum (U.S.A.):

ATM Forum World Headquarters
303 Vintage Park Drive
Foster City, CA 94404-1138

Tel: 415-578-6860
Fax: 415-525-0182

ATM Forum European Office
14 Place Marie - Jeanne Bassot
Levallois Perret Cedex
92593 Paris France

Tel: 33 1 46 39 56 26
Fax: 33 1 46 39 56 99

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

EIA - Electronic Industries Association (U.S.A.):

Global Engineering Documents
Suite 407
7730 Carondelet Avenue
Clayton, MO 63105

Tel: 800-854-7179 (In U.S.A.)
Fax: 314-726-6418

ETSI (Europe):

European Telecommunications Standards Institute
ETSI, 06921 Sophia - Antipolis
Cedex France

Tel: 33 92 94 42 00
Fax: 33 93 65 47 16

ITU-T (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (T)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

MIL-STD Military Standard (U.S.A.):

Standardization Documents Order Desk
700 Robbins Avenue
Building 4D
Philadelphia, PA 19111-5094

Tel: 212-697-1187
Fax: 215-697-2978

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated SOT-3 Data Sheet that have significant differences relative to the previous and now superseded SOT-3 Data Sheet.

Updated SOT-3 Data Sheet: Edition 2, November 1998

Previous SOT-3 Data Sheet: *PRODUCT PREVIEW* Edition 1, September 1995

The page numbers indicated below of this updated Data Sheet include significant changes relative to the previous Data Sheet (consequent changes in pagination and figure numbers are not described in this list of changes).

Page Number of Updated Data Sheet	Summary of the Change
All	Changed the edition number from 1 to 2 and the date from September 1995 to November 1998.
All	Deleted markings and explanations of Product Preview document status.
1	Added item 15 to the Features list (power supply). Clarified item 16 (package). Updated patent and copyright information.
2-4	Updated Table of Contents and List of Figures, inserted blank page.
7	In second paragraph of Transmit Terminal Input Block subsection, added text related to the effect of the MODE0 pin.
13	Added text to second paragraph of Name/Function column for Symbol TSPE.
18, 19	Added the last sentence to Name/Function column for Symbols $\overline{\text{FAIS1}}$ (pin 130), $\overline{\text{FAIS2}}$ (pin 129) and $\overline{\text{FAIS3}}$ (pin 128). Clarified the last sentence of Name/Function column for Symbol RESET.
20	Added reference to receive VT AIS to Name/Function column for Symbols RXAIS1 (pin 76), RXAIS2 (pin 77), RXAIS3 (pin 78) and Note 1.
21	Changed title of first table to include environmental limitations and added last five rows of related information. Deleted rows for continuous power dissipation and operating junction temperature. Added Conditions column and expanded notes. Added Note 1 to last table and changed values in table rows for I_{DD} and P_{DD}.
22	In the Input Parameters for CMOS table, changed V_{IH} Min value and V_{IL} Max value. In the Input/Output Parameters for CMOS2mA table, changed V_{IH} Min value, V_{IL} Max value, V_{OH} Min value and V_{OL} Max value.
23-24	In the Input/Output Parameters for TTL2mA and TTL8mA tables and the Output Parameters for CMOS2mA and TTL4mA tables, changed V_{OH} Min value and V_{OL} Max value.
25	Added second paragraph.
26	Changed Min column for Symbol $t_{D(4)}$ from 40 ns to 20 ns.
28	Modified pulse markings in waveform diagrams. Added Typ value of 15 ns for Symbol $t_{D(3)}$.
29	Changed Min column for Symbols $t_{H(1)}$ and $t_{H(2)}$ from 3 ns to 6 ns. Added note.

Page Number of Updated Data Sheet	Summary of the Change
30	Modified waveform diagram and added first note. Changed Min value of t_{SU} from 19 to 12 ns.
31	Modified waveform diagram and added first note. Changed Min value of t_{SU} from 19 to 12 ns. Added last sentence to second note.
36	Increased values in Max column for Symbols $t_{D(1)}$, $t_{F(1)}$, $t_{D(2)}$ and $t_{PW(2)}$.
37	Increased values in Max column for Symbols $t_{D(1)}$ and $t_{PW(2)}$. Corrected error in Parameter column for Symbol t_f. Added Min value of 0 ns for Symbol $t_{SU(4)}$.
38	Added Max value for Symbol $t_{D(1)}$. Increased Max values for Symbols t_F and $t_{PW(2)}$. Added the notes.
39	Increased Max value for Symbol $t_{PW(2)}$. Added Min value of 0 ns for Symbol $t_{SU(4)}$. Added the note.
40-41	Modified last sentence of last paragraph on page 40 and added the footnote.
41	Modified second and third paragraphs of VTAIS and Path AIS Insertion at Receive Terminal Interface subsection.
42	Modified diagram and note of Figure 18.
43	Modified diagram and note of Figure 19.
44	Modified last row of table and diagram of Figure 20.
45	Added Pointer Tracking Interpretation subsection.
46	Added Figure 21.
49	Clarified non-path terminating mode in first paragraph.
50	Modified diagram of Figure 23.
61 and 62	Modified Note 1.
63	Modified first paragraph of Description column for Symbol Z23.
65	Modified table and last paragraph of Description column for Symbol H41.
67	Modified table and last paragraph of Description column for Symbol H42.
68	Modified table and last paragraph of Description column for Symbol H43.
75	In Description column for Symbols Z21, Z22 and Z23, changed second paragraph and “Action” column text in last two rows of final table.
85	Changed “LOP to AIS” to “AIS to LOP” in Description column for Symbol CCITT.
86	Changed figure references in first paragraph for Symbols PTE21 and PTE11. Added last sentence to Description column for Symbol RING.
88	Added Note 1 and references to this Note for Address 3E2.
89	Changed Description column for Symbols TPRDI1 and SRAIS1.
90	Added last sentence to Description column for Symbol Z2FEBE.
91	Added last sentence to Description column for Symbol TPLEV.
94-97	Added Note to first paragraph of Description column for bits 6-0 of Address 3E5.
98	Added references to bit RAISE in Description column for Symbols TPRDI3, TPRDI2.
98-99	Added Note at end of Description column for bits 7-2 at Address 3E6.
100	Added MODE0 column to table in Description column for symbol STIME.

Page Number of Updated Data Sheet	Summary of the Change
100-101	Added Note to Description column for every bit at Address 3E7. Modified Description column for Symbols ELOM3, ELOM2 and ELOM1.
102	Clarified Description column for Symbols C2R1, C2R2 and C2R3. Added Note to Description column for Symbols C2R2 and C2R3. Added last two sentences to Description column for Symbol INVCI. Modified Description column for Symbol RDPAR.
103	Clarified Description column for Symbols RLOS, ROOF, RLOF, RPAIS3, RPAIS2 and RPAIS1.
104	Added Note to Description column for Symbols RLOP3, RLOP2 and RLOP1. Made minor clarifications to Description column for Symbols RLOP3, RLOP2, RLOP1, RLOM3, RLOM2 and RLOM1
104-105	Added references to MODE0 pin effect to Description column for Symbols RLOM3, RLOM2 and RLOM1.
106	Clarified Description column for Symbol APNAPS.
109	Added Interrupt Mask Bit Registers subsection.
110	Modified Description column for Symbol dbK1K2.
111	Added last sentence to Description column for Symbol dbK1K2AP.
112	Removed reference to socket mounting of package. Added part number to top view diagram.
113	Changed TXC-03452 to TXC-03452B.
114-115	Updated contents of Standards Documentation Sources section.
116-118	Added List of Data Sheet Changes.

- NOTES -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