SOT-1 Device
SONET STS-1 Overhead Terminator
TXC-03001

DATA SHEET
Preliminary

FEATURES

- Provides SONET interface to any type of payload
- Programmable STS-1 or STS-N modes
- Receive bit-serial STS-1 signal in the line side using external reference frame pulse input for STS-N applications
- Transmit bit-serial STS-1 signal from the line side using external reference frame pulse for outgoing phase synchronization
- Programmable: full STS-1 or SPE-only I/O on the terminal side
- Bit-serial or byte-parallel I/O on the terminal side
- Optional AIS communication with peer SOT-1 or SOT-3
- Interfaces to microprocessors with hierarchical scan and optional hardware interrupt on alarms
- SONET alarm processing and performance monitoring
- Meets 1991 ANSI/Bellcore standards:
  - T1X1.5/90-025R1
  - TA-NWT-000253

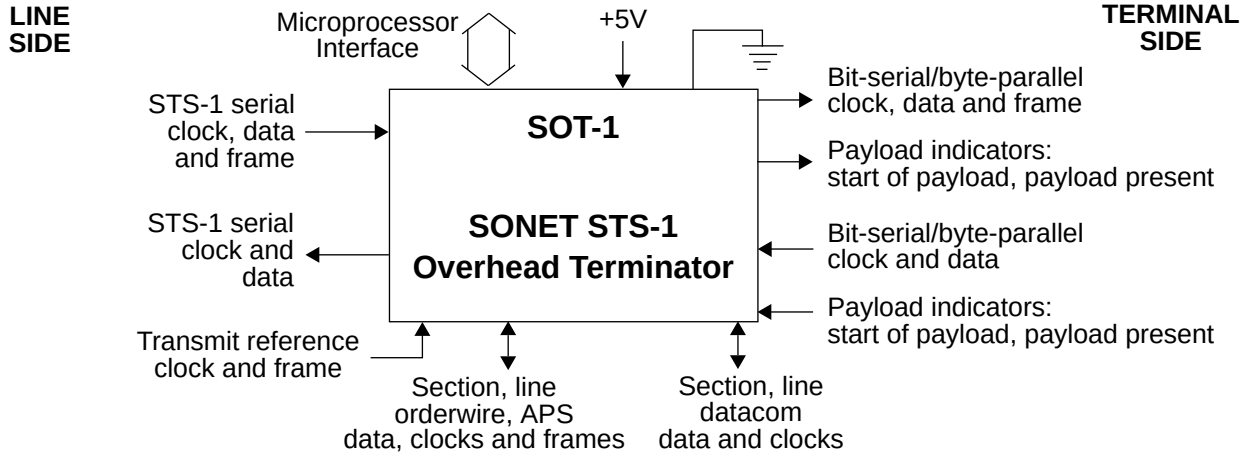
DESCRIPTION

The SOT-1 SONET/STS-1 Overhead Terminator performs section, line and path overhead processing for STS-1 SONET signals. This versatile device can be used anywhere in a SONET network where STS-1 signals are in use, i.e., repeaters and line or path termination points. Interfaces are provided for both section and line orderwire and datacom channels. Further, control bits in the memory map enable the SOT-1 to perform loopback, and serial or parallel I/O. Line side and terminal side clock rates can differ. The receive/transmit pointer is recalculated as necessary to compensate for the differences in these clocks.

All overhead bytes are stored in on-chip RAM. New overhead bytes can be substituted from RAM to either the terminal or line side, depending on the application. The SOT-1 also provides alarm detection and AIS generation, as well as software and hardware interrupt in the event of errors.

APPLICATIONS

- SONET W-DCS/B-DCS
- High speed data communication
- Payload extraction, introduction into STS-1
- STS-N multiplexer
- SONET test sets



PRELIMINARY information documents contain information on products in the sampling, pre-production or early production phases of the product life cycle. Characteristic data and other specifications are subject to change. Contact TranSwitch Applications Engineering for current information on this product.

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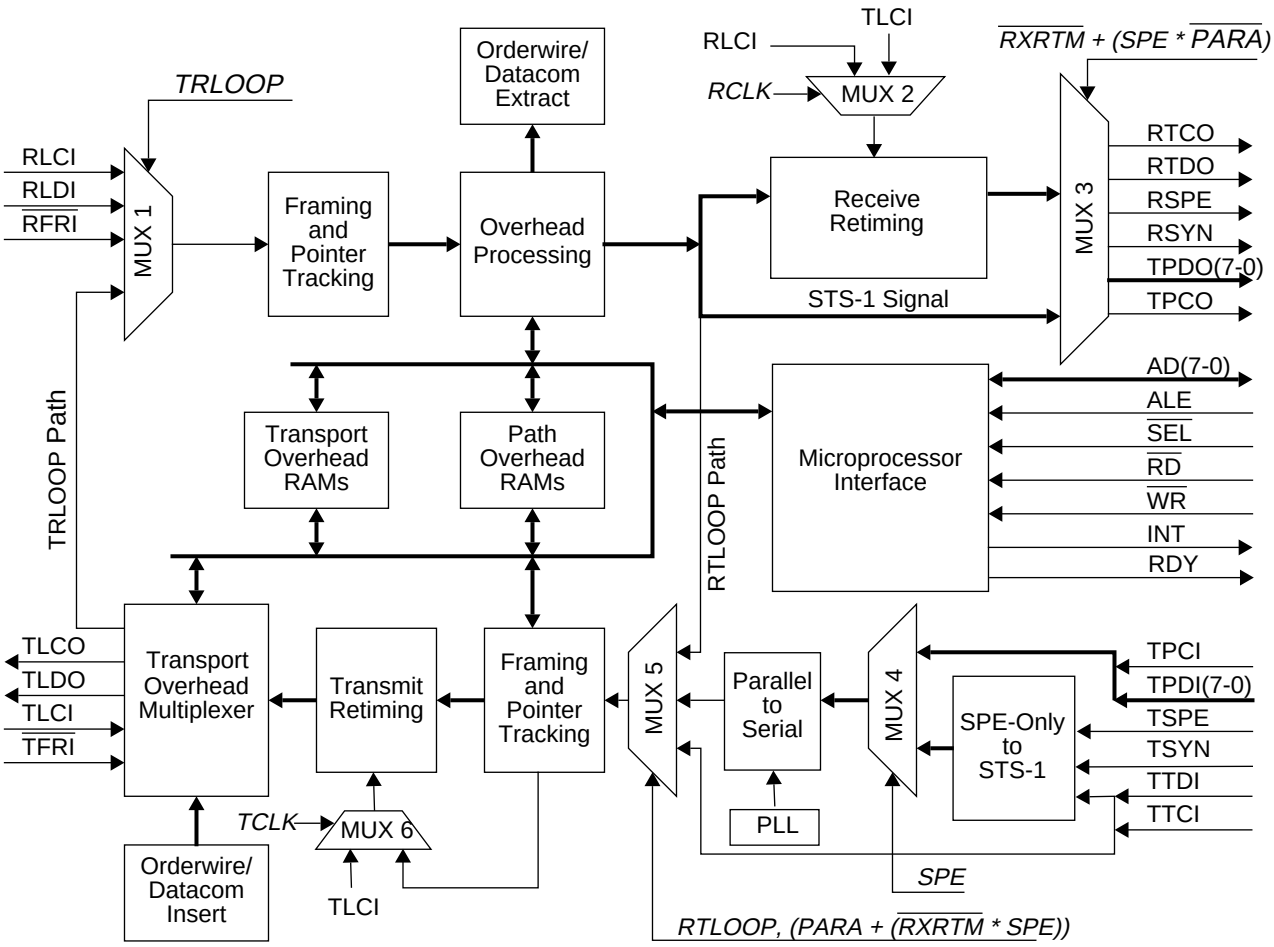
BLOCK DIAGRAM



Note: Names in italics are internal control bits.

Figure 1. SOT-1 Block Diagram

BLOCK DIAGRAM DESCRIPTION

The block diagram of the SOT-1 is shown in Figure 1. The input multiplexer (MUX 1) selects either the line side input, or the looped back signal from transmit line output, as the input to the Framing and Pointer Tracking Block. The Framing and Pointer Tracking Block performs frame synchronization to the incoming STS-1 signal, serial to parallel conversion, and pointer tracking. Incoming STS-1 alarms are also detected. The Overhead Processing Block stores the line, section, and path overhead bytes into RAM locations for access by the microprocessor. It then optionally multiplexes the line, section, and path overhead bytes from the RAM locations written by the microprocessor. Incoming SONET performance monitoring functions as well as debouncing of selected overhead bytes are also performed by the Overhead Processing Block. The Orderwire/Datacom Extract Block extracts and routes the APS and the two orderwire bytes to the orderwire interface, and the section and line data communication bytes to the two datacom interfaces.

The Receive Retiming Block retimes the line input to the reference frequency, and performs pointer recalculation and SPE-only extraction. All transport overhead bytes are demultiplexed and the payload is retimed. The

reference clock used for retiming is selected by MUX 2 as either the line clock (RLCI) or the reference clock (TLCI). The terminal side output multiplexer (MUX 3) allows selection of either the output of the Overhead Processing Block or the output of the Receive Retiming Block.

In the transmit direction, the SPE-Only to STS-1 Block receives serial SPE-only signals from the terminal, and introduces framing and pointer bytes to produce a parallel STS-1 signal. The Parallel to Serial Block uses the phase-locked loop (PLL) to serialize either the data from the SPE-Only to STS-1 Block or parallel input from the terminal, as selected by MUX 4. The MUX 5 multiplexer selects for input to the Transmit Framing and Pointer Tracking Block either the looped back data from the output of the receive side Overhead Processing Block, or the output of the Parallel to Serial Block, or the serial STS-1 input from the terminal.

The Framing and Pointer Tracking Block performs frame synchronization to the serial STS-1 signal, serial to parallel conversion, and pointer tracking. Incoming STS-1 alarms are also detected. The section, line and path overhead bytes are stored into RAM locations for access by the microprocessor. The path overhead bytes are then optionally multiplexed from the RAM locations written by the microprocessor.

The Transmit Retiming Block performs retiming to the reference frequency and pointer recalculation. The Transport Overhead Multiplexer Block optionally multiplexes the section and line overhead bytes from the RAM written by the microprocessor. The Orderwire/Datacom Insert Block optionally multiplexes the orderwire, APS and datacom bytes from the orderwire interface and the two datacom interfaces into the transmit outgoing Transport Overhead RAM locations.

The Transport Overhead RAMs consist of locations for storing receive incoming transport overhead bytes, receive outgoing transport overhead bytes (written by the microprocessor), transmit incoming transport overhead bytes, and transmit outgoing transport overhead bytes. It also stores B1 and B2 performance monitors, and pointer justification counters. The RAMs also act as temporary storage for datacom and orderwire bytes received from the respective interfaces.

The Path Overhead RAMs consist of locations for storing receive incoming path overhead bytes, receive outgoing path overhead bytes (written by the microprocessor), transmit incoming path overhead bytes, and transmit outgoing path overhead bytes. The RAMs also store B3 and FEBE performance monitors.

The Microprocessor Interface provides access to the control registers, which select various modes of operation and status registers that report various alarm conditions. It also provides access to the Transport and Path Overhead RAMs, and provides both software and hardware interrupt capability based on the status of the chip.

When SPE = 1 in the serial mode (PARA = 0), the terminal output of the SOT-1 contains payload bits but no transport overhead, TOH (see the SOT-1 Memory Map section of this data sheet). The RSPE output provides a gapping signal for the SPE-only mode of operation. Nominally, there are 8 x 3 = 24 bits of TOH and 8 x 87 = 696 bits of payload. For this circumstance, the RSPE provides 24 equally spaced gaps in the output data (720/24 = 30, every 30th bit is gapped). When there is an increment in the pointer, there must be 32 equally spaced gaps, and when there is a decrement, there are 16 equally spaced gaps for the row containing the pointer bytes.

PIN DIAGRAM

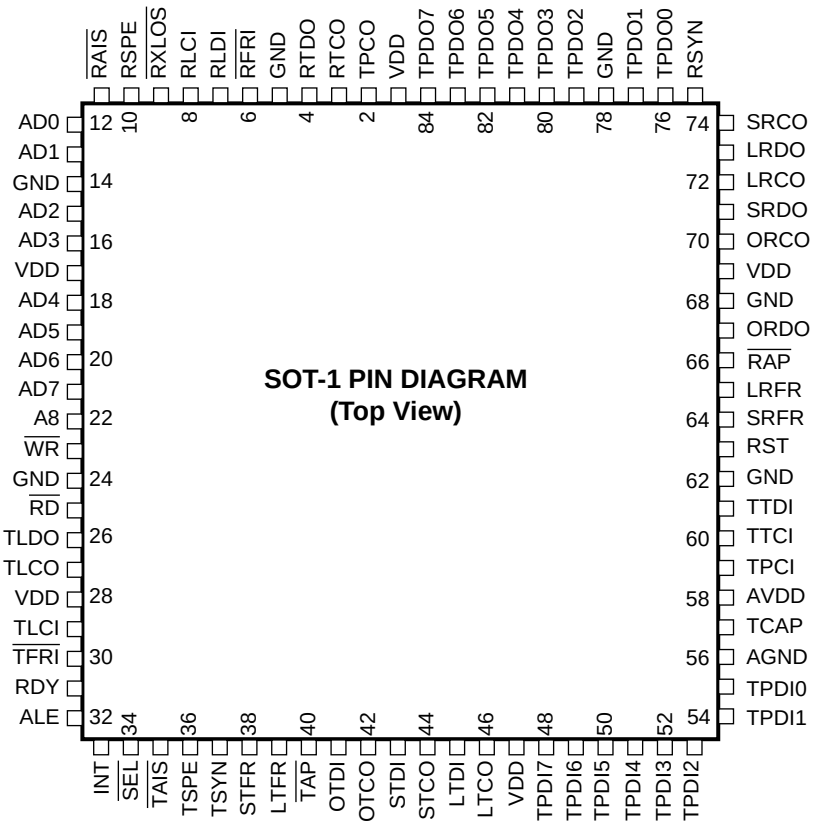


Figure 2. SOT-1 Pin Diagram

PIN DESCRIPTIONS

Power Supply and Ground

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	1,17,28,47,69	P		**Power Supply:** +5-volt supply voltage, +/- 5%
AVDD	58	P		**Analog Power:** +5 volts, +/- 5%
GND	5,14,24,62,68 78	P		**Digital Ground**
AGND	56	P		**Analog Ground**

*Note: I = Input; O = Output; P = Power; OD = Open Drain Output

Microprocessor Bus Interface

Symbol	Pin No.	I/O/P	Type *	Name/Function
AD(7-4) AD(3-2) AD(1-0)	21-18 16-15 13-12	I/O	TTL8mA	**Address/Data Bus:** These signal leads constitute the time-multiplexed address and bidirectional data bus.
A8	22	I	TTL	**Address Bus - Bit 8:** Bit 8 of the address bus.
$\overline{WR}$	23	I	TTLp	**Write:** An active low signal generated by the microprocessor for writing to the SOT-1.
$\overline{RD}$	25	I	TTLp	**Read:** An active low signal generated by the microprocessor for reading the SOT-1.
RDY	31	OD	OD16mA	**Ready:** A high is an active acknowledgment from the SOT-1 indicating that the transfer can be completed. The RDY line will go low whenever the address being read or written to corresponds to a RAM location. When status or control registers are accessed, RDY remains high. The RDY lead is an open drain capable of sinking a maximum of 16 mA. The value of the pull-up resistor value depends on the number of devices that use the RDY signal in the system.
ALE	32	I	TTLp	**Address Latch Enable:** An active high input signal provided by the microprocessor to latch the address into a SOT-1 address latch for a bus cycle.
INT	33	O	TTL4mA	**Interrupt:** A high on this pin signals an interrupt request for the microprocessor. The hardware interrupt request is enabled by HINT=1 (bit 5, address 0FA).
$\overline{SEL}$	34	I	TTLp	**Select:** An active low signal which enables data transfers between the microprocessor and SOT-1 RAM during a read/write bus cycle.
RST	63	I	TTL	**Reset:** Resets all internal counters and sets all alarms except RLOC. RST is a positive pulse with a minimum width of 300 ns. It must be used after power is applied, registers are initialized, and the clocks are stable.

Receive Line Side Interface:

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{RFRI}$	6	I	CMOSp	**Receive Line Frame In:** An optional active low frame pulse that occurs during the C1 byte, bit 7 time. When used, it reduces the OOF exit time from two frames to one frame.
RLDI	7	I	CMOS	**Receive Line Data In:** Incoming serial STS-1/STS-N data which is clocked into the SOT-1 on the rising edge of RLCI.

*See Input, Output and I/O Parameters section below for Type definitions.

Symbol	Pin No.	I/O/P	Type	Name/Function
RLCI	8	I	CMOS	**Receive Line Clock In:** A 51.84 MHz clock that clocks in the serial data and the optional framing pulse. RLCI is used as the time base for framing, pointer tracking, and demultiplexing the transport overhead bytes, and for RAM access in the receive side.
$\overline{\text{RXLOS}}$	9	I	TTLp	**Receive Loss of Signal:** An active low external loss of signal indication from a higher multiplexer such as an SM3. SOT-1 combines $\overline{\text{RXLOS}}$ with the internal loss of signal and reports the result to the microprocessor as the RLOS status bit.

Transmit Line Side Interface:

Symbol	Pin No.	I/O/P	Type	Name/Function
TLDO	26	O	CMOS4mA	**Transmit Line Data Out:** Outgoing serial STS-1/ STS-N data which is clocked out of the SOT-1 on the falling edge of TLCO.
TLCO	27	O	CMOS4mA	**Transmit Line Clock Out:** An outgoing serial STS-1/ STS-N clock. Depending on the operating mode, TLCO is derived from TLCI, TTCI or TPCI.
TLCI	29	I	CMOS	**Transmit Line Clock In:** The 51.84 MHz reference clock input.
$\overline{\text{TFRI}}$	30	I	CMOSp	**Transmit Frame Reference In:** An optional active low frame pulse, synchronous with TLCI, which determines outgoing A1, A2 epoch. $\overline{\text{TFRI}}$ can be used only if TCLK=1 (bit 6, address 1FA).

Orderwire/APS Interface:

Symbol	Pin No.	I/O/P	Type	Name/Function
STFR	38	O	TTL4mA	**Transmit Section Orderwire Framing Pulse:** Transmit frame pulse for section orderwire codec/filter.
LTFR	39	O	TTL4mA	**Transmit Line Orderwire Framing Pulse:** Transmit frame pulse for line orderwire codec/filter.
$\overline{\text{TAP}}$	40	O	TTL4mA	**Transmit APS Framing Pulse:** An active low signal which occurs one clock cycle before the MSB of the K1 byte is expected in the serial bit stream (OTDI).
OTDI	41	I	TTLp	**Transmit Orderwire Byte and APS Byte Input:** The two orderwire bytes and APS bytes are clocked into the SOT-1 on negative transitions of OTCO.
OTCO	42	O	TTL4mA	**Transmit Orderwire and APS Clock:** A 576 KHz clock, synchronous to TLCO, which is used for sourcing the orderwire and APS bytes into the SOT-1.

Symbol	Pin No.	I/O/P	Type	Name/Function
SRFR	64	O	TTL4mA	**Receive Section Orderwire Framing Pulse:** Receive frame pulse for section orderwire codec/filter.
LRFR	65	O	TTL4mA	**Receive Line Orderwire Framing Pulse:** Receive frame pulse for line orderwire codec/filter.
$\overline{\text{RAP}}$	66	O	TTL4mA	**Receive APS Framing Pulse:** An active low signal which occurs one clock cycle after the LSB of the first K2 byte in the serial bit stream (ORDO).
ORDO	67	O	TTL4mA	**Receive Orderwire Byte and APS Byte Output:** The two orderwire bytes and APS bytes are clocked out of the SOT-1 on positive transitions of ORCO.
ORCO	70	O	TTL4mA	**Receive Orderwire and APS Clock:** A 576 KHz clock, derived from RLCI, which is used for clocking the orderwire and APS bytes from the SOT-1.

Section and Line Data Communication Interface:

Symbol	Pin No.	I/O/P	Type	Name/Function
STDI	43	I	TTLp	**Transmit Section Data Communication Data Input:** Serial 192 Kbit/s data (D1 - D3 bytes) is clocked into the SOT-1 on positive transitions of the clock STCO.
STCO	44	O	TTL4mA	**Transmit Section Data Communication Clock Output:** A 192 KHz clock, derived from TLCO, which is used for sourcing the section data communication data into the SOT-1.
LTDI	45	I	TTLp	**Transmit Line Data Communication Data Input:** Serial 576 Kbit/s data (D4 - D12 bytes) is clocked into the SOT-1 on positive transitions of the clock LTCO.
LTCO	46	O	TTL4mA	**Transmit Line Data Communication Clock Output:** A 576 KHz clock, derived from TLCO, which is used for sourcing the line data communication data into the SOT-1.
SRDO	71	O	TTL4mA	**Receive Section Data Communication Data Output:** Serial 192 Kbit/s data (D1 - D3 bytes) is clocked out of the SOT-1 on negative transitions of the clock SRCO.
LRCO	72	O	TTL4mA	**Receive Line Data Communication Clock Output:** A 576 KHz clock, derived from RLCI, which is used for clocking out the line data communication data.
LRDO	73	O	TTL4mA	**Receive Line Data Communication Data Output:** Serial 576 Kbit/s data (D4 - D12 bytes) is clocked out of the SOT-1 on negative transitions of the clock LRCO.

Symbol	Pin No.	I/O/P	Type	Name/Function
SRCO	74	O	TTL4mA	**Receive Section Data Communication Clock Output:** A 192 KHz clock, derived from RLCI, which is used for clocking out the section data communication data.

Terminal Side Interface:

Symbol	Pin No.	I/O/P	Type	Name/Function
RTCO	3	O	CMOS4mA	**Receive Terminal Clock Output:** The 51.84 MHz terminal clock, used for clocking out the serial data RTDO. Depending on operating mode, RTCO can be derived either from RLCI or TLCI.
RTDO	4	O	CMOS4mA	**Receive Terminal Data Output:** Serial 51.84 Mbit/s STS-1 receive data. Data is clocked out of the SOT-1 on negative transitions of the clock RTCO.
RSPE	10	O	CMOS4mA	**Receive Terminal SPE Indication:** An active high signal indicating the synchronous payload envelope in the terminal data output, RTDO or TPDO. For SPE-only, the RSPE output is a gapping signal.
RSYN	75	O	CMOS4mA	**Receive Terminal Sync Pulse:** RSYN is high during the C1 byte and J1 byte of RTDO or TPDO. In serial SPE-only mode, RSYN is high only during the J1 byte of RTDO.
TPCO	2	O	TTL4mA	**Terminal Parallel Clock Output:** The 6.48 MHz clock, derived from RTCO, that clocks out receive terminal byte data TPDO.
TPDO(7-2) TPDO(1-0)	84-79 77-76	O	TTL4mA	**Terminal Parallel Data Output:** Byte-wide 6.48 Mbyte/s receive terminal data which is clocked out of the SOT-1 on positive transitions of the clock TPCO.
TTCI	60	I	CMOS	**Transmit Terminal Serial Clock Input:** A 51.84 MHz terminal clock used for clocking in serial data (TTDI), as well as transmit SPE indication (TSPE) and the transmit sync pulse (TSYN).
TTDI	61	I	CMOS	**Transmit Terminal Data Input:** Serial 51.84 Mbit/s transmit terminal data which is clocked into the SOT-1 on positive transitions of the clock TTCI.
TSPE	36	I	CMOS	**Transmit Terminal SPE Indication:** Required input for the SPE-only mode. A high value indicates the location of the SPE bits in the data input, TTDI. A low value identifies the location of a gap in the input data.
TSYN	37	I	CMOS	**Transmit Terminal Sync Pulse:** Required input for the SPE-only mode. TSYN must be high during incoming J1 byte of TTDI in the SPE-only mode.

Symbol	Pin No.	I/O/P	Type	Name/Function
TPCI	59	I	TTL	**Terminal Parallel Clock Input:** A 6.48 MHz clock used for clocking in terminal transmit data TPDI.
TPDI(7-0)	48-55	I	TTL	**Terminal Parallel Data Input:** Byte-wide 6.48 Mbyte/s transmit terminal data. Data is clocked into the SOT-1 on positive transitions of the clock TPCI.

Alarm Indication Ports:

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{RAIS}}$	11	O	TTL4mA	**Receive Alarm Indication Signal:** An active low signal indicating a downstream AIS must be generated under the conditions indicated in the Receive Alarm Propagation Table section below as resulting in action code 'A'.
$\overline{\text{TAIS}}$	35	I	TTLp	**Transmit Alarm Indication Signal:** An active low input causes AIS to be introduced into transmit line, as indicated in the '$\overline{\text{TAIS}}$ pin is low', column of the Transmit Alarm Propagation Table section below.

Phase-Locked Loop:

Symbol	Pin No.	I/O/P	Type	Name/Function
TCAP	57	I/O		**External Resistor/Capacitor:** A 1.2 Kohm, 1/4 watt, 5% carbon composition resistor in series with a 1000 pF capacitor connected to analog ground. The RC network is required when the terminal interface is used in the following modes: 1. Byte-parallel 2. SPE-only

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	+7.0	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Continuous power dissipation	P_C		825	mW
Ambient operating temperature	T_A	-40	85	^oC
Operating junction temperature	T_J		125	^oC
Storage temperature range	T_S	-55	150	^oC

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		32	34	$^oC/W$	

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
V_{ANALOG}	4.75	5.0	5.25	V	
I_{DD}		130	150	mA	
I_{ANALOG}		5	7	mA	
P_{DD}		650	788	mW	Output switching
P_{ANALOG}		25	37	mW	

INPUT, OUTPUT, AND I/O PARAMETERS

Input Parameters For CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			1.65	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Input Parameters For CMOSp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		0.5	1.4	mA	$V_{DD} = 5.25$; Input = 0 volts
Input capacitance		5.5		pF	

Note: Input has a 100K (nominal) internal pull-up resistor.

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Input Parameters For TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		0.5	1.4	mA	$V_{DD} = 5.25$; Input = 0 volts
Input capacitance		5.5		pF	

Note: Input has a 9K (nominal) internal pull-up resistor.

Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.8	6.5	9.2	ns	C_{LOAD} = 15 pF
t_{FALL}	1.3	2.3	3.4	ns	C_{LOAD} = 15 pF

Output Parameters For CMOS4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	1.4	2.9	4.2	ns	C_{LOAD} = 15 pF
t_{FALL}	1.3	2.3	3.4	ns	C_{LOAD} = 15 pF

Input/Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 $\leq V_{DD} \leq$ 5.25
V_{IL}			0.8	V	4.75 $\leq V_{DD} \leq$ 5.25
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		5.5		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.8	6.5	9.2	ns	C_{LOAD} = 15 pF
t_{FALL}	1.3	2.3	3.4	ns	C_{LOAD} = 15 pF

Input/Output Parameters For TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -4.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 8.0$
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	2.4	4.9	7.0	ns	$C_{LOAD} = 25$ pF
t_{FALL}	1.1	1.8	2.5	ns	$C_{LOAD} = 25$ pF

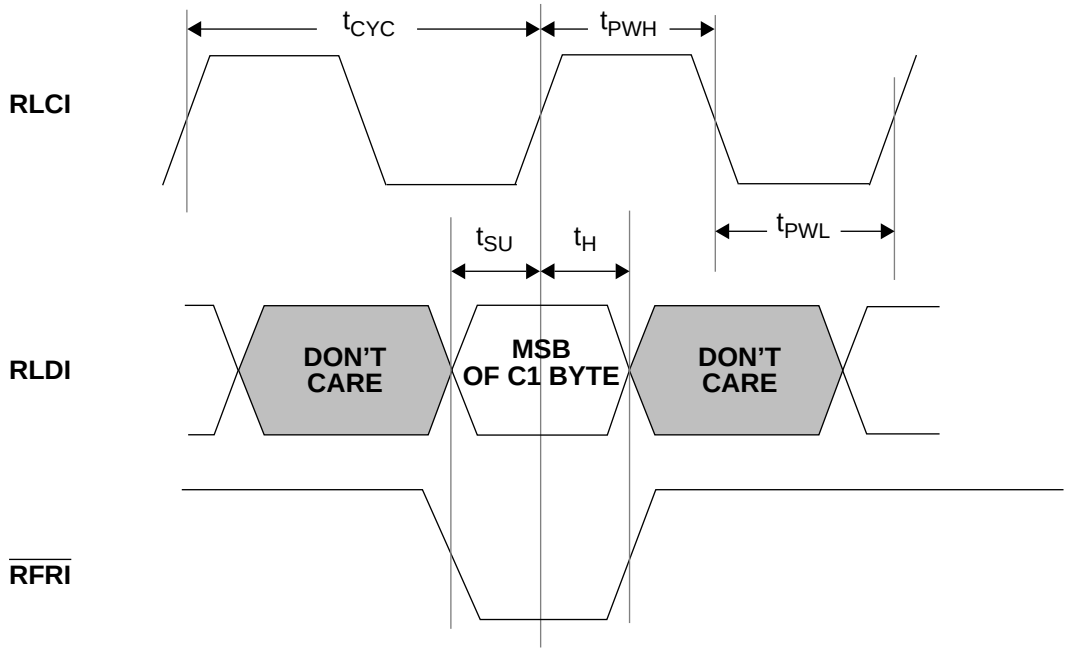
Output Parameters for OD16mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 16.0$
I_{OL}			16.0	mA	
t_{FALL}	0.8	1.0	1.5	ns	$C_{LOAD} = 15$ pF

TIMING CHARACTERISTICS

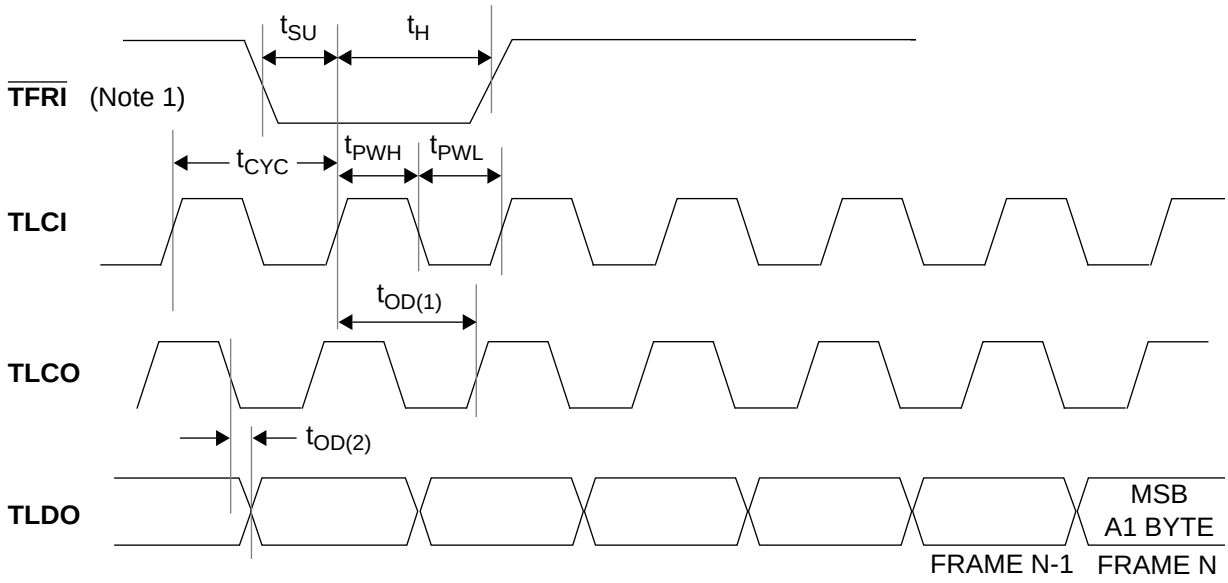
Detailed timing diagrams for the SOT-1 are illustrated in Figures 3 through 20, with values of the timing intervals following each figure. All output times are measured with a maximum 15 pF load capacitance. Timing parameters are measured at (V_{OH} - V_{OL})/2 or (V_{IH} - V_{IL})/2, as applicable.

Figure 3. Line Side Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
RLCI clock period	t_{CYC}	19.25	19.29		ns
RLCI high time	t_{PWH}	8.68	9.65	10.61	ns
RLCI low time	t_{PWL}	8.68	9.65	10.61	ns
RLDI/$\overline{\text{RFRI}}$ set-up time to RLCI$\uparrow$	t_{SU}	4			ns
RLDI/$\overline{\text{RFRI}}$ hold time after RLCI$\uparrow$	t_H	2			ns

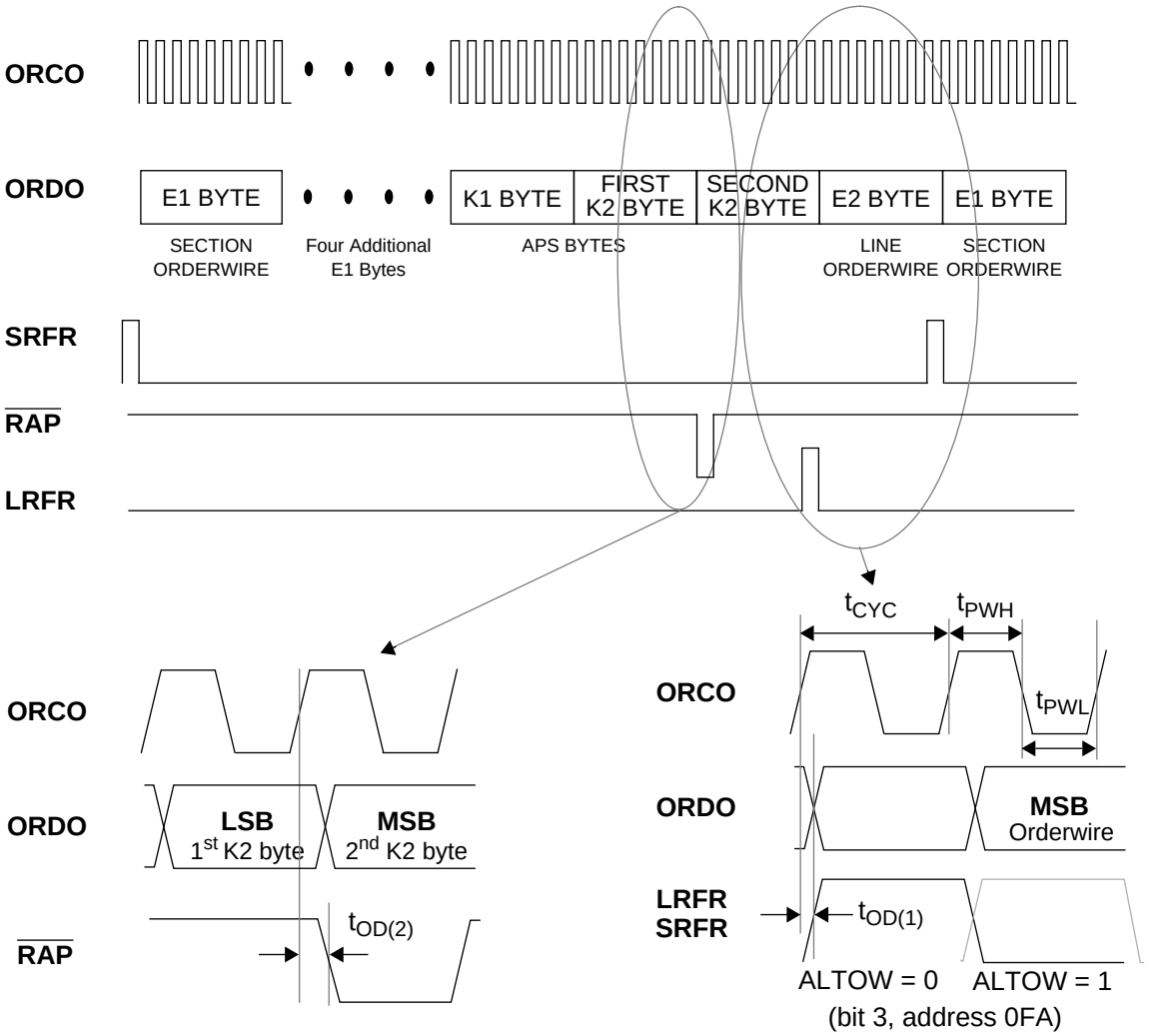
Figure 4. Line Side Output Timing



Parameter	Symbol	Min	Typ	Max	Unit
TLCI clock period (Note 2)	t_{CYC}	19.285	19.290	19.295	ns
TLCI high time	t_{PWH}	8.68	9.65	10.61	ns
TLCI low time	t_{PWL}	8.68	9.65	10.61	ns
$\overline{\text{TFRI}}$ set-up time to TLCI↑	t_{SU}	4			ns
$\overline{\text{TFRI}}$ hold time after TLCI↑	t_H	2			ns
TLCO output delay after TLCI↑	$t_{OD(1)}$	6	15	24	ns
TLDO output delay after TLCO↓	$t_{OD(2)}$	-1	0	3	ns

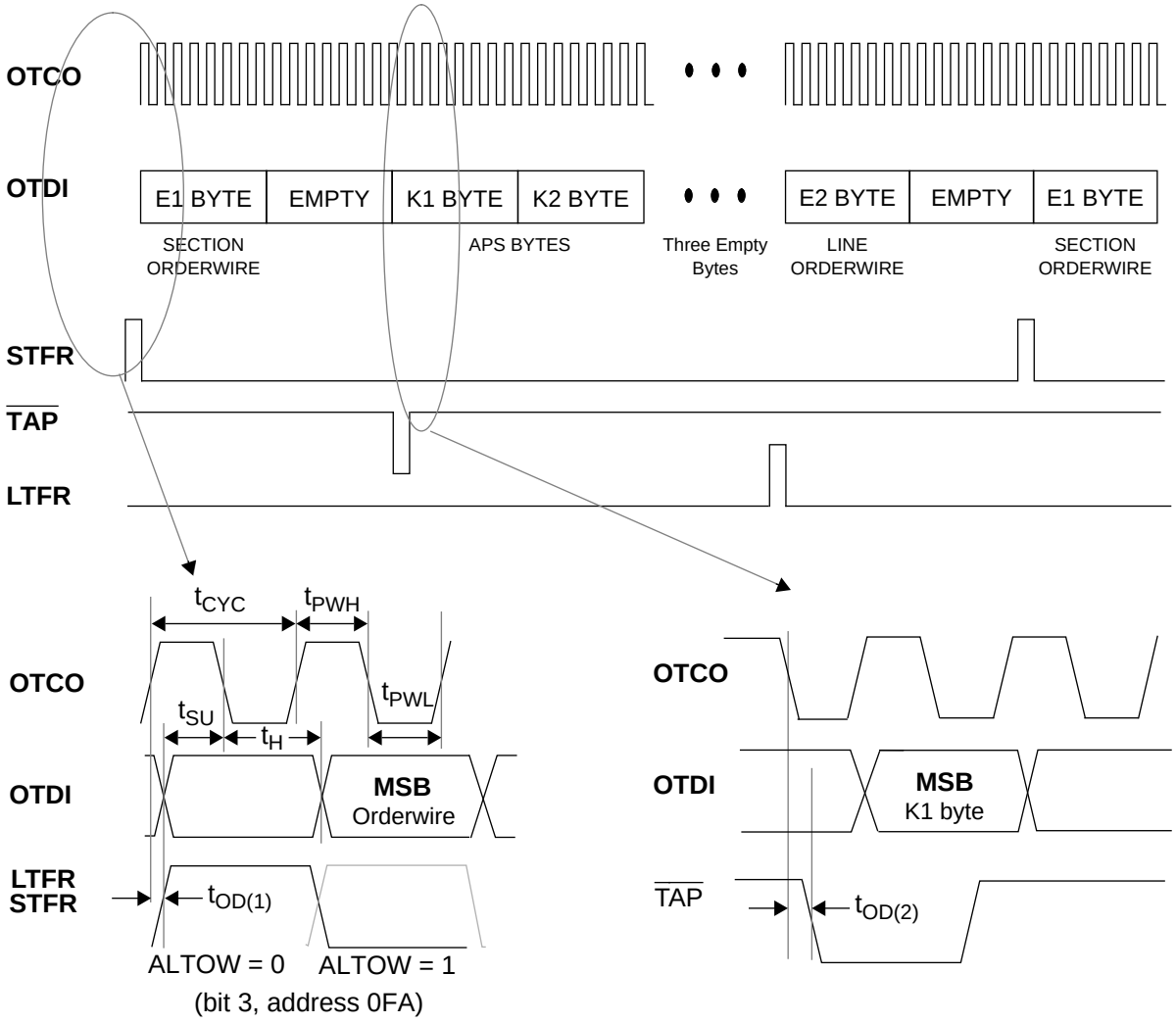
Note 1. $\overline{\text{TFRI}}$ can only be used if the control bit TCLK = 1.
Note 2. TLCI should not be operated outside of the range of 51.830 to 51.850 MHz: Data errors may occur and a reset of the device may be required after the clock frequency is returned to the normal operating range.

Figure 5. APS and Orderwire Output Timing



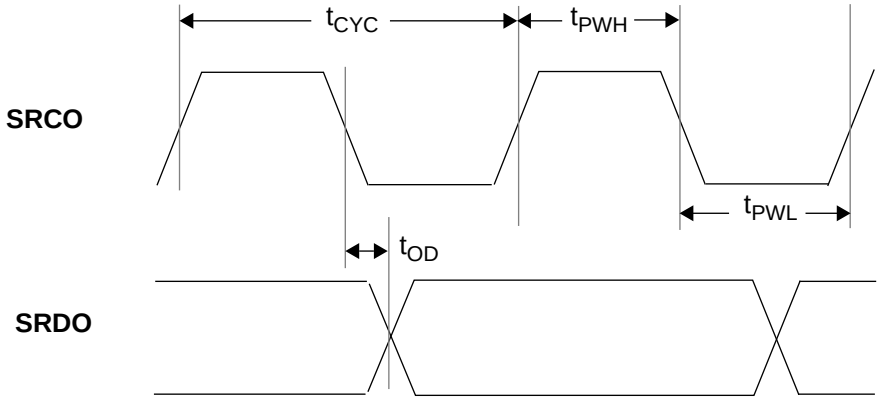
Parameter	Symbol	Min	Typ	Max	Unit
ORCO clock period	t_{CYC}	1732	1736		ns
ORCO high time	t_{PWH}	860	868	875	ns
ORCO low time	t_{PWL}	860	868	875	ns
SRFR, LRFR output delay after ORCO↑	$t_{OD(1)}$	1		5	ns
$\overline{RAP}$ output delay after ORCO↑	$t_{OD(2)}$	1		5	ns

Figure 6. APS and Orderwire Input Timing



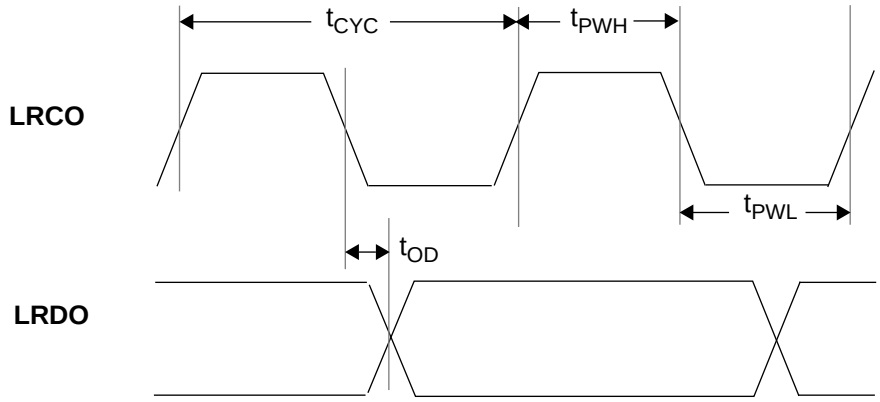
Parameter	Symbol	Min	Typ	Max	Unit
OTCO clock period	t_{CYC}	1732	1736		ns
OTCO high time	t_{PWH}	860	868	875	ns
OTCO low time	t_{PWL}	860	868	875	ns
OTDI set-up time to OTCO↓	t_{SU}	7			ns
OTDI hold time after OTCO↓	t_H	3			ns
STFR, LTFR output delay after OTCO↑	$t_{OD(1)}$	2		5	ns
$\overline{TAP}$ output delay after OTCO↓	$t_{OD(2)}$	2		5	ns

Figure 7. Section Datacom Channel Output Timing



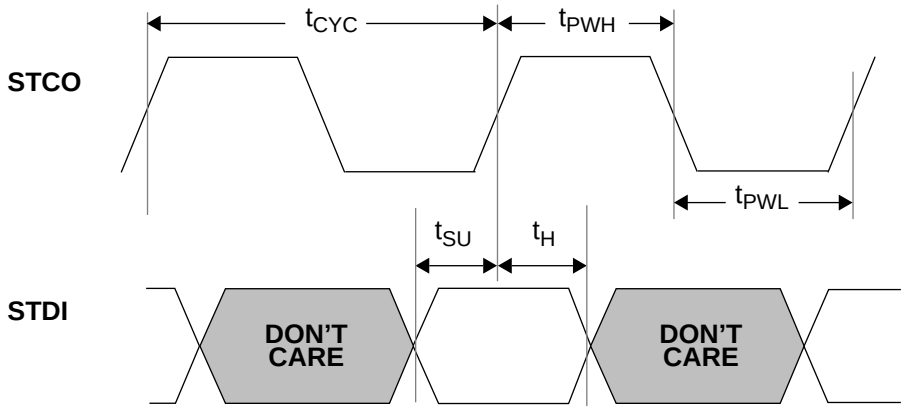
Parameter	Symbol	Min	Typ	Max	Unit
SRCO clock period	t_{CYC}	5.20	5.21	5.22	µs
SRCO high time	t_{PWH}	2.59	2.60	2.61	µs
SRCO low time	t_{PWL}	2.59	2.60	2.61	µs
SRDO output delay after SRCO↓	t_{OD}	2	4	5	ns

Figure 8. Line Datacom Channel Output Timing



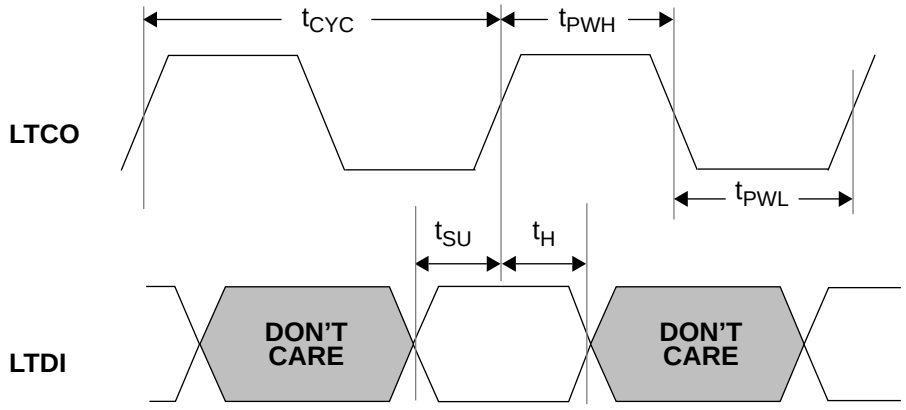
Parameter	Symbol	Min	Typ	Max	Unit
LRCO clock period	t_{CYC}	1732	1736		ns
LRCO high time	t_{PWH}	860	868	875	ns
LRCO low time	t_{PWL}	860	868	875	ns
LRDO output delay after LRCO↓	t_{OD}	2	4	5	ns

Figure 9. Section Datacom Channel Input Timing



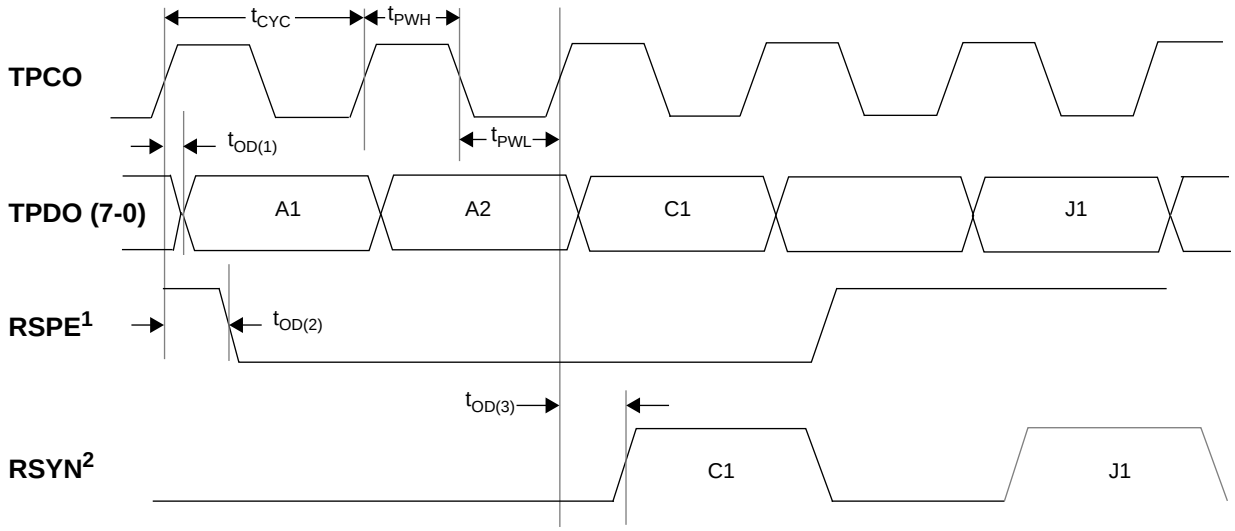
Parameter	Symbol	Min	Typ	Max	Unit
STCO clock period	t_{CYC}	5.20	5.21	5.22	µs
STCO high time	t_{PWH}	2.59	2.60	2.61	µs
STCO low time	t_{PWL}	2.59	2.60	2.61	µs
STDI set-up time to STCO↑	t_{SU}	7			ns
STDI hold time after STCO↑	t_H	3			ns

Figure 10. Line Datacom Channel Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
LTCO clock period	t_{CYC}	1732	1736		ns
LTCO high time	t_{PWH}	860	868	875	ns
LTCO low time	t_{PWL}	860	868	875	ns
LTDI set-up time to LTCO↑	t_{SU}	7			ns
LTDI hold time after LTCO↑	t_H	3			ns

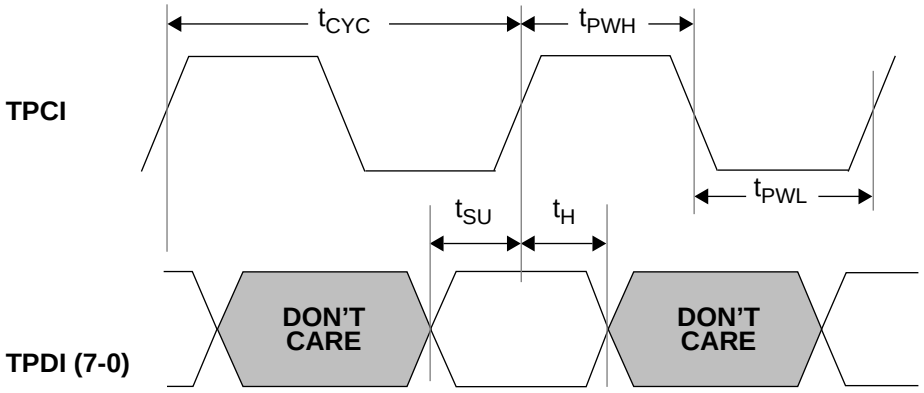
Figure 11. Terminal Parallel STS-1 Output Timing



Parameter	Symbol	Min	Typ	Max	Unit
TPCO clock period	t_{CYC}	154.0	154.3		ns
TPCO high time	t_{PWH}	72.2	77.2	82.2	ns
TPCO low time	t_{PWL}	72.2	77.2	82.2	ns
TPDO output delay after TPCO↑	$t_{OD(1)}$	7	12	19	ns
RSPE output delay after TPCO↑	$t_{OD(2)}$	52.9	57.9	62.9	ns
RSYN output delay after TPCO↑	$t_{OD(3)}$	52.9	57.9	62.9	ns

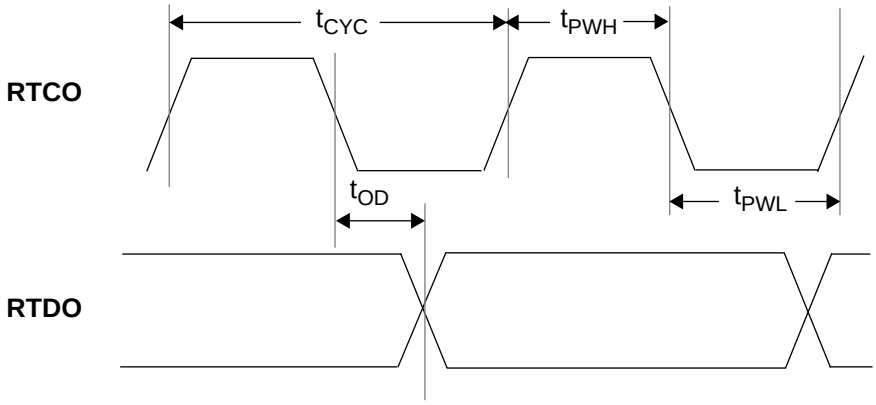
Note 1: Pointer movements are indicated by RSPE in subframe #4.
Note 2: J1 can be anywhere in the payload.

Figure 12. Terminal Parallel STS-1 Input Timing



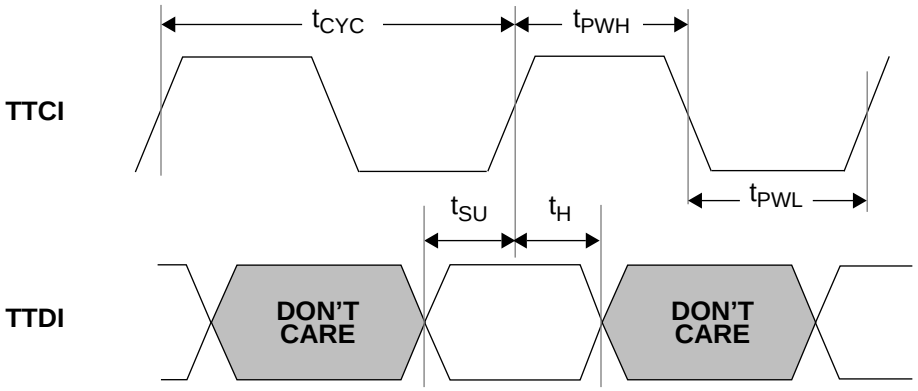
Parameter	Symbol	Min	Typ	Max	Unit
TPCI clock period	t_{CYC}	154.0	154.3		ns
TPCI high time	t_{PWH}	38.5	77.2	115.7	ns
TPCI low time	t_{PWL}	38.5	77.2	115.7	ns
TPDI set-up time to TPCI↑	t_{SU}	20			ns
TPDI hold time after TPCI↑	t_H	0			ns

Figure 13. Terminal Serial STS-1 Output Timing



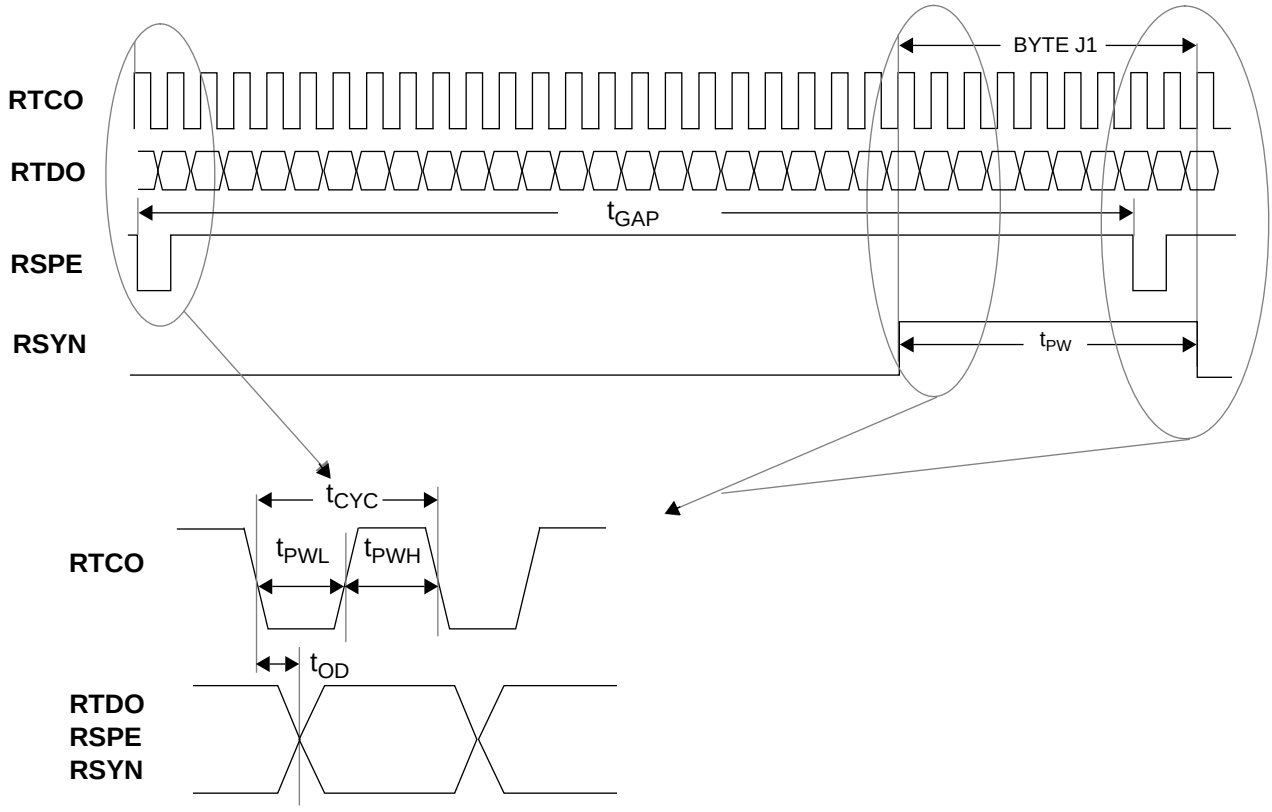
Parameter	Symbol	Min	Typ	Max	Unit
RTCO clock period	t_{CYC}	19.25	19.29		ns
RTCO high time	t_{PWH}	8.68	9.65	10.61	ns
RTCO low time	t_{PWL}	8.68	9.65	10.61	ns
RTDO output delay after RTCO↓	t_{OD}	-1		3	ns

Figure 14. Terminal Serial STS-1 Input Timing



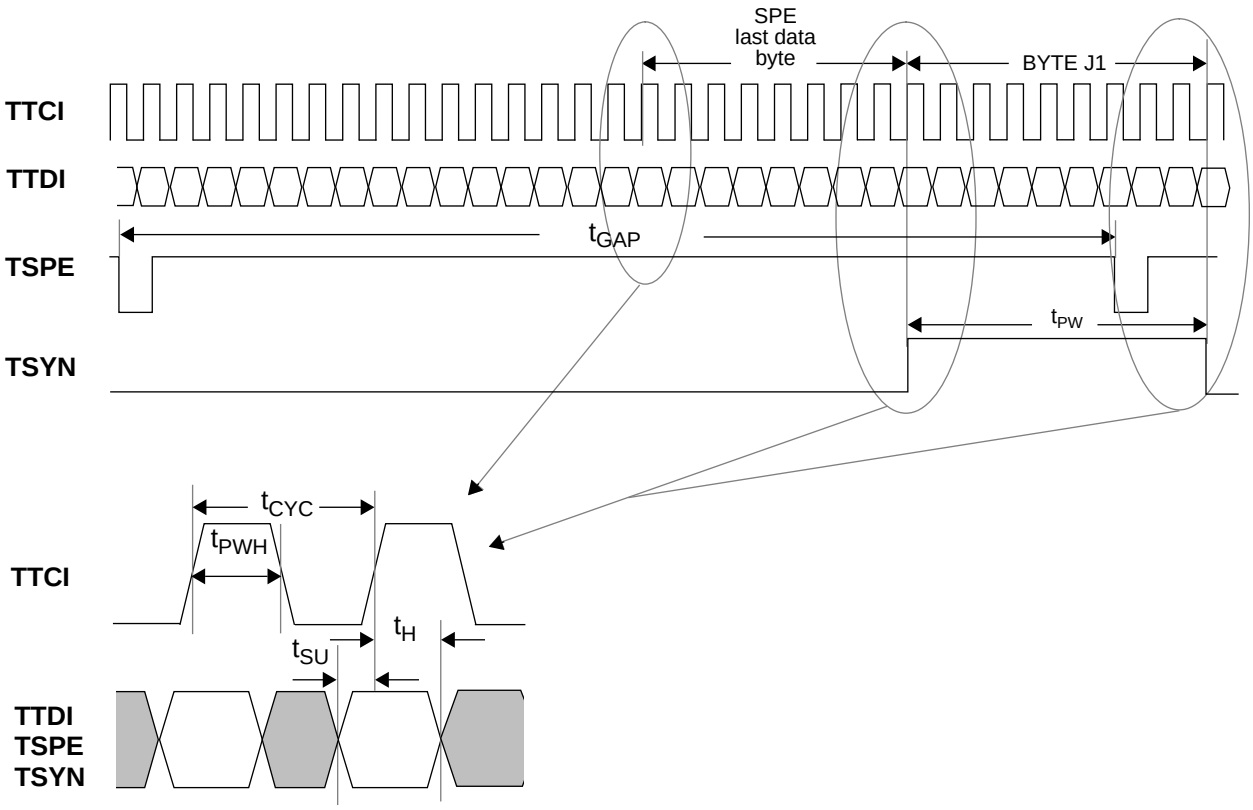
Parameter	Symbol	Min	Typ	Max	Unit
TTCI clock period	t_{CYC}	19.25	19.29		ns
TTCI high time	t_{PWH}	8.68	9.65	10.61	ns
TTCI low time	t_{PWL}	8.68	9.65	10.61	ns
TTDI set-up time to TTCI↑	t_{SU}	4			ns
TTDI hold time after TTCI↑	t_H	2			ns

Figure 15. Terminal Serial SPE-Only Output Timing



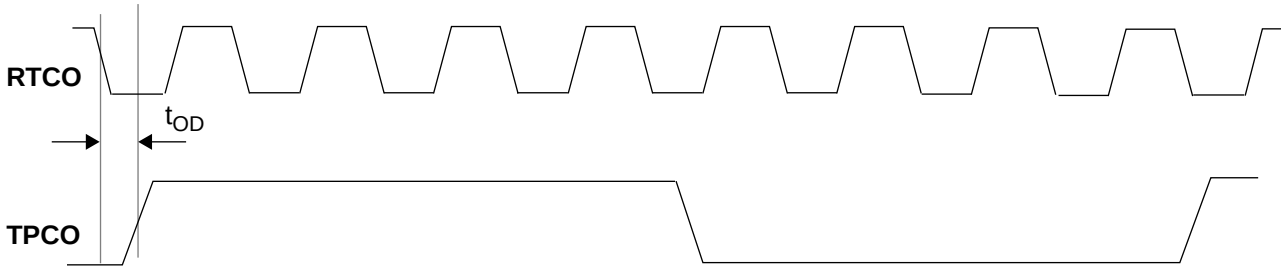
Parameter	Symbol	Min	Typ	Max	Unit
RTCO clock period	t_{CYC}	19.25	19.29		ns
RTCO high time	t_{PWH}	8.68	9.65	10.61	ns
RTCO low time	t_{PWL}	8.68	9.65	10.61	ns
RTDO,RSPE, RSYN output delay after RTCO↓	t_{OD}	-1		5	ns
RSPE gap between pulses	t_{GAP}	22 t_{CYC}	30 t_{CYC}	45 t_{CYC}	
RSYN pulse width	t_{PW}	8 t_{CYC}		9 t_{CYC}	

Figure 16. Terminal Serial SPE-Only Input Timing



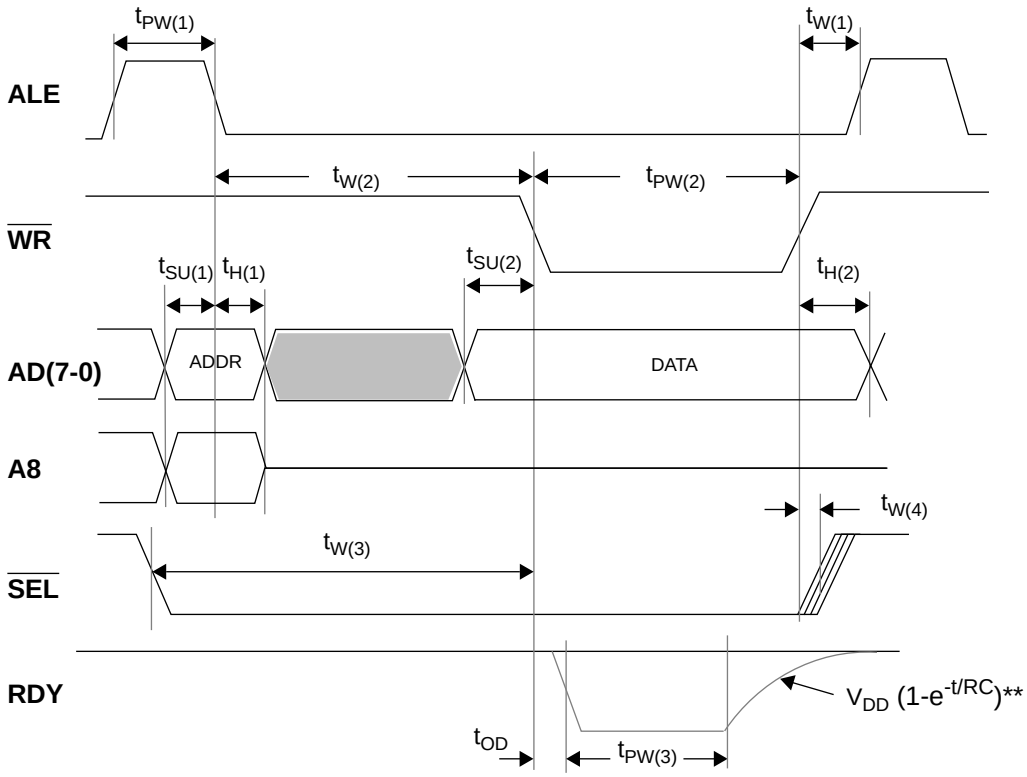
Parameter	Symbol	Min	Typ	Max	Unit
TTCI clock period	t_{CYC}	19.25	19.29		ns
TTCI high time	t_{PWH}	8.68	9.65	10.61	ns
TTCI low time	t_{PWL}	8.68	9.65	10.61	ns
TTDI, TSPE, TSYN set-up time to TTCI↑	t_{SU}	4			ns
TTDI, TSPE, TSYN hold time after TTCI↑	t_H	2			ns
TSPE gap between pulses	t_{GAP}	22 t_{CYC}	30 t_{CYC}	45 t_{CYC}	
TSYN pulse width	t_{PW}		8 t_{CYC}	9 t_{CYC}	

Figure 17. Receive Terminal Clock Output Timing



Parameter	Symbol	Min	Typ	Max	Unit
TPCO output delay after RTCO↓	t_{OD}	-1		5	ns

Figure 18. Microprocessor Write Cycle Timing

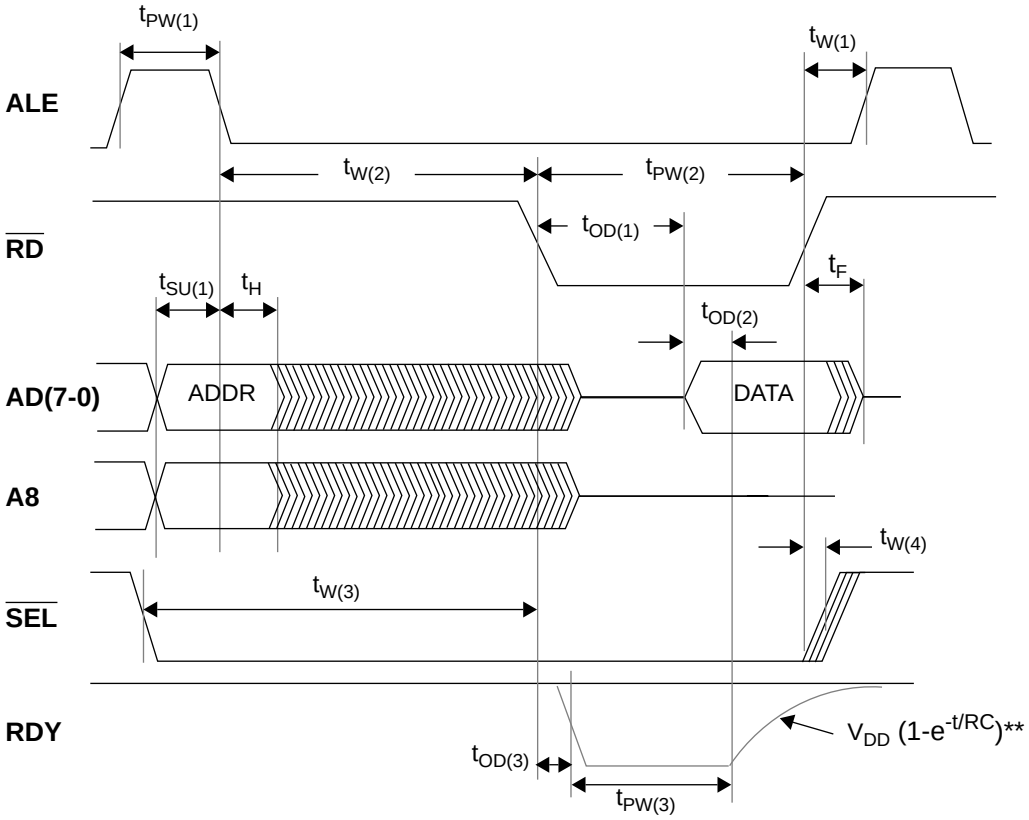


Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	20			ns
ALE wait after $\overline{WR}\uparrow$	$t_{W(1)}$	0			ns
$\overline{WR}$ wait time after ALE$\downarrow$	$t_{W(2)}$	20			ns
$\overline{WR}$ pulse width	$t_{PW(2)}$	20			ns
AD set-up time to ALE$\downarrow$	$t_{SU(1)}$	7			ns
AD hold time after ALE$\downarrow$	$t_{H(1)}$	3			ns
AD hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	3			ns
RDY output delay after $\overline{WR}\downarrow$	t_{OD}	2		7	ns
RDY pulse width*	$t_{PW(3)}$	0		2500	ns
Data set-up to $\overline{WR}\downarrow$	$t_{SU(2)}$	0			ns
$\overline{WR}\downarrow$ wait time after $\overline{SEL}\downarrow$	$t_{W(3)}$	0			ns
$\overline{SEL}\uparrow$ wait time after $\overline{WR}\uparrow$	$t_{W(4)}$	0			ns

*RDY goes low when the address being written to corresponds to a RAM location but remains high during status or control register access.

**Open drain rise time is dependent upon external pull-up resistor and load capacitance.

Figure 19. Microprocessor Read Cycle Timing

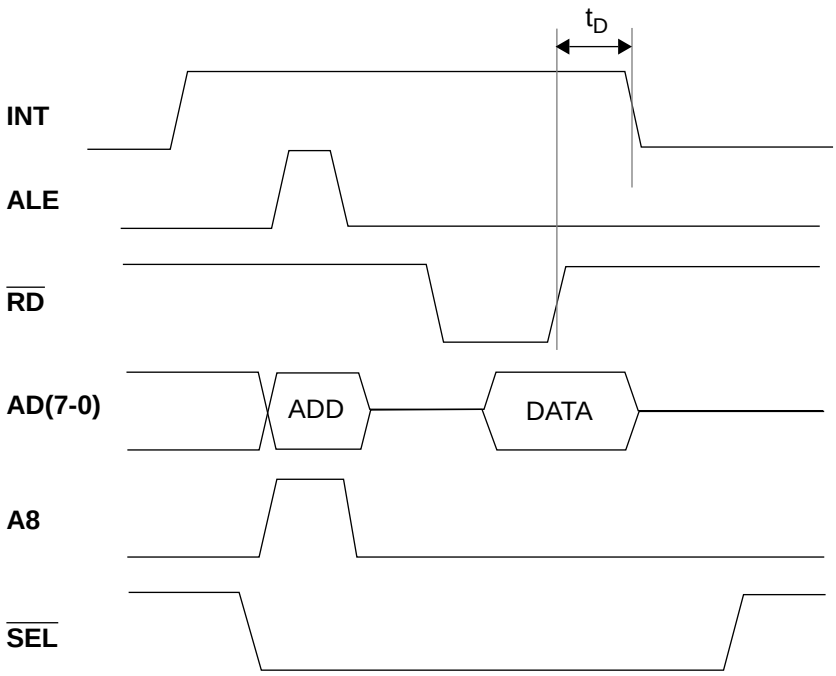


Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	20			ns
ALE wait after $\overline{RD}\uparrow$	$t_{W(1)}$	0			ns
$\overline{RD}$ wait time after ALE$\downarrow$	$t_{W(2)}$	7			ns
$\overline{RD}$ pulse width	$t_{PW(2)}$	40			ns
AD set-up time to ALE$\downarrow$	$t_{SU(1)}$	7			ns
AD hold time after ALE$\downarrow$	t_H	3			ns
AD output delay after $\overline{RD}\downarrow$	$t_{OD(1)}$	5		2500	ns
RDY$\uparrow$ output delay after AD	$t_{OD(2)}$	0	20		ns
AD float after $\overline{RD}\uparrow$	t_F	2		7	ns
RDY output delay after $\overline{RD}\downarrow$	$t_{OD(3)}$	2		7	ns
RDY pulse width*	$t_{PW(3)}$	0		2500	ns
$\overline{RD}\downarrow$ wait time after $\overline{SEL}\downarrow$	$t_{W(3)}$	0			ns
$\overline{SEL}\uparrow$ wait time after $\overline{RD}\uparrow$	$t_{W(4)}$	0			ns

*RDY goes low when the address being read corresponds to a RAM location but remains high during status or control register access.

**Open drain rise time is dependent upon external pull-up resistor and load capacitance.

Figure 20. Microprocessor Interrupt Timing

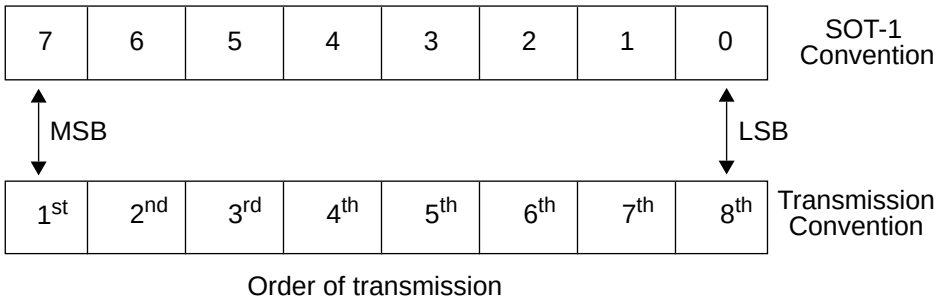


Parameter	Symbol	Min	Typ	Max	Unit
INT delay after $\overline{RD}\uparrow$	t_D	2		7	ns

OPERATION

Conventions

All address locations are given in Hex (H). The relationship between a transmission byte (e.g., C1) and the corresponding SOT-1 location is the following:



Register Bit Map

Address (Hex)	Mode[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comments[2]
0F0	R/W	RLOC	RNPTR	RPAIS	RLAIS	RLOP	RLOF	ROOF	RLOS	SR0
0F1	R/W	Same as 0F0 except does not reset on read; write ones to reset individual bits								SR0
0F2	R/W	INT	RTNEW	RPNEW	RPYE	RFERF	RAPS	--	--	SR1
0F3	R/W	Same as 0F2 except does not reset on read; write ones to reset individual bits								SR1
0F4	R	Same as 0F0 except unlatched values								SR0
0F5	R	Same as 0F2 except unlatched values								SR1
0F8	R/W	RRSD	RRLD	RRE1	RRE2	RPATH	RRAPS	RRPTR	TRLOOP	CR0
0F9	R/W	RRF1	RRC1	RRZ1	RRZ2	RRAIS	LTE	RRFRM	RRB1	CR1
0FA	R/W	STS1	PARA	HINT	TRFERF	ALTOW	TIEN	PIEN	-VE	CR2
1F0	R/W	TLOC	TNPTR	TPAIS	TLAIS	TLOP	TLOF	TOOF	TLOS	SR2
1F1	R/W	Same as 1F0 except does not reset on read; write ones to reset individual bits								SR2
1F4	R	Same as 1F0 except unlatched values								SR2
1F8	R/W	TRSD	TRLD	TRE1	TRE2	TPATH	TRAPS	EXAPS	RTLOOP	CR3
1F9	R/W	TRF1	TRC1	TRZ1	TRZ2	TRAIS	PTE	$\overline{\text{RXRTM}}$	RRB2	CR4
1FA	R/W	SPE	TCLK	RCLK	Reserved	TXRTM	Reserved	INC	DEC	CR5
1FB	R/W	TRFRM	TRERR	TAIS	Unused	RE2A	RA2E	TE2A	TA2E	CR6

Notes:
1. Read/write (R/W); Read only (R).
2. SR = Status Register; CR = Control Register

REGISTER BIT MAP DESCRIPTIONS

Control Register 0

Address (Hex)	Bit	Name	Description		Comments
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)	
0F8	7	RRSD	**Receiver Terminal-Side Section Datacom Bytes Control:** Outgoing terminal data has section datacom bytes from the RAM. (D1-D3)	Outgoing terminal data has section datacom bytes from the receive line.	See Note 1.
0F8	6	RRLD	**Receiver Terminal-Side Line Datacom Bytes Control:** Outgoing terminal data has line datacom bytes from the RAM. (D4-D12)	Outgoing terminal data has line datacom bytes from the receive line.	See Note 1.
0F8	5	RRE1	**Receiver Terminal-Side E1 Byte Control:** Outgoing terminal data has section orderwire byte from the RAM. RA2E must be low.	Outgoing terminal data has section orderwire byte from the receive line.	See Note 1.
0F8	4	RRE2	**Receiver Terminal-Side E2 Byte Control:** Outgoing terminal data has line orderwire byte from the RAM.	Outgoing terminal data has line orderwire byte from the receive line.	See Note 1.
0F8	3	RPATH	**Receiver Terminal-Side Path Overhead Control:** Outgoing terminal data has path overhead (except H4) bytes from the RAM.	Outgoing terminal data has path overhead bytes from the receive line.	Multi-frame indicator byte (H4) always passes through.
0F8	2	RRAPS	**Receiver Terminal-Side APS Bytes Control:** Outgoing terminal data has APS bytes (K1 and K2) from the RAM.	Outgoing terminal data has APS bytes (K1 and K2) from the receive line.	See Note 1.
0F8	1	RRPTR	**Receiver Terminal-Side Pointer Control:** Outgoing terminal data has pointer bytes (H1 and H2) from the RAM.	Outgoing terminal data has pointer bytes from the receive line or recalculated.	See Notes 1 and 2. Only pointer value is introduced.
0F8	0	TRLOOP	**Transmit-Receive Loopback Enable:** Line output looped back to receive line input.	Normal operation.	$\overline{\text{RFRI}}$ is disabled during loopback.

Notes:

1. The TOH bytes are inserted into the terminal data only in the pass-through mode.
2. This mode does not modify the payload; it simply inserts H1 and H2 bytes from insert RAM locations. It can be used for self test.

Control Register 1

Address (Hex)	Bit	Name	Description		Comments
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)	
0F9	7	RRF1	**Receiver Terminal-Side F1 Byte Control:** Outgoing terminal data has section user byte (F1) from the RAM.	Outgoing terminal data has section user byte from the receive line.	See Note 1.
0F9	6	RRC1	**Receiver Terminal-Side C1 Byte Control:** Outgoing terminal data has STS-1 ID byte (C1) from the RAM.	Outgoing terminal data has STS-1 ID byte (C1) from the receive line.	See Note 1.
0F9	5	RRZ1	**Receiver Terminal-Side Z1 Byte Control:** Outgoing terminal data has growth byte Z1 from the RAM.	Outgoing terminal data has growth byte Z1 from the receive line.	See Note 1.
0F9	4	RRZ2	**Receiver Terminal-Side Z2 Byte Control:** Outgoing terminal data has growth byte Z2 from the RAM.	Outgoing terminal data has growth byte Z2 from the receive line.	See Note 1.
0F9	3	RRAIS	**Receiver Terminal-Side AIS Output Control:** Enables automatic insertion of AIS into outgoing terminal data, as shown in the Receive Alarm Propagation Table section below for action codes 'L' and 'P'.	Disables automatic insertion of AIS into outgoing terminal data.	See Note 2.
0F9	2	LTE	**Line Terminating Equipment Enable:** Line terminating equipment for AIS transmission and introduction.	Not line terminating equipment for AIS transmission and introduction.	Section terminating equipment if LTE=0 and PTE = 0. LTE and PTE control alarm propagation as shown in the Alarm Propagation Tables section below.
0F9	1	RRFRM	**Receive Terminal-Side Framing Byte Control:** Outgoing terminal data has framing bytes regenerated.	Outgoing terminal data has framing bytes from the receive line.	See Note 1.
0F9	0	RRB1	**Receive Terminal-Side B1 Parity Byte Control:** Outgoing terminal data has B1 byte recalculated.	Outgoing terminal data has B1 byte from the receive line.	See Notes 1 and 3.

Notes:

1. The TOH bytes are inserted into the terminal data only in the pass-through mode.
2. The SPE bytes are set to all ones when an AIS is sent. All TOH bytes except A1, A2, E1, H1, and H2 are set to zero.
3. When operating the SOT-1 in STS-1 mode RRB1 should be set high or else B1 errors will be transmitted on the receive terminal side.

Control Register 2

Address (Hex)	Bit	Name	Description		Comments
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)	
0FA	7	STS1	**STS-1/STS-N Mode Control:** Line side in STS-1 mode. Received data is descrambled and transmit data is scrambled. Received B1 contains BIP-8 parity. Transmit B1 is recalculated.	Line Side in STS-N mode. Data is NOT scrambled. Received B1 byte contains BIP-8 errors. Transmit B1 byte contains error mask.	Controls both receive and transmit line side.
0FA	6	PARA	**Parallel/Serial Mode Control:** Terminal side interface is parallel. In receive direction, both serial and parallel interfaces are active.	Terminal side interface is serial. In receive direction, both serial and parallel interfaces are active except in SPE-only mode.	
0FA	5	HINT	**Hardware Interrupt Enable:** Enables hardware interrupt.	Disables hardware interrupt.	
0FA	4	TRFERF	**Transmit Line-Side FERF Enable:** Enables automatic introduction of line FERF into line side output under the conditions indicated in the Receive Alarm Propagation Table section below as resulting in action code 'F'.	Disables automatic introduction to line FERF into line side output.	
0FA	3	ALTOW	**Orderwire Mode Control:** Selects alternate orderwire interface -frame coincident with data MSB.	Selects normal orderwire interface - frame ahead of data MSB by one bit.	See Figures 5 and 6.
0FA	2	TIEN	**Transport Layer Interrupt Enable:** Enables interrupts for alarms detected in the transport overhead bytes.	Disables interrupts for alarms detected in the transport overhead bytes.	See Note 1.
0FA	1	PIEN	**Path Layer Interrupt Enable:** Enables interrupts for alarms detected in the path overhead bytes.	Disables interrupts for alarms detected in the path overhead bytes.	See Note 2.
0FA	0	-VE	**Interrupt Edge Control:** Interrupts on both positive and negative edges of alarms.	Interrupts only on positive going edge of alarms.	See Note 3.

Notes:

1. The conditions for transport layer interrupt are transport layer alarms (RLOS, ROOF, RLOF, RLAIS, RFERF, RAPS, RPAIS, RLOP, TLOS, TOOF, TLOF, TLAIS, TPAIS, and TLOP), overflow of transport layer performance monitors (receive B1 counter, receive B2 counter, receive INC counter, receive DEC counter, transmit INC counter, transmit DEC counter, transmit B1 counter, and transmit B2 counter) and new debounced values of C1, F1, K1, K2, Z1, and Z2 receive overhead bytes.
2. The conditions for path layer interrupt are path yellow alarm, overflow of path layer performance monitors (receive B3 counter, receive FEBE counter, and transmit B3 counter), and new debounced values of C2, F2, Z3, Z4, and Z5 receive path overhead bytes.
3. Performance counter overflows, alarms RPNEW and RTNEW if enabled by PIEN or TIEN respectively, only cause interrupts on the positive edge of the alarm regardless of the setting of -VE.

Control Register 3

Address (Hex)	Bit	Name	Description		Comments
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)	
1F8	7	TRSD	**Transmit Line-Side Section Datacom Bytes Control:** Outgoing line data has section datacom bytes from the section datacom interface. (D1-D3)	Outgoing line data has section datacom bytes from the terminal.	See Notes 1, 2, and 4.
1F8	6	TRLD	**Transmit Line-Side Line Datacom Bytes Control:** Outgoing line data has line datacom bytes from the line datacom interface. (D4-D12).	Outgoing line data has line datacom bytes from the terminal.	See Notes 1, 2, and 4.
1F8	5	TRE1	**Transmit Line Side E1 Byte Control:** Outgoing line data has section orderwire byte from the orderwire interface.	Outgoing line data has section orderwire byte from the terminal.	See Notes 1, 2, and 4.
1F8	4	TRE2	**Transmit Line-Side E2 Byte Control:** Outgoing line data has line orderwire byte from the orderwire interface.	Outgoing line data has line orderwire byte from the terminal.	See Notes 1, 2, and 4.
1F8	3	TPATH	**Transmit Line-Side Path Overhead Control:** Outgoing line data has path overhead (except H4) bytes from the RAM.	Outgoing line data has path overhead bytes from the terminal.	Multi-frame indicator byte (H4) always passes through.
1F8	2	TRAPS	**Transmit Line-Side APS Control:** Outgoing line data has APS bytes from the RAM.	Outgoing line data has APS bytes from the terminal.	See Notes 2, 3, and 4.
1F8	1	EXAPS	**External APS-to-RAM Enable:** APS bytes from the orderwire interface loaded to the RAM every frame.	RAM location for APS bytes not modified.	See Notes 2, 3, and 4.
1F8	0	RTLOOP	**Receive-to-Transmit Loopback Enable:** Receive terminal output looped back to transmit terminal input.	Normal operation.	

Notes:

1. Orderwire or datacom channels can come either from the terminal or the respective serial interface.
2. These channels cannot come from the terminal in the SPE-only mode.
3. Transmit line APS bytes have three sources: terminal, orderwire interface or RAM (using microprocessor interface).
4. These features are not available in the SPE-only mode.

Control Register 4

Address (Hex)	Bit	Name	Description		Comments
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)	
1F9	7	TRF1	**Transmit Line-Side F1 Byte Control:** Outgoing line data has section user byte (F1) from the RAM.	Outgoing line data has section user byte from the terminal.	See Note 1.
1F9	6	TRC1	**Transmit Line-Side C1 Byte Control:** Outgoing line data has STS-1 ID byte (C1) from the RAM.	Outgoing line data has STS-1 ID byte (C1) from the terminal.	See Note 1.
1F9	5	TRZ1	**Transmit Line-Side Z1 Byte Control:** Outgoing line data has growth byte Z1 from the RAM.	Outgoing line data has growth byte Z1 from the terminal.	See Note 1.
1F9	4	TRZ2	**Transmit Line-Side Z2 Byte Control:** Outgoing line data has growth byte Z2 from the RAM.	Outgoing line data has growth byte Z2 from the terminal.	See Note 1.
1F9	3	TRAIS	**Transmit Line-Side AIS Enable:** Enables automatic insertion of AIS into outgoing line data, as shown in the Transmit Alarm Propagation Table section below for action codes 'L' and 'P'.	Disables automatic insertion of AIS into outgoing line data.	
1F9	2	PTE	**Path Terminating Equipment Enable:** Path terminating equipment for AIS transmission and introduction.	Not path terminating equipment for AIS transmission and introduction.	Section terminating equipment if LTE=0 and PTE = 0. PTE and LTE control alarm propagation as shown in the Alarm Propagation Tables section below.
1F9	1	$\overline{\text{RXRTM}}$	**Receive Retiming Control:** Disables receive retiming and SPE-only mode.	Enables receive retiming for the SPE-only mode.	See “Interfaces and Operating Modes” section of this data sheet.
1F9	0	RRB2	**Receive Terminal-Side B2 Byte Control:** Outgoing terminal data has B2 byte recalculated.	Outgoing terminal data has B2 byte from the receive line.	See Note 2.

Notes:

1. These bytes cannot come from the terminal in the SPE-only mode.
2. These features are not available in SPE-only mode.

Control Register 5

Address (Hex)	Bit	Name	Description		Comments
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)	
1FA	7	SPE	**SPE-Only/STS-1 Mode Control:** SPE-only mode in the terminal side. $\overline{\text{RXRTM}}$ bit must be low.	STS-1 mode in the terminal side. $\overline{\text{RXRTM}}$ bit must be high.	
1FA	6	TCLK	**Transmitter Clock Source Select:** TLCO derived from TLCI.	TLCO derived from terminal clock, TTCI, in serial mode, or TPCI in parallel mode.	
1FA	5	RCLK	**Receiver Clock Source Select:** RTCO and TPCO derived from TLCI. $\overline{\text{RXRTM}}$ bit must be low.	RTCO and TPCO derived from RLCI.	See Note 2.
1FA	4	RESERVED	Not defined.	Normal operation.	This bit must be set low.
1FA	3	TXRTM	**Transmit Retiming Mode Control:** Enables automatic pointer justifications by transmit retiming circuitry.	Disables automatic pointer justifications by transmit retiming circuitry.	See Note 1.
1FA	2	RESERVED	Not defined.	Normal operation.	This bit must be set low.
1FA	1	INC	**Increment Pointer Control:** Forces pointer increments in line side.	Normal operation.	These bits must be reset two frames after being set to prevent multiple pointer justifications. See Note 1.
1FA	0	DEC	**Decrement Pointer Control:** Forces pointer decrements in line side.	Normal operation.	

Notes:

1. These bits should be used with caution - error in transmission may result.
2. RCLK may only be set to 1 when in SPE-only mode.

Control Register 6

Address (Hex)	Bit	Name	Description		Comments
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)	
1FB	7	TRFRM	**Transmit Line-Side Framing Control:** Enables automatic generation of the transmit framing bytes (A1 and A2).	Disables automatic generation of the transmit framing bytes (A1 and A2).	See Note 1.
1FB	6	TRERR	**Transmit Line-Side Parity Error Mask Control:** Enables automatic reset of transmit line B1, B2 and B3 error masks after one transmission.	Disables automatic reset of transmit line B1, B2 and B3 error masks after one transmission.	See Note 1.
1FB	5	TAIS	**Transmit Line-Side AIS Control:** Introduces AIS into transmit line, as indicated in the 'TAIS (control)' column of the Transmit Alarm Propagation Table section below.	Normal operation.	LTE and PTE bits determine line AIS or path AIS.
1FB	4	UNUSED			
1FB	3	RE2A	**Receiver E1-to-AIS Mode Control:** Enables received line E1 byte to be interpreted as AIS transmission byte, as indicated in the 'RE2A=1 and E1=FFh' column of the Receive Alarm Propagation Table section below.	Disables received line E1 byte to be interpreted as AIS transmission byte.	
1FB	2	RA2E	**Receiver AIS-to-E1 Mode Control:** Enables AIS transmission using receive terminal E1 byte under the conditions indicated in the Receive Alarm Propagation Table section below as resulting in action code 'E'.	Disables AIS transmission using receive terminal E1 byte.	

Notes:

1. These bits should be used with caution - error in transmission may result. It should be noted that even if TRFRM=1 writing to RAM locations 136 and 137 may cause the value written to these locations to be transmitted for one frame. If TRFRM=0 RAM location 136 must be written with F6 hex and RAM location 137 must be written with 28 hex or framing errors will be sent out the transmit line interface.

Address (Hex)	Bit	Name	Description		Comments
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)	
1FB	1	TE2A	**Transmitter E1-to-AIS Mode Control:** Enables transmit terminal E1 byte to be interpreted as AIS transmission byte, as indicated in the 'TE2A=1 and E1=FFh' column of the Transmit Alarm Propagation Table section below.	Disables transmit terminal E1 byte to be interpreted as AIS transmission byte.	
1FB	0	TA2E	**Transmitter AIS-to-E1 Mode Control:** Enables AIS transmission using transmit line E1 byte under the conditions indicated in the Transmit Alarm Propagation Table section below as resulting in action code 'E'.	Disables AIS transmission using transmit line E1 byte.	

Status Register 0

Address (Hex)	Bit	Symbol	Name	Conditions	
				Enter	Exit
0F0, 0F1, 0F4	7	RLOC	Receive Loss of Clock.	Typically 100 ns of no transitions in receive line clock RLCI.	Any transition of the receive line clock RLCI.
0F0, 0F1	6	RNPTR	Receive New Pointer.	A new pointer value due to new data flag or three consecutive frames of different pointer values.	Microprocessor read from address 0F0 or writing 1 to bit 6 of address 0F2.
0F0, 0F1, 0F4	5	RPAIS	Receive Path AIS.	Three consecutive frames of all ones in H1, H2 bytes.	NDF with valid pointer or three successive frames with valid pointer.
0F0, 0F1, 0F4	4	RLAIS	Receive Line AIS	Five consecutive frames of 111 in the bits 2,1,0 (6,7,8 transmission standard) of the K2 byte.	Five consecutive frames of patterns other than 111 in the bits 2,1,0 (6,7,8 transmission standard) of the K2 byte.
0F0, 0F1, 0F4	3	RLOP	Receive Loss of Pointer	Eight consecutive frames of invalid pointer or NDF.	Three consecutive frames of valid pointer.
0F0, 0F1, 0F4	2	RLOF	Receive Loss of Frame	Twenty four consecutive frames of out of frame condition.	Eight consecutive frames of in-frame condition.
0F0, 0F1, 0F4	1	ROOF	Receive Out of Frame	Failure to acquire valid framing pattern for four consecutive frames.	Valid framing pattern exactly 6480 bits apart.
0F0, 0F1, 0F4	0	RLOS	Receive Loss of Signal	STS-1 Mode: 20 µsec of all zeros in the scrambled data RLDI, or $\overline{\text{RXLOS}}$ pin low; see Note 4. STS-N mode: 6480 bits of all zeros or all ones, or $\overline{\text{RXLOS}}$ pin low.	STS-1 Mode: A valid framing pattern in the scrambled data and $\overline{\text{RXLOS}}$ pin high; see Note 4. STS-N Mode: Any transition in RLDI and $\overline{\text{RXLOS}}$ pin high.

Notes:

1. The address 0F0 contains latched values of these status bits, which reset on read.
2. The address 0F1 contains latched values of these status bits, but do not reset on read. Write one to individual bit to reset. Write back read value to reset the entire register.
3. The address 0F4 contains unlatched values of these status bits. The information is transient.
4. The SOT-1 RLOS detector is meant as an internal detector for the RLDI pin. SONET LOS detection must be done at the optical or electrical interface. For an STS-1 electrical interface a device such as the TranSwitch ARTE can provide this function and drive the $\overline{\text{RXLOS}}$ pin in the event of a loss of signal.

Status Register 1

Address (Hex)	Bit	Symbol	Name	Conditions	
				Enter	Exit
0F2, 0F3	7	INT	Interrupt.	Rising edge / both edges alarms, new debounced overhead bytes or performance monitor overflow.	Microprocessor read from address 0F2 or writing one to bit 7 of address 0F3.
0F2, 0F3	6	RTNEW	Receive New Debounced Transport Overhead Byte.	Any new debounced value for the following TOH bytes: C1, F1, K1, K2, Z1 and Z2.	Microprocessor read from address 0F2 or writing one to bit6 of address 0F3.
0F2, 0F3	5	RPNEW	Receive New Debounced Path Overhead Byte.	Any new debounced value for the following POH bytes: C2, F2, Z3, Z4 and Z5.	Microprocessor read from address 0F2 or writing one to bit5 of address 0F3.
0F2, 0F3, 0F5	4	RPYE	Receive Path Yellow.	Ten consecutive frames of 1 in bit 3 (bit 5 transmission standard) of the G1 byte.	Ten consecutive frames of zero in the bit 3 (bit 5 transmission standard) of the G1 byte.
0F2, 0F3, 0F5	3	RFERF	Receive FERF.	Five consecutive frames of 110 in the bits 2,1,0 (bits 6,7,8 transmission standard) of the K2 byte.	Five consecutive frames of 000 or 111 in the bits 2,1,0 (bits 6,7,8 transmission standard) of the K2 byte
0F2, 0F3, 0F5	2	RAPS	Receive APS Bytes Failure.	Twelve successive frames with no three consecutive frames containing identical APS bytes.	Three consecutive frames containing identical APS bytes.
0F2, 0F3, 0F5	1	UNUSED			
0F2, 0F3, 0F5	0	UNUSED			

Notes:

1. The address 0F2 contains latched values of these status bits, which reset on read.
2. The address 0F3 contains latched values of these status bits, but do not reset on read. Write one to individual bit to reset. Write back read value to reset the entire register.
3. The address 0F5 contains unlatched values of these status bits.

Status Register 2

Address (Hex)	Bit	Symbol	Name	Conditions	
				Enter	Exit
1F0, 1F1, 1F4	7	TLOC	Transmit Loss of Clock.	200 ns of no transitions in the clock TTCI. See Note 5.	Any transition of the clock TTCI. See Note 5.
1F0, 1F1,	6	TNPTR	Transmit New Pointer.	A new pointer value due to new data flag or three consecutive frames of different pointer values.	
1F0, 1F1, 1F4	5	TPAIS	Transmit Path AIS.	Three consecutive frames of all ones in H1, H2 bytes.	NDF with valid pointer or three successive frames with valid pointer.
1F0, 1F1, 1F4	4	TLAIS	Transmit Line AIS	Five consecutive frames of 111 in bits 6,7,8 of the K2 byte.	Five consecutive frames of patterns other than 111 in bits 6,7,8 of the K2 byte
1F0, 1F1, 1F4	3	TLOP	Transmit Loss of Pointer	Eight consecutive frames of invalid pointer or NDF.	Three consecutive frames of valid pointer.
1F0, 1F1, 1F4	2	TLOF	Transmit Loss of Frame	Eight consecutive frames of out of frame condition.	Eight consecutive frames of not out of frame condition.
1F0, 1F1, 1F4	1	TOOF	Transmit Out of Frame	Failure to acquire valid framing pattern for four consecutive frames.	Valid framing pattern exactly 6480 bits apart.
1F0, 1F1, 1F4	0	TLOS	Transmit Loss of Signal	6480 bits of all zeros or all ones.	Any transition in TTDI.

Notes:

1. The address 1F0 contains latched values of these status bits, which reset on read.
2. The address 1F1 contains latched values of these status bits, but do not reset on read. Write one to individual bit to reset. Write back read value to reset the entire register.
3. The address 1F4 contains unlatched values of these status bits.
4. None of these alarms except TLOS work in the SPE-only mode.
5. If PARA=1, TPCI generates TTCI internally. In this mode, loss of TPCI will generate TLOC in 10 to 11 µsec. Exit from TLOC will also take 10 to 11 µsec after TPCI is restored.

ALARM PROPAGATION TABLES

Receive Alarm Propagation Table

Rx Line Termination	LTE	PTE	Rx Terminal Output Alarm Actions						
			RE2A=1 and E1=FFh	RLOF	RLOS	RLOC	RLAIS	RPAIS	RLOP
Section Only	0	0	LEA-	LEAF	LEAF	LEAF	L*--F	P*---	----
Path Only	0	1	PEA-	PEAF	PEAF	PEAF	---F	PEA-	PEA-
Section, Line Only	1	0	PEA-	PEAF	PEAF	PEAF	PEAF	PEA-	PEA-
Section, Line, Path	1	1	PEA-	PEAF	PEAF	PEAF	PEAF	PEA-	PEA-

Key to Action Codes

L = Line AIS is generated at Rx terminal if RRAIS=1.
L*= Line AIS is not generated but is passed through if RRAPS=0.
P = Path AIS is generated at Rx terminal if RRAIS=1.
P*= Path AIS is not generated but is passed through if RPATH=0.
E = E1 byte at Rx terminal goes to FF if RA2E=1
(if RA2E=1 and no alarm indicated with an E is detected, the E1 byte goes to 00).
A = $\overline{\text{RAIS}}$ pin goes low.
F = Tx FERF is sent if TRFERF=1.

Transmit Alarm Propagation Table

Tx Line Origination	LTE	PTE	Tx Line Output Alarm Actions								
			TE2A=1 and E1=FFh	$\overline{\text{TAIS}}$ (pin) is low	TAIS (control)	TLOF	TLOS	TLOC	TLAIS	TPAIS	TLOP
Section Only	0	0	LE	LE	LE	LE	LE	LE	L*E	P*-	--
Path Only	0	1	PE	PE	PE	PE	PE	PE	--	PE	PE
Section, Line Only	1	0	PE	PE	PE	PE	PE	PE	--	PE	PE
Section, Line, Path	1	1	PE	PE	PE	PE	PE	PE	--	PE	PE

Key to Action Codes

L = Line AIS is generated at Tx line if TRAIS=1
(exception: TAIS (control) does not require TRAIS=1).
L*= Line AIS is not generated but is passed through if TRAPS=0.
P = Path AIS is generated at Tx line if TRAIS=1
(exception: TAIS (control) does not require TRAIS=1).
P*= Path AIS is not generated but is passed through if TPATH=0.
E = E1 byte at Tx line goes to FF if TA2E=1
(if TA2E=1 and no alarm indicated with an E is detected, the E1 byte goes to 00).

MEMORY MAP

Receive LIne Overhead Byte Locations (in Hex)

SECTION	**A1**	**A2**	**C1**		**J1**
	016	017	01C		080-0BF
	B1	**E1**	**F1**		**B3**
	014	018	01D		0C0
	D1	**D2**	**D3**		**C2**
	005	006	007		0C1
LINE	**H1**	**H2**	**H3**		**G1**
	011	012	013		0C2
	B2	**K1**	**K2**		**F2**
	015	01E	01F		0C3
	D4	**D5**	**D6**		**H4**
	008	009	00A		0C4
	D7	**D8**	**D9**		**Z3**
	00B	00C	00D		0C5
	D10	**D11**	**D12**		**Z4**
	00E	00F	010		0C6
	Z1	**Z2**	**E2**		**Z5**
	01A	01B	019		0C7
	TRANSPORT				PATH

Receive Insert Overhead Byte Locations (in Hex)

SECTION	**A1**[1]	**A2**[1]	**C1**		**J1**
	036	037	03C		080-0BF
	B1[1]	**E1**	**F1**		**B3**
	034	038	03D		0C8
	D1	**D2**	**D3**		**C2**
	025	026	027		0C9
LINE	**H1**	**H2**	**H3**		**G1**
	031	032	033		0CA
	B2[1]	**K1**	**K2**		**F2**
	035	03E	03F		0CB
	D4	**D5**	**D6**		**H4**
	028	029	02A		(Not Available)
	D7	**D8**	**D9**		**Z3**
	02B	02C	02D		0CD
	D10	**D11**	**D12**		**Z4**
	02E	02F	030		0CE
	Z1	**Z2**	**E2**		**Z5**
	03A	03B	039		0CF
	TRANSPORT				PATH

Notes:

1: These bytes are optionally regenerated by the SOT-1.

Receive Line and Terminal Overhead Byte RAM Locations Description

Symbol	Address (in Hex)		Control Bit [1]	Description
	Incoming	Insert [1]		
A1	016	036	RRFRM	**Framing Pattern:** The A1 and A2 bytes are automatically regenerated and are stored in insert locations.
A2	017	037		
C1	01C 05C	03C	RRC1	**STS-1 Signal Identifier:** The incoming C1 byte is debounced and stored in location 05C.
B1	014	034 049	RRB1	**Section BIP-8 Parity:** The received B1 byte carries B1 BIP-8 parity in the STS-1 mode and B1 BIP-8 parity error indications in the STS-N mode. The parity errors are added to the receive B1 counter. The B1 BIP-8 parity for the outgoing terminal data is recalculated and stored in the insert location.
E1	018	038	RRE1 RE2A[2] RA2E[2]	**Section Orderwire Byte:** The incoming E1 byte is also available in the orderwire/APS interface. The E1 byte can be reused for AIS communication between multiple SOT-1s.
F1	01D 05D	03D	RRF1	**Section User Byte:** The F1 byte is debounced and stored in location 05D.
D1 D2 D3	005 006 007	025 026 027	RRSD	**Section Data Communication Channel:** The incoming D1, D2 and D3 bytes are available as a single 192 Kbit/s serial HDLC channel on the section datacom interface.
H1 H2 H3	011 012 013	031 032 033	RRPTR	**Payload Pointer and Pointer Action Bytes:** The insert H1, H2 and H3 bytes are inserted into the outgoing terminal data without changing the J1 byte position. See Note 3.
B2	015	035 051	RRB2	**Line BIP-8 Bit Parity:** The received B2 byte carries the B2 BIP-8 parity. The parity errors are added to the B2 counter. The recalculated B2 byte is stored in the insert address.
K1 K2	01E, 05E 01F, 05F	03E 03F	RRAPS	**Automatic Protection Switching Bytes:** The K1 and K2 bytes are debounced and stored in locations 05E and 05F, respectively. The APS bytes are also available in the orderwire/APS interface.
D4 - D12	008 - 010	028 - 030	RRLD	**Line Data Communication Channel:** The incoming D4 through D12 bytes are available as a single 576 Kbit/s serial HDLC channel on the line datacom interface.
E2	019	039	RRE2	**Line Orderwire Byte:** The incoming E2 byte is also available in the orderwire/APS interface.
Z1 Z2	01A, 05A 01B, 05B	03A 03B	RRZ1 RRZ2	**Growth Bytes:** The Z1 and Z2 bytes are debounced and stored in locations 05A and 05B, respectively.

Notes:

1. The insert bytes are multiplexed into the terminal data when the corresponding control bit is set. Otherwise, the incoming bytes are multiplexed into the terminal data. If used, the microprocessor should initialize the insert locations. This feature is available in pass through mode only. In SPE-only mode, the terminal data has no TOH bytes.
2. The E1 byte could be used for AIS transmission. All ones in the E1 byte indicates an AIS condition; all zeros indicates a non-AIS condition. If the control bit RE2A is set, the SOT-1 will interpret the incoming E1 byte for AIS information. When the control bit RA2E is set, the terminal E1 byte carries AIS information.
3. The H3 byte is always taken from RAM location 133 except during a pointer decrement. A pointer decrement will not change the value at RAM location 133.

Receive Path Overhead Byte RAM Locations

Symbol	Address		Control Bit[1]	Description
	Incoming	Insert		
J1	080 - 0BF	080 - 0BF		**Path Trace:** The incoming message is stored in the RAM locations in a rotating fashion. There is no specified starting point, but any incoming J1 byte is written into the next sequential RAM location. The J1 byte always passes through the SOT-1 without modification.
B3	0C0	0C8 0D0	RPATH	**Path BIP-8 Parity:** The received B3 byte carries the B3 BIP-8 parity. The parity errors are added to the B3 counter. The recalculated B3 byte is stored in the insert address.
C2	0C1 0D1	0C9	RPATH	**Path Signal Label:** The C2 byte is debounced and stored in location 0D1.
G1	0C2	0CA	RPATH	**Path Status:** The upper nibble of the G1 byte contains the FEBE count (up to eight per frame) and is added to the receive FEBE counter.
F2	0C3 0D3	0CB	RPATH	**Path User Channel:** This byte provides user information between path terminating network elements. The F2 byte is debounced and stored in location 0D3.
H4	0C4			**Multiframe Indicator:** The H4 byte always passes through the SOT-1 without modification.
Z3 Z4 Z5	0C5, 0D5 0C6, 0D6 0C7, 0D7	0CD 0CE 0CF	RPATH	**Path Growth:** The Z3, Z4 and Z5 bytes are debounced and stored in locations 0D5, 0D6 and 0D7, respectively.

Notes:

1. The insert bytes are multiplexed into the terminal data when the corresponding control bit is set. Otherwise, the incoming bytes are multiplexed into the terminal data.

Receive Performance Monitor Locations

Symbol	Address	Bits	Disable Conditions	Description
B1	046	7 - 0	RLOS, RLOF	**STS-1 mode**: Counts B1 BIP-8 parity errors. **STS-N mode:** Counts ones in the B1 byte.
B2	047	7 - 0	RLOS, RLOF, RLAIS	Counts incoming B2 BIP-8 parity errors.
INC	045	7 - 4	RLOS, RLOF, RLAIS, RLOP, RPAIS	Counts incoming pointer increments.
DEC	045	3 - 0		Counts incoming pointer decrements.
B3	0D4	7 - 0		Counts incoming B3 BIP-8 parity errors.
FEBE	0D2	7 - 0		Counts incoming FEBE nibbles.

Note:

All performance monitors saturate at the maximum value and reset to zero on read.

Transmit Insert Overhead Byte Locations (in Hex)

SECTION	**A1[1]**	**A2[1]**	**C1**		**J1**
	136	137	13C		180-1BF
	B1[2]	**E1[3]**	**F1**		**B3**
	134	138	13D		1C8
	D1 Serial I/O	**D2 Serial I/O**	**D3 Serial I/O**		**C2**
	125	126	127		1C9
LINE	**H1**	**H2**	**H3**		**G1**
	(Not Available)	(Not Available)	133		1CA
	B2[2]	**K1[3,4]**	**K2[3,4]**		**F2**
	135	13E	13F		1CB
	D4[3]	**D5[3]**	**D6[3]**		**H4**
	128	129	12A		(Not Available)
	D7 Serial I/O	**D8 Serial I/O**	**D9[3]**		**Z3**
	12B	12C	12D		1CD
	D10[3]	**D11[3]**	**D12[3]**		**Z4**
	12E	12F	130		1CE
	Z1	**Z2**	**E2[3]**		**Z5**
	13A	13B	139		1CF
	← TRANSPORT →				← PATH →

Notes:

1: These bytes are optionally regenerated by the SOT-1.
2: These bytes are recalculated by the SOT-1. They are XORed with respective error mask before transmission.
3: These bytes are inserted from the orderwire, APS, and datacom interfaces.
4: The APS bytes can be inserted from the APS interface or the microprocessor.

Transmit Terminal Overhead Byte RAM Locations (in Hex)

SECTION	**A1**	**A2**	**C1**		**J1**
	116	117	11C		180-1BF
	B1	**E1**	**F1**		**B3**
	114	118	11D		1C0
	D1	**D2**	**D3**		**C2**
	105	106	107		1C1
LINE	**H1**	**H2**	**H3**		**G1**
	111	112	113		1C2
	B2	**K1**	**K2**		**F2**
	115	11E	11F		1C3
	D4	**D5**	**D6**		**H4**
	108	109	10A		1C4
	D7	**D8**	**D9**		**Z3**
	10B	10C	10D		1C5
	D10	**D11**	**D12**		**Z4**
	10E	10F	110		1C6
	Z1	**Z2**	**E2**		**Z5**
	11A	11B	119		1C7
	← TRANSPORT →				← PATH →

Transmit Terminal and Line Overhead Byte RAM Locations Description

Symbol	Address (in Hex)		Control Bit[1]	Description
	Incoming[2]	Insert[1]		
A1	116	136		**Framing Pattern:** The outgoing A1 and A2 bytes are stored in insert locations and automatically inserted into the outgoing line data. The A1 and A2 bytes are regenerated every frame, when the control bit TRFRM = 1.
A2	117	137		
C1	11C	13C	TRC1	**STS-1 Signal Identifier:** Normal operation.
B1	114	134 149	TRERR[4]	**Section BIP-8 Parity/Error Mask:** B1 errors are added to the transmit B1 counter. The outgoing B1 BIP-8 parity is recalculated and stored in insert location 134. In the STS-1 mode, the recalculated B1 is XORed with the B1 error mask from location 149 before transmission. In the STS-N mode, the B1 error mask from location 149 is transmitted.
E1	118	138	TRE1 TE2A[3] TA2E[3]	**Section Orderwire Byte:** The E2 byte from the orderwire interface is stored in the insert location. The E1 byte is optionally reused for AIS communication between SOT-1s.
F1	11D	13D	TRF1	**Section User Byte:** Normal operation.
D1 D2 D3	105 106 107	125 126 127	TRSD	**Section Data Communication Channel:** The section datacom bytes, D1 - D3, from the section datacom interface are stored in the insert location.
H1 H2 H3	111 112 113	 133		**Payload Pointer and Pointer Action Bytes:** The SOT-1 automatically recalculates the outgoing pointer. The H3 byte is inserted from RAM location 133.
B2	115	135 151	TRERR[4]	**Line BIP-8 Bit Parity:** The B2 errors are added to the transmit B2 counter. The outgoing B2 BIP-8 parity is recalculated and stored in the insert location 135. The recalculated B2 is XORed with the B2 error mask from location 151 before transmission.
K1 K2	11E 11F	13E 13F	TRAPS EXAPS	**Automatic Protection Switching Bytes:** If EXAPS is set, the APS bytes from the orderwire interface are stored in the insert RAM locations.
D4 - D12	108 - 110	128 - 130	TRLD	**Line Data Communication Channel:** The line datacom bytes, D4 - D12, from the section datacom interface are stored in the insert location.
E2	119	139	TRE2	**Line Orderwire Byte:** The E2 byte from the orderwire interface is stored in the insert location.
Z1 Z2	11A 11B	13A 13B	TRZ1 TRZ2	**Growth Bytes:** Normal operation.

Notes:

1. The insert bytes are multiplexed into the line data when the corresponding control bit is set. If used, the microprocessor should initialize the insert locations.
2. In SPE-only modes, the incoming terminal data has these bytes as an all zeros pattern.
3. The E1 byte could be used for AIS transmission. All ones in the E1 byte indicates an AIS condition; all zeros indicates a non-AIS condition. If the control bit TE2A is set, the SOT-1 will interpret the incoming E1 byte for AIS information. When the control bit TA2E is set, the line E1 byte carries AIS information.
4. If TRERR is set, the error masks are reset after transmission; otherwise, error is transmitted continuously.

Transmit Path Overhead Byte RAM Locations

Symbol	Address		Control Bit[1]	Description
	Incoming	Insert[1]		
J1	180 - 1BF	180 - 1BF	TPATH	**Path Trace:** The incoming/outgoing message is stored into/ extracted from the RAM locations in a rotating fashion. There is no specified starting point, but any incoming J1 byte is written to/read from the next sequential RAM location.
B3	1C0	1C8	TPATH TRERR[2]	**Path BIP-8 Parity:** The parity errors are added to the B3 counter. The recalculated B3 byte is stored in the insert address. The recalculated B3 is XORed with the B3 error mask from location 1D0 before transmission.
C2	1C1	1C9	TPATH	**Path Signal Label:** Normal operation.
G1	1C2	1CA	TPATH	**Path Status:** If TPATH is set, the SOT-1 sends a FEBE indication in the upper nibble of the outgoing G1 byte automatically. A path yellow indication can be sent by setting bit 3 to one. The path yellow indication should be sent 2-3 seconds after the following receive alarms are active: RLOS, RLOF, RLAIS, RLOP and RPAIS; and it should be removed 10-20 seconds after the receive alarms are cleared.
F2	1C3	1CB	TPATH	**Path User Channel:** Normal operation.
H4	1C4			**Multiframe Indicator:** The H4 byte always passes through the SOT-1 without modification.
Z3 Z4 Z5	1C5 1C6 1C7	1CD 1CE 1CF	TPATH	**Path Growth:** Normal operation.

Notes:

1. The insert bytes are multiplexed into the line data stream when the corresponding control bit is set. Otherwise, the incoming bytes are multiplexed into the line data stream.
2. If TRERR is set, the error mask is reset after transmission; otherwise, error is transmitted continuously.

Transmit Performance Monitor Locations

Symbol	Address	Bits	Disable Conditions	Description
B1	146	7 - 0	TLOS, TLOF	Counts B1 BIP-8 parity errors.
B2	147	7 - 0	TLOS, TLOF, TLAIS	Counts incoming B2 BIP-8 parity errors.
INC	145	7 - 4	TLOS, TLOF, TLAIS, TLOP, TPAIS	Counts incoming pointer increments.
DEC	145	3 - 0		Counts incoming pointer decrements.
B3	1D4	7 - 0		Counts incoming B3 BIP-8 parity errors.

Note:

All performance monitors saturate at the maximum value and reset to zero on read.

Receive Transport Overhead RAM Contents Summary

Address	__0	__1	__2	__3	__4	__5	__6	__7	__8	__9	__A	__B	__C	__D	__E	__F
00_	Spare	Spare	Spare	Spare	Spare	In D1	In D2	In D3	In D4	In D5	In D6	In D7	In D8	In D9	In D10	In D11
01_	In D12	In H1	In H2	In H3	In B1	In B2	In A1	In A2	In E1	In E2	In Z1	In Z2	In C1	In F1	In K1	In K2
02_	Spare	Spare	Spare	Spare	Spare	Out D1	Out D2	Out D3	Out D4	Out D5	Out D6	Out D7	Out D8	Out D9	Out D10	Out D11
03_	Out D12	Out H1	Out H2	Out H3	Out B1	Out B2	Out A1	Out A2	Out E1	Out E2	Out Z1	Out Z2	Out C1	Out F1	Out K1	Out K2
04_	Spare	Spare	Spare	Spare	Spare	PJC Counter	B1 Counter	B2 Counter	Spare	B1 Mask	F[-1] Z1	F[-1] Z2	F[-1] C1	F[-1] F1	F[-1] K1	F[-1] K2
05_	Spare	B2 Mask	F[-2] Z1	F[-2] Z2	F[-2] C1	F[-2] F1	F[-2] K1	F[-2] K2	Spare	Spare	Deb Z1	Deb Z2	Deb C1	Deb F1	Deb K1	Deb K2

Receive Path Overhead RAM Contents Summary

Address	__0	__1	__2	__3	__4	__5	__6	__7	__8	__9	__A	__B	__C	__D	__E	__F
08_	F[-8] In J1	F[-7] In J1	F[-6] In J1	F[-5] In J1	F[-4] In J1	F[-3] In J1	F[-2] In J1	F[-1] In J1	In J1	F[-63] In J1	F[-62] In J1	F[-61] In J1	F[-60] In J1	F[-59] In J1	F[-58] In J1	F[-57] In J1
09_	F[-56] In J1	F[-55] In J1	F[-54] In J1	F[-53] In J1	F[-52] In J1	F[-51] In J1	F[-50] In J1	F[-49] In J1	F[-48] In J1	F[-47] In J1	F[-46] In J1	F[-45] In J1	F[-44] In J1	F[-43] In J1	F[-42] In J1	F[-41] In J1
0A_	F[-40] In J1	F[-39] In J1	F[-38] In J1	F[-37] In J1	F[-36] In J1	F[-35] In J1	F[-34] In J1	F[-33] In J1	F[-32] In J1	F[-31] In J1	F[-30] In J1	F[-29] In J1	F[-28] In J1	F[-27] In J1	F[-26] In J1	F[-25] In J1
0B_	F[-24] In J1	F[-23] In J1	F[-22] In J1	F[-21] In J1	F[-20] In J1	F[-19] In J1	F[-18] In J1	F[-17] In J1	F[-16] In J1	F[-15] In J1	F[-14] In J1	F[-13] In J1	F[-12] In J1	F[-11] In J1	F[-10] In J1	F[-9] In J1
0C_	In B3	In C2	In G1	In F2	In H4	In Z3	In Z4	In Z5	Out B3	Out C2	Out G1	Out F2	Spare	Out Z3	Out Z4	Out Z5
0D_	B3 Mask	Deb C2	FEBE Counter	Deb F2	B3 Counter	Deb Z3	Deb Z4	Deb Z5	Spare	F[-1] C2	Spare	F[-1] F2	Spare	F[-1] Z3	F[-1] Z4	F[-1] Z5
0E_	Spare	F[-2] C2	Spare	F[-2] F2	Spare	F[-2] Z3	F[-2] Z4	F[-2] Z5								

Notes:

In: Incoming overhead byte
Out: Insert overhead byte
F[-n]: Overhead byte from previous nth Frame
Deb: Debounced overhead byte

Transmit Transport Overhead RAM Contents Summary

Address	__0	__1	__2	__3	__4	__5	__6	__7	__8	__9	__A	__B	__C	__D	__E	__F
10_	Spare	Spare	Spare	Spare	Spare	In D1	In D2	In D3	In D4	In D5	In D6	In D7	In D8	In D9	In D10	In D11
11_	In D12	In H1	In H2	In H3	In B1	In B2	In A1	In A2	In E1	In E2	In Z1	In Z2	In C1	In F1	In K1	In K2
12_	Spare	Spare	Spare	Spare	Spare	SDCC D1	SDCC D2	SDCC D3	LDCC D4	LDCC D5	LDCC D6	LDCC D7	LDCC D8	LDCC D9	LDCC D10	LDCC D11
13_	LDCC D12	Spare	Spare	Out H3	Out B1	Out B2	Out A1	Out A2	OrderW E1	OrderW E2	Out Z1	Out Z2	Out C1	Out F1	APS K1	APS K2
14_	Spare	Spare	Spare	Spare	Spare	PJC Counter	B1 Counter	B2 Counter	Spare	B1 Mask	Spare	Spare	Spare	Spare	Spare	Internal Use
15_	Internal Use	B2 Mask	Spare	Spare	Spare	Spare	Spare	Spare								

Transmit Path Overhead RAM Contents Summary

Address	__0	__1	__2	__3	__4	__5	__6	__7	__8	__9	__A	__B	__C	__D	__E	__F
18_	F[-8] Out J1	F[-7] Out J1	F[-6] Out J1	F[-5] Out J1	F[-4] Out J1	F[-3] Out J1	F[-2] Out J1	F[-1] Out J1	Out J1	F[-63] Out J1	F[-62] Out J1	F[-61] Out J1	F[-60] Out J1	F[-59] Out J1	F[-58] Out J1	F[-57] Out J1
19_	F[-56] Out J1	F[-55] Out J1	F[-54] Out J1	F[-53] Out J1	F[-52] Out J1	F[-51] Out J1	F[-50] Out J1	F[-49] Out J1	F[-48] Out J1	F[-47] Out J1	F[-46] Out J1	F[-45] Out J1	F[-44] Out J1	F[-43] Out J1	F[-42] Out J1	F[-41] Out J1
1A_	F[-40] Out J1	F[-39] Out J1	F[-38] Out J1	F[-37] Out J1	F[-36] Out J1	F[-35] Out J1	F[-34] Out J1	F[-33] Out J1	F[-32] Out J1	F[-31] Out J1	F[-30] Out J1	F[-29] Out J1	F[-28] Out J1	F[-27] Out J1	F[-26] Out J1	F[-25] Out J1
1B_	F[-24] Out J1	F[-23] Out J1	F[-22] Out J1	F[-21] Out J1	F[-20] Out J1	F[-19] Out J1	F[-18] Out J1	F[-17] Out J1	F[-16] Out J1	F[-15] Out J1	F[-14] Out J1	F[-13] Out J1	F[-12] Out J1	F[-11] Out J1	F[-10] Out J1	F[-9] Out J1
1C_	In B3	In C2	In G1	In F2	In H4	In Z3	In Z4	In Z5	Out B3	Out C2	Out G1	Out F2	Spare	Out Z3	Out Z4	Out Z5
1D_	B3 Mask	Spare	Spare	Spare	B3 Counter	Spare	Spare	Spare								

Notes:
In: Incoming overhead byte
F[-n]: Overhead byte from previous nth Frame
Out: Outgoing overhead byte
Deb: Debounced overhead byte

INTERFACES AND OPERATING MODES

The control bits used for various modes are summarized below in the following table:

Address	7	6	5	4	3	2	1	0
0FA	STS-1	PARA			ALTOW			
1F9							$\overline{\text{RXRTM}}$	
1FA	SPE	TCLK	RCLK					

Line Side Interface

In the receive direction, the line side interface consists of the incoming 51.84 MHz clock (RLCI), the incoming STS-1 data (RLDI), and the optional frame pulse ($\overline{\text{RFRI}}$). When used, $\overline{\text{RFRI}}$ allows exit from the OOF state within 125 microseconds. The transmit line interface consists of the reference 51.84 MHz clock (TLCI), the optional frame reference ($\overline{\text{TFRI}}$), the outgoing clock (TLCO), and the outgoing STS-1 data (TLDO). The line side interface supports either the STS-1 mode or the STS-N mode as summarized in the following table:

Mode	Selection	Description
STS-1	STS-1 = 1	Both incoming and outgoing line data is scrambled. The chip descrambles the received data (RLDI) and scrambles the transmit data (TLDO).
		The receive B1 byte contains B1 BIP-8 parity. The chip compares the incoming B1 byte to calculated B1 and adds the parity errors to the receive B1 counter.
		The transmit B1 byte is the outgoing B1 BIP-8 parity. The chip calculates the outgoing B1 parity, exclusive-ors the result with the outgoing B1 error mask from RAM location 149, and transmits the result on the line.
STS-N	STS-1 = 0	Both incoming and outgoing line data is NOT scrambled.
		The receive B1 byte contains B1 BIP-8 parity error indications. The chip adds the ones in the incoming B1 byte to the receive B1 counter.
		The transmit B1 byte contains the B1 error mask from RAM location 149.

The clock selection bit, TCLK, allows TLCO to be derived from the following sources:

TCLK	SPE	PARA	Source of TLCO
0	0	0	TTCI. $\overline{\text{TFRI}}$ cannot be used in this mode.
0	0	1	TPCI. $\overline{\text{TFRI}}$ cannot be used in this mode.
1	0	0	TLCI. $\overline{\text{TFRI}}$ can be used in this mode.
1	0	1	TLCI. $\overline{\text{TFRI}}$ can be used in this mode.
0, 1	1	0	TLCI. $\overline{\text{TFRI}}$ can be used in this mode, SPE only, Serial only.

Note: The SPE-only mode can be used only if the control bit $\overline{\text{RXRTM}}$ = 0.

Terminal Side Interface

The receive direction terminal side interface consists of the 51.84 MHz serial clock (RTCO), the serial data (RTDO), the payload indicator (RSPE), the C1J1 indicator (RSYN), the 6.48 MHz parallel clock (TPCO), and the parallel data (TPDO7-TPDO0). The transmit terminal interface consists of the 51.84 MHz serial clock (TTCI), the serial data (TTDI), the payload indicator (TSPE), the C1J1 or J1 indicator (TSYN), the 6.48 MHz parallel clock (TPCI), and the parallel data (TPDI7-TPDI0).

The terminal interface supports the following modes:

Mode	Selection	Description
Serial STS-1 Pass Through	$\overline{\text{PARA}}$ = 0 $\overline{\text{RXRTM}}$ = 1 SPE = 0 RCLK = 0	RTDO is serial non-retimed STS-1 data with all TOH bytes from the line input or RAM.
		TPDO7-TPDO0 is parallel STS-1 data with all TOH bytes from the line input or RAM.
		RSPE is nominally: low-width = 24, high-width = 696; increment: low-width = 32, high-width = 688; decrement: low-width = 16, high-width = 704. RSYN is high during the C1 and J1 bytes. Numbers are clock periods.
		TTCI and TTDI are used as terminal STS-1 inputs in the transmit direction.
		TPCI and TPDI 7-TPDI0 are ignored.
		TSPE and TSYN are ignored.
		All TOH bytes can be inserted to/extracted from the terminal.
		The E1 byte can be used for AIS communication.
		Transmit side alarms and performance monitors are enabled.
		RTCO and TPCO are derived from RLCI.
Parallel STS-1 Pass Through	$\overline{\text{PARA}}$ = 1 $\overline{\text{RXRTM}}$ = 1 SPE = 0 RCLK = 0	RTDO is serial non-retimed STS-1 data with all TOH bytes from the line input or RAM.
		TPDO7-TPDO0 is parallel STS-1 data with all TOH bytes from the line input or RAM.
		RSPE is nominally: low-width = 3, high-width = 87; increment: low-width = 4, high-width = 86; decrement: low-width = 2, high-width = 88. RSYN is high during the C1 and J1 bytes. Numbers are clock periods.
		TTCI and TTDI are ignored.
		TPCI and TPDI 7-TPDI0 are used as terminal STS-1 inputs in the transmit direction.
		TSPE and TSYN are ignored.
		All TOH bytes can be inserted to/extracted from the terminal.
		The E1 byte can be used for AIS communication.
		Transmit side alarms and performance monitors are enabled.
		RTCO and TPCO are derived from RLCI.
Serial SPE-Only	$\overline{\text{PARA}}$ = 0 $\overline{\text{RXRTM}}$ = 0 SPE = 1	RTDO is serial retimed SPE-only data.
		TPDO7-TPDO0 consists of all zeros data.
		RSPE is nominally: low-width = 1, high-width = 29; increment: low-width = 1, high-width = 44; decrement: low-width = 1, high-width = alternate 21, 22. RSYN is high during the J1 byte. Numbers are clock periods.
		TTCI, TTDI, TSPE and TSYN are used as the terminal SPE-only inputs.
		TPCI and TPDI 7-TPDI0 are ignored.
		TSPE and TSYN are used.
		No TOH byte can be inserted to/extracted from the terminal.
		There is no terminal E1 byte to be used for AIS communication.
		Transmit side alarms and performance monitors are disabled.
	RCLK = 0	RTCO is derived from RLCI.
	RCLK = 1	RTCO is derived from TLCI.

Microprocessor Interface

The microprocessor interface consists of multiplexed address/data bus (AD7-AD0), address bit (A8), address latch enable (ALE), chip select ($\overline{SEL}$), read enable ($\overline{RD}$), write enable ($\overline{WR}$), Ready (RDY) and interrupt ($\overline{INT}$) signals. In addition, the SOT-1 provides both software and hardware interrupt capability based on the status of the receive and transmit transport, and path overhead alarms.

Orderwire/APS Interface

In the receive direction, the section orderwire byte (E1), the line orderwire byte (E2) and the APS bytes (K1 and K2) are multiplexed to form a 576 Kbit/s bit-serial stream. This interface consists of the multiplexed 576 Kbit/s data signal (ORDO), a clock signal (ORCO), and three framing pulses: a section framing pulse (SRFR), a line framing pulse (LRFR) and an APS framing pulse ($\overline{RAP}$).

The transmit side orderwire/APS interface is similar. The section orderwire byte (E1), the line orderwire byte (E2) and the APS bytes (K1 and K2) are demultiplexed from a 576 Kbit/s bit-serial stream. This interface consists of the multiplexed 576 Kbit/s data signal (OTDI), a clock signal (OTCO), and three framing pulses: a section orderwire framing pulse (STFR), a line orderwire framing pulse (LTFR), and an APS framing pulse ($\overline{TAP}$).

The orderwire interface supports two modes:

Mode	Selection	Description
Normal Orderwire Interface	ALTOW = 0.	SRFR occurs one ORCO clock cycle before MSB of E1 byte in ORDO.
		LRFR occurs one ORCO clock cycle before MSB of E2 byte in ORDO.
		STFR occurs one ORCI clock cycle before MSB of E1 byte is expected in OTDI.
		LTFR occurs one ORCI clock cycle before MSB of E2 byte is expected in OTDI.
Alternate Orderwire Interface	ALTOW = 1.	SRFR occurs coincident with the MSB of E1 byte in ORDO.
		LRFR occurs coincident with the MSB of E2 byte in ORDO.
		STFR occurs coincident with the MSB of E1 byte is expected in OTDI.
		LTFR occurs coincident with the MSB of E2 byte is expected in OTDI.

Datacom Interfaces

In the receive direction, the section overhead data communication interface consists of a receive data out signal (SRDO) and a clock out signal (SRCO). The line overhead data communication interface consists of a receive data out signal (LRDO) and a clock out signal (LRCO).

In the transmit direction, the section overhead data communication channel interface consists of a data in signal (STDI) and a clock out signal (STCO). The line overhead data communication channel interface consists of a data in signal (LTDI) and a clock out signal (LTCO).

Power, Ground, and External Components

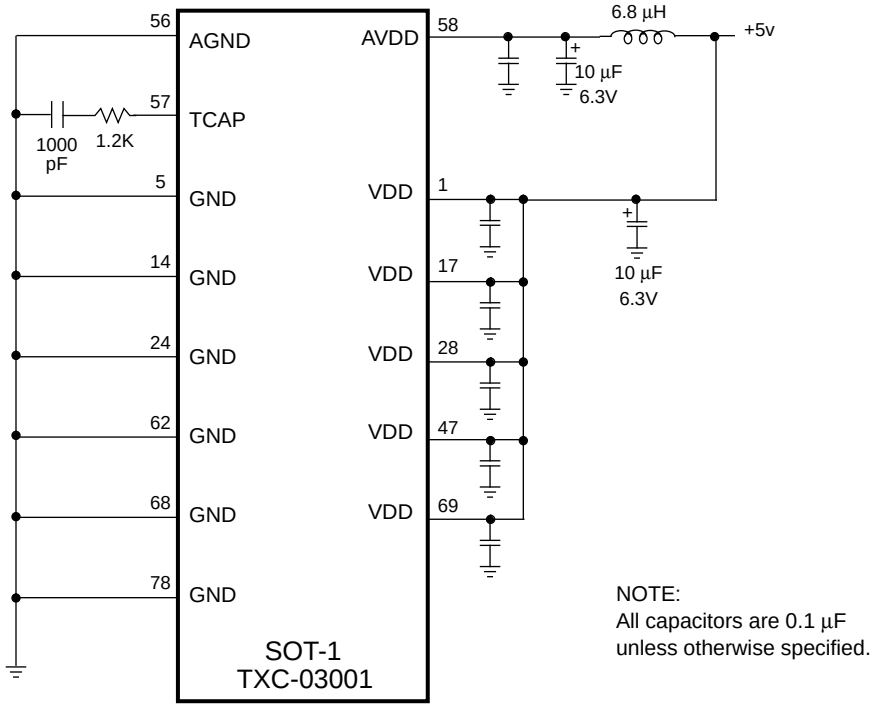


Figure 21. SOT-1 Power Supply Connections

Figure 21 shows the recommended power and ground connection method for the SOT-1 device. Separate planes should be employed for VDD and GND. Bypass networks consist of 10 µF capacitors in parallel with 0.1 µF capacitors as shown. These 0.1 µF capacitors should be RF-quality and closely connected to each of the device's voltage leads to decouple them to ground. A Fair-Rite Products #2743002111 or equivalent ferrite bead is recommended in the AVDD supply path as shown.

Throughput Delays

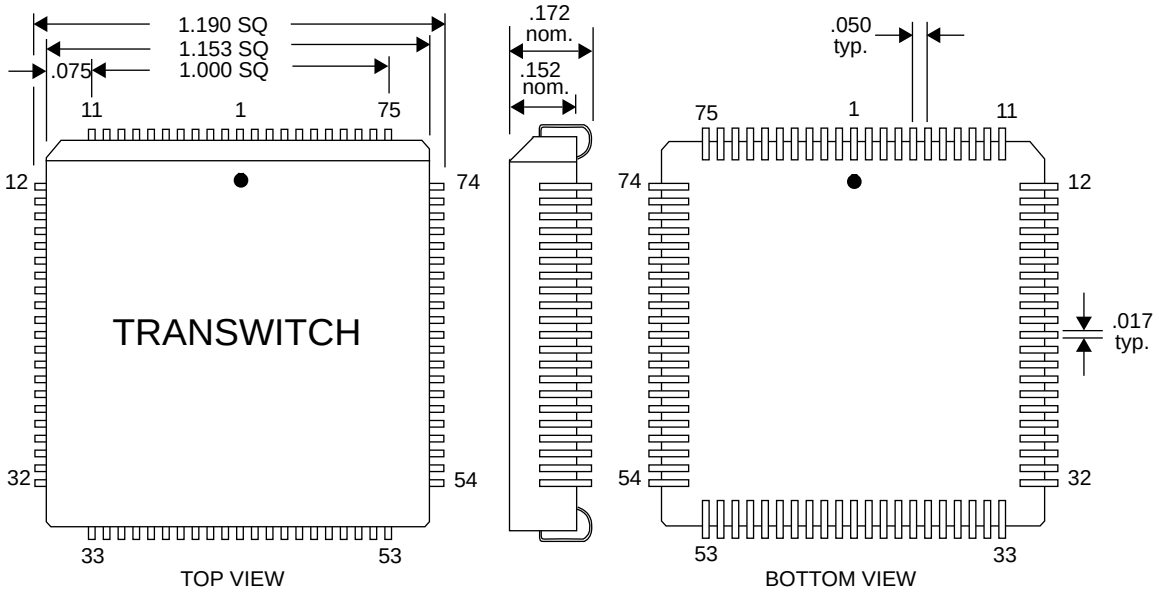
The SOT-1 throughput delays below are listed in terms of STS-1 bit times (1 bit = 19.29 nsec nominal):

1. The throughput delay from the terminal side input to the line side transmit output is from 65 to 113 bits.

2. The throughput delay from the line side receive input to the terminal side output is from 65 to 133 bits in the SPE-only mode or is a fixed 25 bits when not in the SPE-only mode (see bit 7 of register 1FAH).

PACKAGING

The SOT-1 is packaged in an 84-pin plastic chip carrier suitable for socket or surface mounting. All dimensions shown are in inches and are nominal unless otherwise noted. All dimensions and notes for the specified JEDEC outline apply.



(JEDEC Outline MO-047-AF)

Figure 22. SOT-1 84-Pin Plastic Leaded Chip Carrier

ORDERING INFORMATION

Part Number: TXC-03001-AIPL	84-pin plastic leaded chip carrier

RELATED PRODUCTS

The SOT-1 device interfaces with the following TranSwitch VLSI devices:

• TXC-02001, DS3RT	DS3/STS-1 Line Interface device
• TXC-02201, SM3	SONET STS-3/STS-1 Mux/Demux device
• TXC-03451, DS3M	SD3/STS-1 Mapper-Desync device
• TXC-04001, ADMA-T1	DS1 to VT-1.5 Async Mapper-Desync device
• TXC-05101, HDLC	HDLC Controller, 36-Bit Terminal I/O device

TXC-21009, ADMA-T1/SOT-1 Evaluation Board. A complete, ready-to-use single board test system that demonstrates the functions and features of the ADMA-T1 and SOT-1 VLSI devices. Includes on-board microprocessor, RS-232 interface, and MS-DOS compatible PC software. The PC software provides full access to the ADMA-T1 and SOT-1 devices for control and monitor.

TXC-21011, DS3M/SOT-1 Evaluation Board. A complete, ready-to-use single board test system that demonstrates the functions and features of the DS3M and SOT-1 VLSI devices. Includes on-board microprocessor, RS-232 interface, and MS-DOS compatible PC software. The PC software provides full access to the DS3M and SOT-1 devices for control and monitor.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

CCITT:

Publication Services of ITU
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated SOT-1 Data Sheet that have technical differences relative to the superseded SOT-1 Data Sheet:

Updated SOT-1 Data Sheet: Edition 10, September 1994

Superseded SOT-1 Data Sheet: Edition 9, June 1993

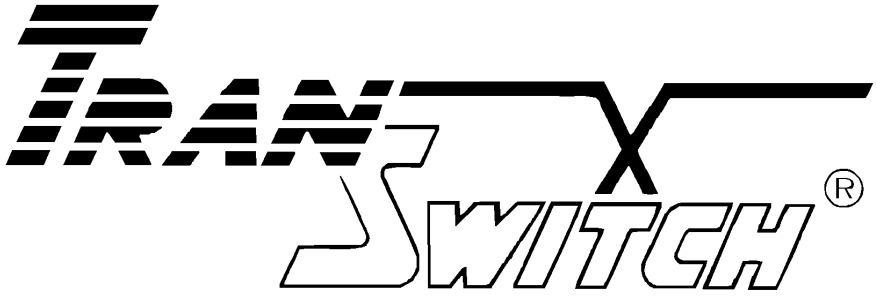
The page numbers indicated below of this updated data sheet include changes relative to the superseded data sheet.

Page Number of Updated Data Sheet	Summary of the Change
1	Changed edition number and date.
2	Modified Table of Contents.
2-61	Added edition number and date.
3-4	Made minor clarifications to Block Diagram Description section.
5	Made minor clarification to the Note.
6	Made minor clarification to Name/Function section of RST.
6	Added a note to the bottom to explain Type column heading.
8	Made minor corrections to Name/Function section of $\overline{RAP}$ and SRDO.
9	Made minor changes to Name/Function section of TTCI and TSYN.
10	Made minor changes to Name/Function section of TPCI.
10	Modified Name/Function sections of $\overline{RAIS}$ and $\overline{TAIS}$ to refer to new Alarm Propagation Tables added on Page 42.
11	Changed Max column on Symbol T_J from 150 to 125.
12	Changed Input Parameters For CMOSp section on Input leakage current.
16	Modified Figure 4: t_{CYC} values changed and Note 2 added.
17	Modified Figure 5, adding K2 byte to ORDO and clarifying diagram.
18	Modified Figure 6, changing byte content of OTDI.
21	Modified Figure 11, changing title and re-defining $t_{OD(1)}$, $t_{OD(2)}$, and $t_{OD(3)}$.
24	Modified Figure 15, clarifying diagram.
25	Modified Figure 16, removing reference to byte C1 in TTCI and adding max value for t_{PW}.

Page Number of Updated Data Sheet	Summary of the Change
26	Modified Figure 17, changing t_{OD} max value.
30	In Bit Map, connected TE2E at Address 1FB (Hex) to TE2A.
31	Modified Note 1.
32	Made amplifying change to Bit Equal to 1 (High) section of Bit 3 (RRAIS).
32	Modified Comments section on Bit 2 (LTE), 1 (RRFRM), and 0 (RRB1).
32	Modified Notes 1, 2 and added Note 3.
33	Made amplifying change to Description section on Bit 4 (TRFERF), and expanded Description section for Bits 2 (TIEN) and 1 (PIEN).
33	Deleted comments from Bit 4 (TRFERF) and added comments to Bit 0 (-VE).
33	Modified the Notes section, deleting former Note 1, changing current Note 1 and adding current Note 3.
35	Made amplifying changes to Bit Equal to 1 (High) section on Bit 3 (TRAIS), to Comments section on Bit 2 (PTE), and to Description section on Bit 1 ($\overline{\text{RXRTM}}$).
36	Made amplifying changes to Bit Equal to 0 (Low) section on Bit 7 (SPE), to Comments section on Bit 5 (RCLK), and added Note 2.
35	Modified to Note 2 to eliminate reference to receive-retiming mode.
37	Expanded Note 1.
37-38	Made changes to Bit Equal to 1 (High) section on Bit 5 (TAIS), 3 (RE2A), 2 (RA2E), 1 (TE2A), and 0 (TA2E) to refer to new Alarm Propagation Tables.
39	Made changes to Conditions section on Bit 7 (RLOC), 2 (RLOF), and 0 (RLOS).
39	Added Note 4.
41	Made minor changes to Conditions section on Bit 7 (TLOC).
41	Deleted 1F4 from Address (Hex) section on Bit 6 (TNPTR).
41	Added Note 5.
42	Added Alarm Propagation Tables. The content of this page is a new addition.
44	Added Note 3 reference to Description section of RRPTR.
44	Deleted reference to receive-retiming mode in Note 1.
44	Added Note 3.
45	Added 0D0 in Address (Insert) section on B3.
45	Deleted Address (Insert) section on H4.
48	Deleted Address (Insert) section on H4 and added Note 2 to Transmit Path Overhead Byte RAM Locations.

Page Number of Updated Data Sheet	Summary of the Change
49	Modified Receive Transport Overhead RAM Contents Summary section, adding Out H1, Out H2 and Out H3 at Address 031, 032 and 033 (Hex).
50	Modified Transmit Transport Overhead RAM Contents Summary section, adding Out H3 at Address 133 (Hex).
51	Modified Source of TLCO section on the last table.
52	Modified the table: RCLK=0,1 changed to RCLK=0 twice in Selection column. For Serial SPE-Only, Description column, changes made in RTDO and RSPE rows.
53	Modified Microprocessor Interface.
54	Modified Figure 21 capacitor symbols and number 2 on Throughput Delays section.
55	Modified Figure 22: some dimensions and JEDEC outline code changed.
57	Added Standards Documentation Sources.
58-60	Added List of Data Sheet Changes.

- NOTES -



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