

Dual N- and P-Channel ± 20 -V Low-Threshold MOSFET

PRODUCT SUMMARY

Channel	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (mA)
N-Channel	20	2.0 @ $V_{GS} = 4.5$ V	250
		2.5 @ $V_{GS} = 2.5$ V	150
P-Channel	-20	3.8 @ $V_{GS} = -4.5$ V	-180
		5.0 @ $V_{GS} = -2.5$ V	-100

FEATURES

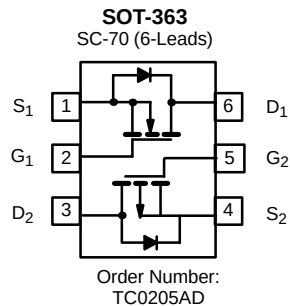
- Very Small Outline (SC-70, 6-Leads)
- Low On-Resistance: 2.0 Ω (N-Ch)
- Low Threshold: 0.9 V (typ)
- Fast Switching Speed: 35 ns
- 2.5-V or Lower Operation

BENEFITS

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation

APPLICATIONS

- Replace Digital Transistors, Level-Shifter
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching-Cell Phones, PDA



Marking Code: EwI

E = Part Number Code for TC0205AD

w = Week Code

I = Lot Traceability

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	20	−20	V
Gate-Source Voltage		V _{GS}	± 8	± 8	
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	250	−180	mA
	T _A = 70°C		200	−140	
Pulsed Drain Current		I _{DM}	500	−500	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	0.20 (Total)		W
	T _A = 70°C		0.13 (Total)		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	625 (Total)	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

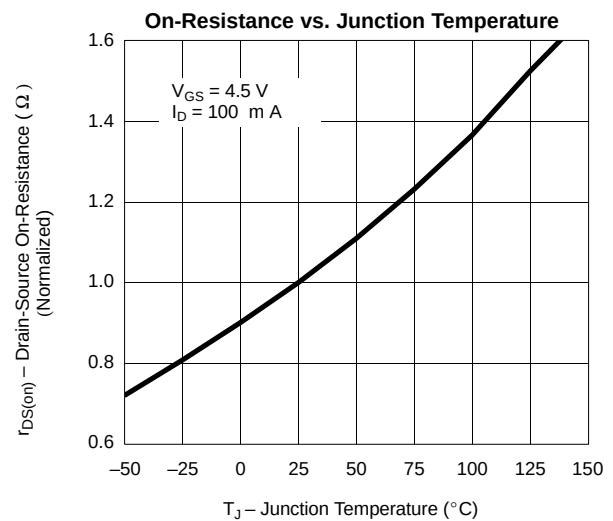
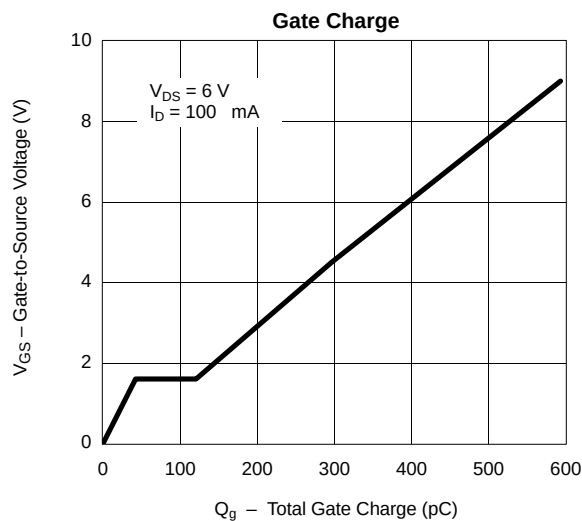
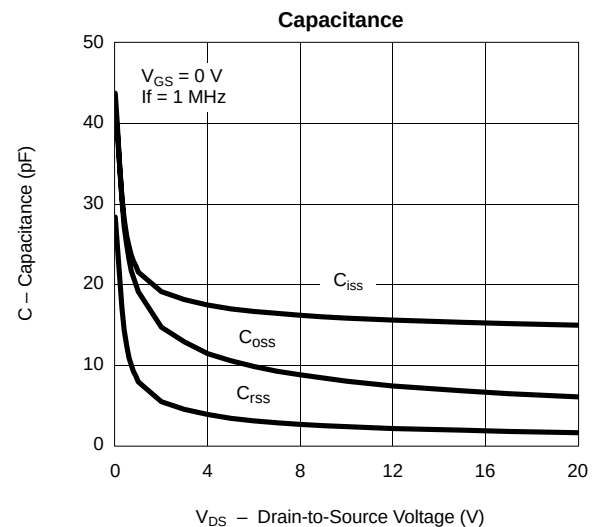
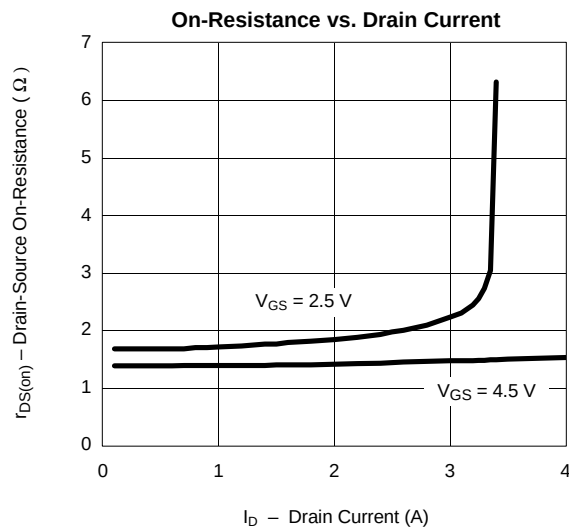
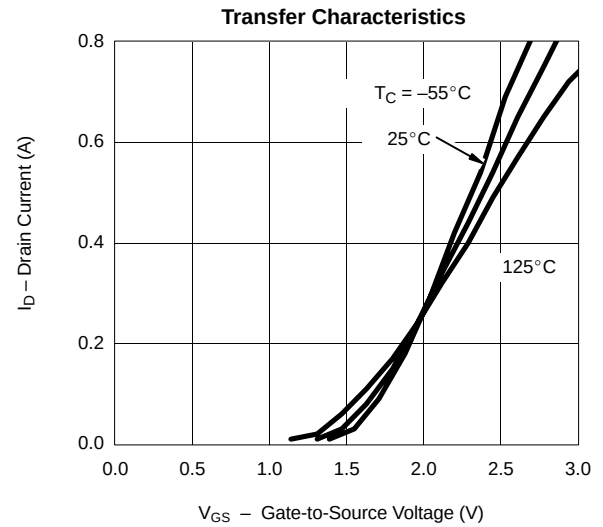
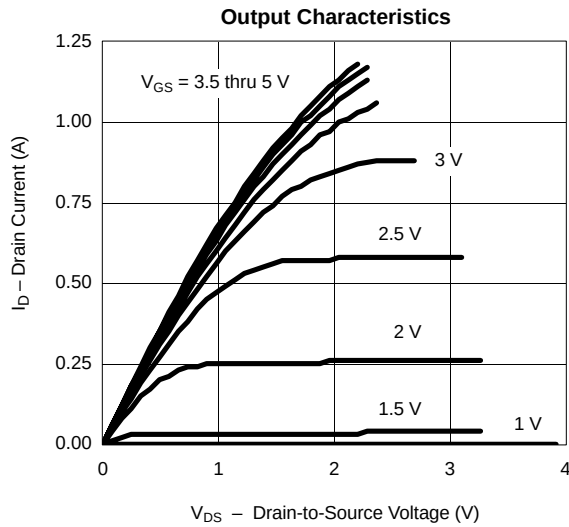
SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

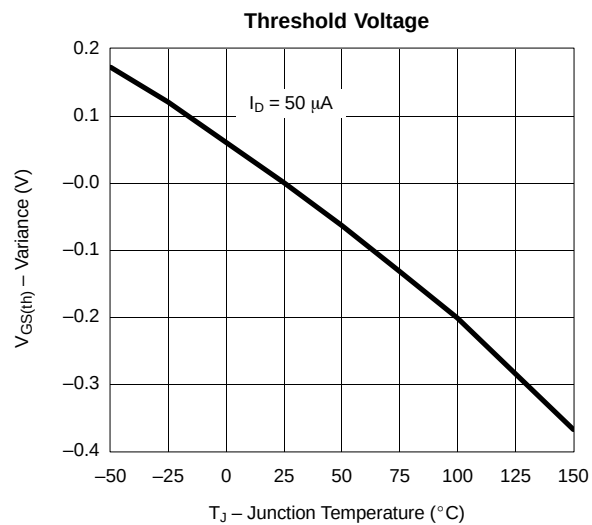
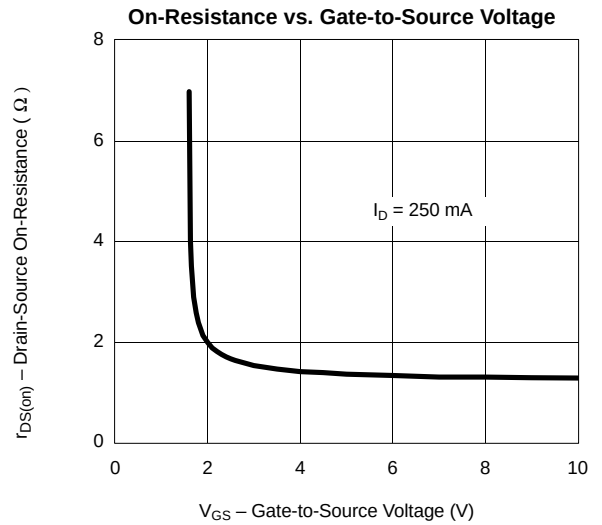
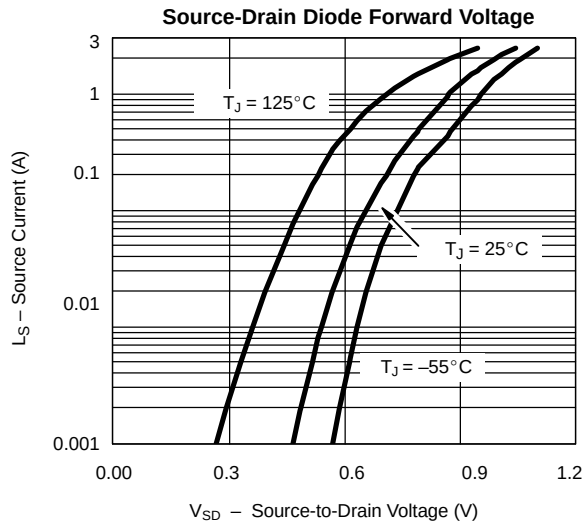
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit		
Static									
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 10 μA	N-Ch	20	24		V		
		V _{GS} = 0 V, I _D = −10 μA	P-Ch	−20	−24				
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 50 μA	N-Ch	0.4	0.9	1.5			
		V _{DS} = V _{GS} , I _D = −50 μA	P-Ch	−0.4	−0.9	−1.5			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V	N-Ch P-Ch		±2 ±2	±100 ±100	nA		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch		0.001	100			
		V _{DS} = −20 V, V _{GS} = 0 V	P-Ch		−0.001	−100			
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55°C	N-Ch			1	μA		
		V _{DS} = −20 V, V _{GS} = 0 V, T _J = 55°C	P-Ch			−1			
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 2.5 V, V _{GS} = 5.0 V	N-Ch	120			mA		
		V _{DS} ≥ −2.5 V, V _{GS} = −5.0 V	P-Ch	−120					
		V _{DS} ≥ 4.5 V, V _{GS} = 8.0 V	N-Ch	400					
		V _{DS} ≥ −4.5 V, V _{GS} = −8.0 V	P-Ch	−400					
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 2.5 V, I _D = 150 mA	N-Ch		1.6	2.5	Ω		
		V _{GS} = −2.5 V, I _D = −75 mA	P-Ch		4	5			
		V _{GS} = 4.5 V, I _D = 250 mA	N-Ch		1.2	2.0			
		V _{GS} = −4.5 V, I _D = −180 mA	P-Ch		2.6	3.8			
Forward Transconductance ^b	g _{fs}	V _{DS} = 2.5 V, I _D = 50 mA	N-Ch		150		mS		
		V _{DS} = −2.5 V, I _D = −50 mA	P-Ch		200				
Diode Forward Voltage ^b	V _{SD}	I _S = 50 mA, V _{GS} = 0 V	N-Ch		0.7	1.2	V		
		I _S = −50 mA, V _{GS} = 0 V	P-Ch		−0.7	−1.2			
Dynamic ^a									
Total Gate Charge	Q _g	N-Channel V _{DS} = 5 V, V _{GS} = 4.5 V, I _D = 100 mA P-Channel V _{DS} = −5 V, V _{GS} = −4.5 V, I _D = −100 mA	N-Ch P-Ch		300 300	450 450	pC		
Gate-Source Charge	Q _{gs}		N-Ch P-Ch		25 25				
Gate-Drain Charge	Q _{gd}		N-Ch P-Ch		100 100				
Input Capacitance	C _{iss}	N-Channel V _{DS} = 5 V, V _{GS} = 0 V P-Channel V _{DS} = −5 V, V _{GS} = 0 V	N-Ch P-Ch		15 15		pF		
Output Capacitance	C _{oss}		N-Ch P-Ch		11 11				
Reverse Transfer Capacitance	C _{rss}		N-Ch P-Ch		5 5				
Switching									
Turn-On Time	t _{d(on)}		N-Channel V _{DD} = 3 V, R _L = 100 Ω I _D = 0.25 A, V _{GEN} = 4.5 V, R _G = 10 Ω P-Channel V _{DD} = −3 V, R _L = 100 Ω I _D = −0.25 A, V _{GEN} = −4.5 V, R _G = 10 Ω	N-Ch P-Ch		7 7		12 12	ns
Rise Time	t _r	N-Ch P-Ch			25 25	35 35			
Turn-Off Delay Time	t _{d(off)}	N-Ch P-Ch			19 19	30 30			
		N-Ch P-Ch			9 9	15 15			

Notes

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

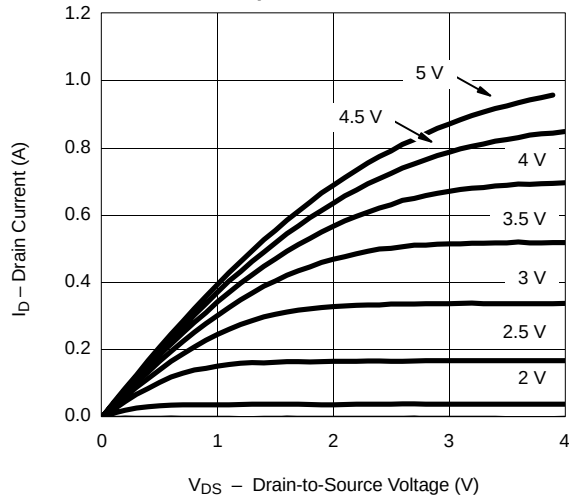
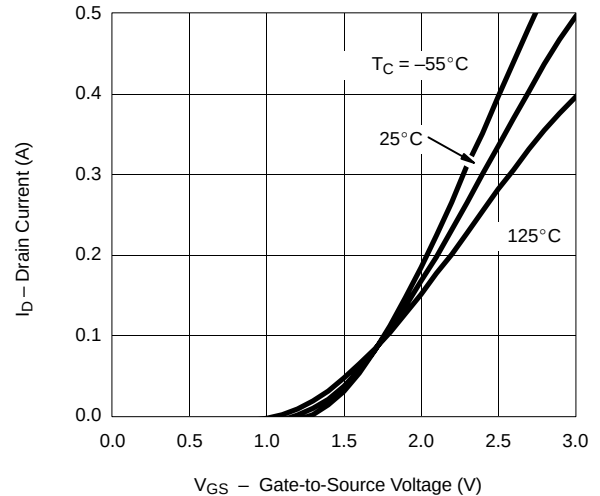
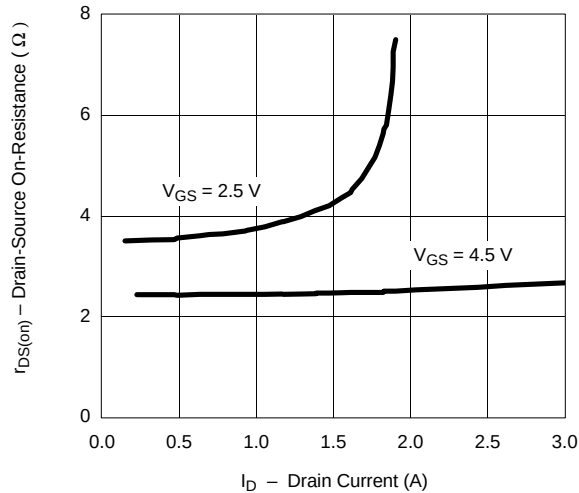
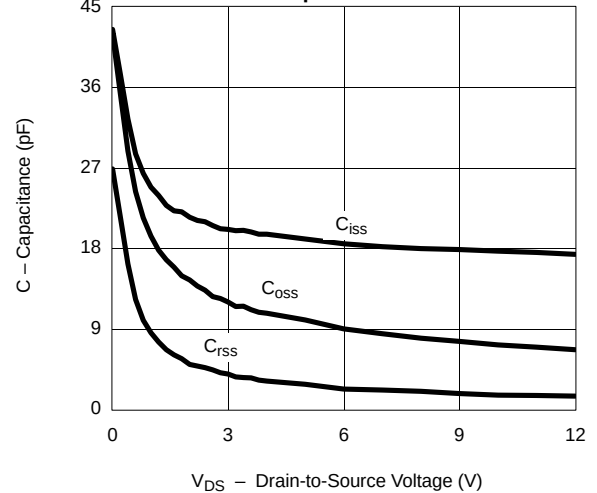
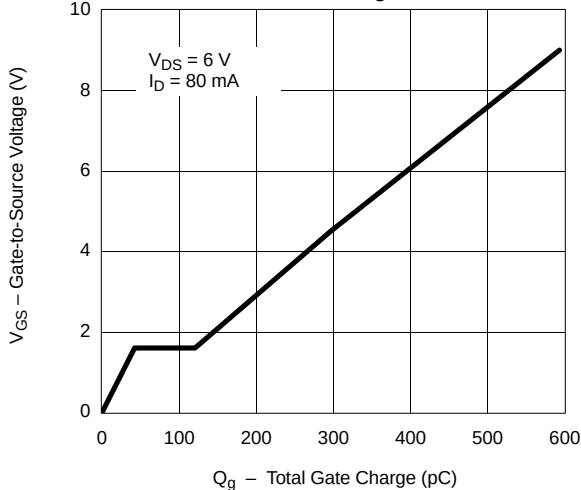
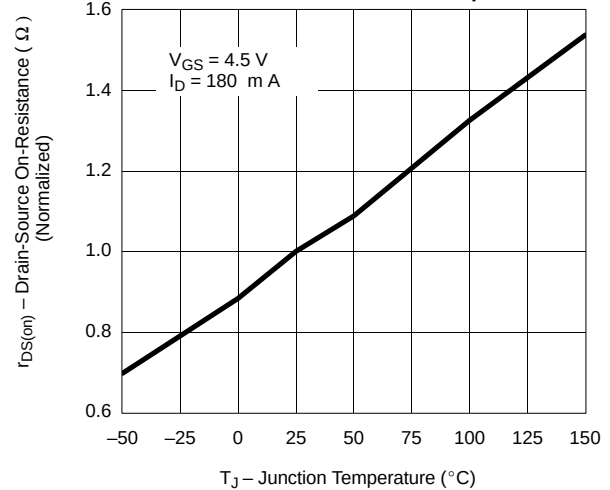
VNOJ
VPOJ

**TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)****N-CHANNEL**

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**TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)****P-CHANNEL**

For the following graphics p-channel negative polarities for all voltage and current values are represented as positive values.

Output Characteristics**Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)**P-CHANNEL**

For the following graphics p-channel negative polarities for all voltage and current values are represented as positive values.

