TNETA1500A
155.52-MBIT/S SONET/SDH ATM RECEIVER/TRANSMITTER

SDNS042A – AUGUST 1997 – REVISED JANUARY 1998

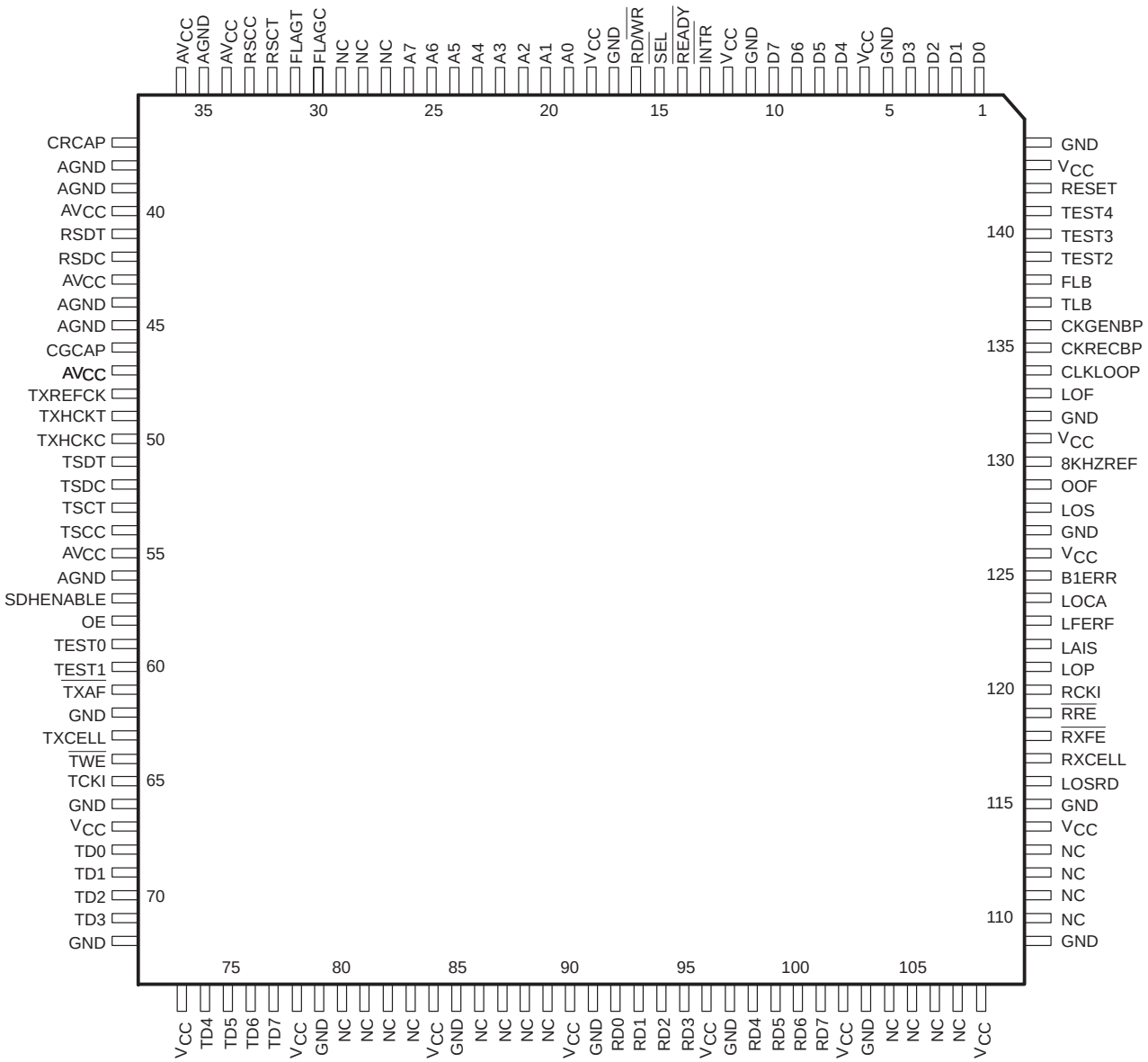
- **Single-Chip Receiver/Transmitter for Transporting 53-Byte Asynchronous Transport Mode (ATM) Cells Via STS-3c/STM-1 Frame (155.52 Mbit/s)**
- **On-Chip Analog Phase-Locked Loop (APLL) Provides:**
  - **Recovery of Receive Clock From Incoming Serial-Data Stream**
  - **Transmit Clock Generation From External 19.44-MHz Clock Source**
- **Inserts and Extracts ATM Cells Into/From SONET/SDH STS-3c/STM-1 SPE**
- **Detects Multiple-Bit Errors and Corrects Single-Bit Errors in the 5-Byte ATM Headers of Incoming ATM Cells**
- **Generates Alarms for:**
  - **Loss of Incoming Serial Signal (LOS)**
  - **Out of Frame (OOF)**
  - **Loss of Frame (LOF)**
  - **B1-Byte Parity Error (B1ERR)**
  - **Loss of ATM Cell Alignment (LOCA)**
  - **Line Far-End Receive Failure (LFERF)**
  - **Receive Loss of Pointer (LOP)**
  - **Line Alarm Indication Signal (LAIS)**
- **Meets ATM Forum ATM User-Network Interface Specification Requirement**
- **Package Options Include 144-Pin Plastic Quad Flat (PCM) and 144-Pin Thin Quad Flat (PGE) Packages**

description

The synchronous optical network (SONET)/synchronous digital hierarchy (SDH) asynchronous transport mode (ATM) line-interface receiver/transmitter provides a single-chip implementation for transporting ATM cells over the SONET/SDH network at the STS-3c/STM-1 rate of 155.52 Mbits/s. This device provides all the functionality required to insert and extract 53-byte ATM cells into/from an STS-3c/STM-1 synchronous payload envelope (SPE), including clock recovery and clock generation using analog phase-locked loops (APLL).

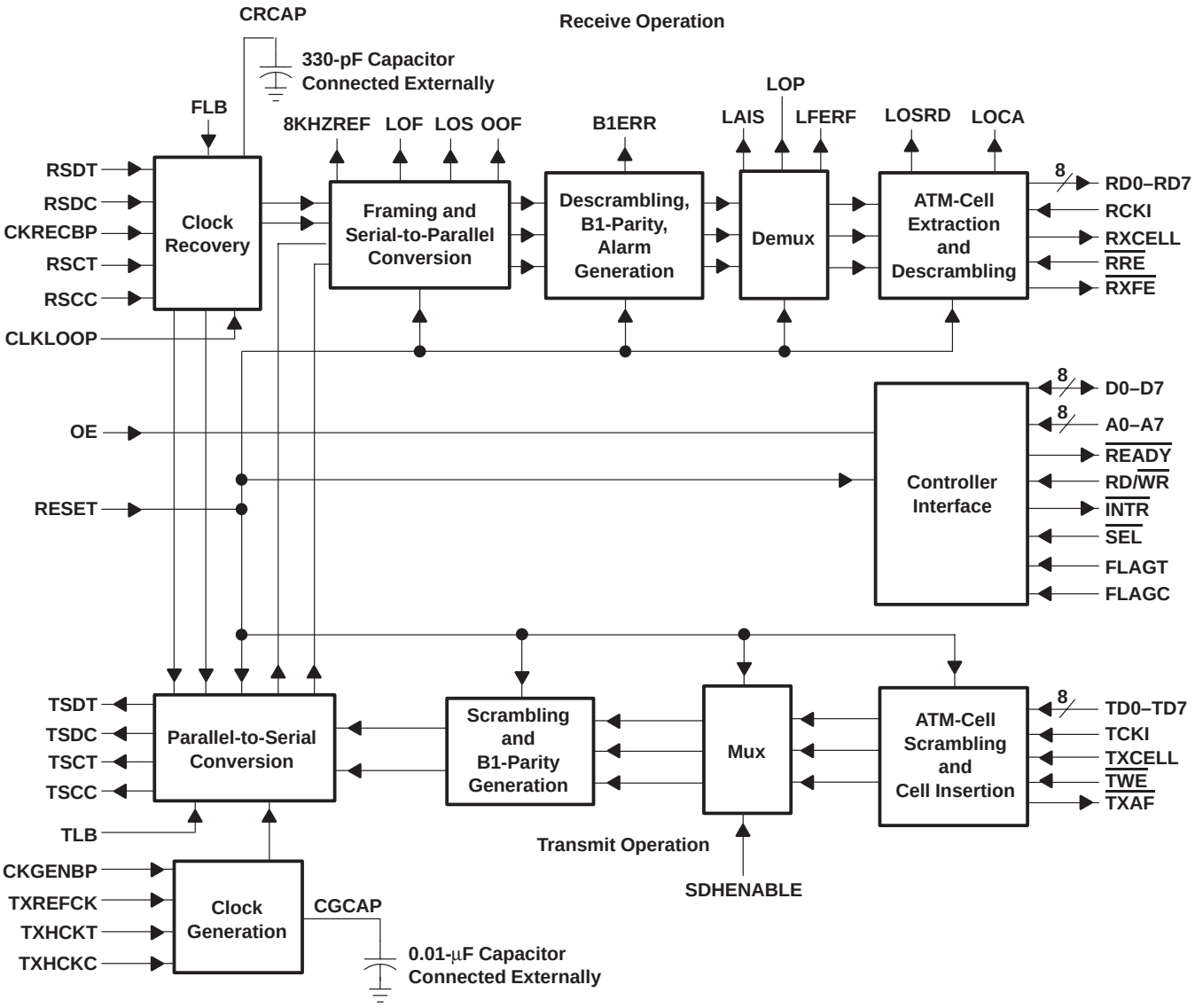
On the receive side, the TNETA1500A accepts 155.52-Mbit/s serial data, recovers the embedded clock signal, performs SONET/SDH frame alignment and serial-to-parallel conversion, identifies the SONET/SDH payload, and establishes the ATM-cell boundaries. The ATM cells are extracted from the payload, descrambled, and passed to the receive output FIFO for output to the next device (i.e., a reassembly device). On the transmit side, complete 53-byte ATM cells are placed in the transmit input FIFO, scrambled, and inserted into an STS-3c/STM-1 SPE. The SONET/SDH frame is scrambled and converted to a serial-data stream for output. An APLL is used to generate the 155.52-MHz output clock from a low-speed 19.44-MHz oscillator, eliminating the need for a high-speed 155.52-MHz oscillator.

PCM OR PGE PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagram



detailed description

transmit operation

The transmit-cell interface consists of the byte-wide input data (TD0–TD7), input clock (TCKI), start of ATM-cell input (TXCELL), transmit write-enable input ($\overline{\text{TWE}}$), and transmit-input FIFO almost-full output ($\overline{\text{TXAF}}$). Input data is clocked into the TNETA1500A on low-to-high transitions of TCKI when $\overline{\text{TWE}}$ is low. The transmit-input FIFO almost-full flag ($\overline{\text{TXAF}}$) goes active when the transmit FIFO is within five bytes of filling up (the FIFO holds three complete ATM cells).

The 48-byte information field of the ATM cell is scrambled using a self-synchronizing scrambler polynomial of $x^{43} + 1$ to improve the efficiency of the cell-delineation procedure. At startup, the scrambler is initialized to an all-1s state. The 5-byte ATM header is not scrambled at this step. TXCELL identifies the first byte of the ATM cell and disables the scrambler. The input data is stored in the transmit-input FIFO and multiplexed into the SONET/SDH payload after all 53 bytes have been received. If the FIFO does not contain 53 bytes of information at the start of a cell-insertion cycle, an idle or unassigned cell is sent, dependent on the status of the control registers. An idle cell is defined as an ATM cell with the 5-byte header set to 00 00 00 01 52 (hex) and the 48-byte payload set to 6A (hex). An unassigned cell is defined as an ATM cell with the 5-byte header set to 00 00 00 00 55 (hex) and the 48-byte payload set to 6A (hex). See *controller-interface operation* for more information on the operation of the control registers.

The transmit section calculates the header-error-check (HEC) byte in the ATM header by default. This implies that the fifth byte of the ATM cell that is input through the transmit-cell interface is ignored. The HEC byte is calculated in accordance with the ANSI T1.624-1993 and CCITT recommendation I.432. This feature can be disabled by setting a bit in the control register.

The transmit operation can be programmed to send either a SONET STS-3c frame or an SDH STM-1 frame. When SDHENABLE is low, a SONET STS-3c frame is transmitted. When SDHENABLE is high, an STM-1 frame is transmitted. For both the STS-3c and STM-1 frames, the location of the J1 byte in the path overhead is fixed; the J1 byte always comes after the third C1 byte of the transport overhead (TOH). This is known as location 522. The data-communication channels (D1 through D12 bytes) in the TOH are set to a hex value of FF 00 00. The values for the transport- and path-overhead bytes for both an STS-3c frame and an STM-1 frame are given in Table 1.

The parity bytes B1, B2 (three bytes), and B3 are calculated as follows:

B1 — B1 is a bit-interleaved parity-8 (BIP-8) code using even parity. B1 is calculated over all bits of the previous STS-3c frame after scrambling. The calculated value of B1 is placed in the STS-3c frame before the frame is scrambled.

B2 — For an STS-3c frame, the three B2 bytes combine to form a BIP-24 code; however, each B2 byte is calculated as if the frame is composed of three individual STS-1s. Each B2 is calculated over all bits of the line overhead and STS-1 envelope capacity of the previous STS-1 frame before scrambling, using even parity. The computed value is placed in the appropriate B2 byte location before scrambling. The line overhead consists of the six rows of TOH bytes, beginning with the first H1 byte and ending before the row containing the first A1 byte (see Table 1).

B3 — For an STS-3c frame, the B3 byte is calculated over all bits of the previous STS-3c SPE before scrambling. B3 is a BIP-8 code, using even parity. The computed value is placed in the B3 location before scrambling.

transmit operation (continued)

Table 1. Transmit Transport-Overhead and Path-Overhead Bytes

OVERHEAD BYTE		SONET FRAME VALUE WHEN SDHENABLE = LOW		SDH FRAME VALUE WHEN SDHENABLE = HIGH	
A1		1111 0110 (F6h)		1111 0110 (F6h)	
A2		0010 1000 (28h)		0010 1000 (28h)	
C1 bytes		01 02 03 (h)		01 00 00 (h)	
B1		Calculated		Calculated	
B2					
B3					
First H1		0110 0010 (62h)		0110 1010 (6Ah)	
Second H1 (H1*)		1001 0011 (93h)		1001 1011 (9Bh)	
Third H1 (H1*)					
First H2		0000 1010 (0Ah)		0000 1010 (0Ah)	
Second H2 (H2*)		1111 1111 (FFh)		1111 1111 (FFh)	
Third H2 (H2*)					
Three H3 bytes		0000 0000 (00h)		0000 0000 (00h)	
First K2		Normal operation: 0000 0000 Line FERF: 0000 0110		Normal operation: 0000 0000 Line FERF: 0000 0110	
Third Z2		B2 error count: 0000 0000–0001 1000		B2 error count: 0000 0000–0001 1000	
J1		0000 0000		0000 0000	
C2		0001 0011		0001 0011	
G1	Bits 1–4	B3 error count: 0000–1000	Path FERF: 1001	B3 error count: 0000–1000	Path FERF: 1001
	Bit 5	Path RDI: 1		Path RDI: 1	
	Bits 6–8	000		000	
H4		0000 0000		0000 0000	

Before transmission, the STS-3c frame is scrambled using a generating polynomial of $x^7 + x^6 + 1$. The A1, A2, and C1 overhead bytes are not scrambled, and the scrambler is reset to 1111111 on the most-significant bit of the byte immediately following the third C1 byte. The scrambler runs continuously throughout the complete STS-3c frame.

After the STS-3c frame has been scrambled, the bytes are converted to a serial-data stream using a parallel-to-serial converter. An APLL is used to generate the 155.52-MHz output clock from a 19.44-MHz oscillator connected to TXREFCK. Two other sources can be used for the 155.52-MHz clock. CKGENBP and CLKLOOP are used to select either a 155.52-MHz external clock source or the clock recovered from the incoming serial-data stream APLL (loop timing). The functions for selecting the transmit-clock source are shown in Table 2. The clock-generation APLL requires that an external 0.01-μF capacitor be connected from CGCAP to ground.

transmit operation (continued)

Table 2. Functions for CKGENBP and CLKLOOP

CKGENBP	CLKLOOP	CLOCK SOURCE
L	L	TXREFCK (19.44 MHz)
L	H	Receive recovered clock (loop timing)
H	H or L	TXHCKT, TXHCKC (155.52 MHz)

Both true and complementary pseudo-emitter-coupled logic (PECL)-compatible serial data and clock outputs are available. The serial data is output on the rising edge of the true clock signal (falling edge of the complement clock). The outputs are designed to drive a 50-Ω line terminated through a 50-Ω resistor to 3 V (or its equivalent).

A terminal-loopback feature also is provided on the device. When the terminal-loopback input is high, the ATM cells received on the transmit input are looped back to the receive output. The ATM cells received are blocked. The transmit operation is not affected in this mode and operates as previously described.

receive operation

The receive serial inputs to the TNETA1500A consist of 155.52-Mbit/s true and complementary PECL data and an optional 155.52-MHz true and complementary PECL clock. The 155.52-MHz clock inputs are needed only if the clock-recovery-bypass input (CKRECBP) is high, which disables the clock-recovery circuit. This feature is used typically for test purposes and normally is not used in a system application.

The clock-recovery circuit is used to recover the embedded clock signal from the serial nonreturn-to-zero (NRZ) data inputs RSDT and RSDC. The clock-recovery circuit consists of a transition detector, an APLL, and a retiming circuit. The transition detector is used to double the frequency of the incoming serial-data stream. This is necessary because the NRZ-data stream does not contain a second harmonic, which is necessary to recover the transmit clock. The APLL consists of a phase-frequency detector, a charge pump/loop filter, and an internal voltage-controlled oscillator (VCO). The phase-frequency detector compares the output of the transition detector to the output of the VCO and generates a signal to the charge-pump/loop filter that is used to change the frequency of the VCO. The frequency of the VCO is adjusted until it matches the frequency of the transition detector. When this occurs, the APLL is locked to the frequency of the embedded clock signal.

The clock-recovery circuit also contains a circuit that retimes the input serial data to the recovered output clock. The only external component required for the clock-recovery circuit is a 330-pF capacitor that is connected from CRCAP to ground. This capacitor is part of the charge-pump/loop-filter circuit.

The clock signal recovered from the incoming serial-data stream also can be used as the transmit clock for the transmit section. This is known as clock looping. The advantage of using the recovered receive clock as the transmit clock is that the transmit clock is frequency locked to the same clock source that is used to generate the incoming data stream. If this clock source provides a highly accurate low-parts-per-million clock, the transmit clock also is a very accurate clock. The drawback to using clock looping is that if the receive signal is lost for any reason, the transmit clock also is lost.

A facility-loopback (FLB) input loops the input data and recovered clock to the transmit output data and clock. This provides a method of testing the function of the clock-recovery circuit and its jitter performance. It also can be used for system-loopback testing.

The PECL inputs FLAGT and FLAGC are provided for interfacing to the loss-of-optical-signal outputs on optical receivers. If the optical signal is lost, the loss-of-optical-carrier bit in the interrupt register is set and the interrupt output ($\overline{\text{INTR}}$) becomes active low.

The recovered clock signal and retimed input data are passed from the clock-recovery circuit to the framing circuit. The framing circuit searches for the SONET framing bytes A1 and A2, where A1 has a set value of F6h and A2 has a value of 28h. The exact framing pattern for an STS-3c frame is A1A1A1A2A2A2 (F6F6F6282828h). These bytes are not scrambled by the transmitter.

receive operation (continued)

The TNETA1500A provides loss-of-signal (LOS), out-of-frame (OOF), and loss-of-frame (LOF) alarms in accordance with BellCore specification TR-NWT-000253, Issue 2, December 1991. The LOS alarm goes active when no transitions are detected on the receive serial data for 3.3 μs. The LOS alarm goes inactive when two consecutive framing patterns have been detected, and during the intervening time (one frame time), no transitionless 3.3-μs period is detected. The OOF alarm goes active when four consecutive-errored framing patterns are received. The OOF alarm clears when two successive error-free framing patterns are received. If the OOF condition fails to clear within 3 ms, the LOF alarm goes active. The LOF alarm goes inactive when eight consecutive error-free SONET frames are identified. The LOS, OOF, and LOF alarms are indicated by external signals and by setting a bit in the interrupt registers. This causes $\overline{\text{INTR}}$ of the controller interface to go active low, signaling an interrupt.

After the SONET frame is established and the serial data converted to byte-wide data, the B1 BIP-8 parity is calculated over the scrambled SONET frame. This value is compared with the value of B1 contained in the next (n + 1) frame. The value of B1 calculated over the previous frame (n – 1) is compared to the value B1 in this frame (frame n). If the two values do not match, B1ERR goes active, denoting that a B1 parity error has occurred. In addition, the B1 parity-error bit in the interrupt register is set and $\overline{\text{INTR}}$ goes active low.

Next, the SONET frame is unscrambled (except for the A1, A2, and C1 bytes, which were not scrambled by the transmitter). The B2 BIP-24 value is calculated over all the bits of the line overhead and the STS-3c envelope capacity and compared to the value contained in the next frame. If a B2 parity error occurs, the B2 parity-error bit in the interrupt register is set and $\overline{\text{INTR}}$ goes active low to notify the controller that a parity error has occurred.

The TNETA1500A monitors the receive K2 byte for line alarm-indication signal (LAIS) and line far-end receive failure (LFERF) alarms. A LAIS alarm occurs when bits 6–8 of the receive K2 byte are set to a value of 111 for five consecutive frames. The LAIS alarm goes inactive when bits 6–8 of the receive K2 byte are set to any value other than 111 for five consecutive frames. The LFERF alarm goes active when bits 6–8 of the receive K2 byte are set to a value of 110 for five consecutive frames. The LFERF alarm goes inactive when bits 6–8 of the receive K2 byte are set to any value other than 110 for five consecutive frames. Both the LAIS and LFERF alarms are indicated on an external terminal and by setting a bit in interrupt register 2.

The location of the J1 byte in the SPE is determined from the H1 and H2 bytes in the TOH. The location of the J1 byte does not change from the previous frame unless the first four bits of H1 are set to 1001 (the new-data flag) or the pointer value contained in H1 and H2 is different for three consecutive frames. The location of J1 also can be incremented or decremented by a 1-byte position by inverting certain bits in the H1 and H2 byte pointer. If bits 7, 9, 11, 13, and 15 are inverted, the location of J1 is incremented one time slot. If bits 8, 10, 12, 14, and 16 are inverted, the location of J1 is decremented one time slot. Subsequent pointers contain the new offset.

The TNETA1500A provides a loss-of-pointer (LOP) alarm to indicate that either an invalid pointer was detected in the incoming H1 and H2 bytes or a new-data flag (NDF) (set to a value of 1001 — the first four bits of H1) was found in eight consecutive frames. The LOP alarm goes inactive when a valid pointer with the NDF set to 0110 is detected in three consecutive frames. The device also provides a path-AIS alarm to indicate that a path-AIS condition has been detected in the H1 and H2 bytes. A path-AIS condition is detected as an all-1s condition in bytes H1 and H2 for three consecutive frames. The path-AIS alarm goes inactive when a valid pointer, with the NDF set to 0110, is detected for three consecutive frames. The LOP alarm is not set if a path-AIS condition is detected. The LOP alarm is indicated by an external signal and by the interrupt register. The path-AIS alarm is indicated only by the interrupt register.

The B3 BIP-8 byte is calculated over the contents of the STS-3c SPE, which begins with the J1 byte. The value calculated for B3 is compared with the value found in the next frame. If a B3 parity error occurs, the B3 parity-error bit is set in the interrupt register and $\overline{\text{INTR}}$ goes active low to notify the controller.

receive operation (continued)

The TNETA1500A monitors the receive G1 byte for a path far-end receive failure (FERF) and path remote-defect indication (RDI) alarms. A path FERF occurs when bits 1–4 of the G1 byte are set to a value of 1001. The path FERF alarm goes inactive when bits 1–4 of the G1 byte are set to a non-1001 value. A path RDI occurs when bit 5 of the G1 byte is set to a value of 1 for ten consecutive frames. The path RDI alarm goes inactive when bit 5 of the G1 byte is set to a value of 0 for ten consecutive frames. Both the path FERF and path RDI alarms are indicated through interrupt register 3.

Once the STS-3c SPE is located, the ATM cells are identified and extracted. Cell delineation is accomplished by computing the HEC for the first four bytes after the J1 byte and comparing the calculated value with the fifth byte. If the values do not match, the process advances one byte and then repeats. This process continues until a match between the calculated value and the fifth byte occurs. Cell alignment is assumed to have occurred when seven consecutive matches occur. Until cell alignment occurs, the loss-of-cell-alignment (LOCA) alarm remains active. Once cell alignment is established, it is monitored constantly for a LOCA condition. A LOCA condition is declared (LOCA goes active) when seven consecutive cells occur with header errors. At this point, the hunting process starts over.

The receive side detects multiple-bit errors and corrects single-bit errors occurring in the 5-byte ATM header of incoming ATM cells by using the HEC byte. This feature is deactivated by setting a bit in control register 1 (see Table 6). The ATM cells with multiple-bit header errors are dropped, unless a bit is set in control register 1 (see Table 6) to disable the dropping of cells with uncorrectable errors. An 8-bit saturating counter (accessible through the controller interface) counts the number of ATM cells with multiple-bit ATM-header errors.

After the ATM cells are extracted, they are descrambled. The 48-byte payload in the ATM cell is scrambled at the transmitter using an $x^{43} + 1$ polynomial to further distinguish the payload from the header bytes and improve the efficiency of the cell-delineation algorithm. The $x^{43} + 1$ polynomial also is used to descramble the payload so that it can be sent to the next device.

The TNETA1500A has the capability of dropping idle and unassigned cells from the receive-data stream. An idle cell is defined as a cell with a 5-byte ATM header set to a value of 00 00 00 01 52 (hex) and an unassigned cell is defined as a cell with a 5-byte header of 00 00 00 00 55 (hex). In both cases, the payload is ignored. The dropping of idle and/or unassigned cells can be disabled through control register 1 (CR1) in the controller interface.

After descrambling, the ATM cell is passed to the output buffer, which operates as a FIFO. The receive-cell interface consists of the output data (RD0–RD7), receive-clock input (RCKI), receive-read-enable ($\overline{\text{RRE}}$) input, receive-FIFO-empty ($\overline{\text{RXFE}}$) output, beginning-of-ATM-cell indicator (RXCELL), and loss-of-receive-data (LOSRD) alarm. Data is sent out from the device on the rising edge of RCKI when $\overline{\text{RRE}}$ is low. The LOSRD alarm goes active when the output FIFO overflows. In this case, the last cell placed into the FIFO is overwritten. The output FIFO holds three complete ATM cells.

Cumulative counts of receive B1, B2, and B3 errors are provided by registers accessible through the controller interface. These registers maintain running totals of B1, B2, and B3 block errors and coding violations. The block-error counters maintain a count of the number of frames that are received with B1, B2, and B3 errors. The coding-violation counters count the exact number of B1, B2, and B3 BIP errors that occur. It is possible for a single frame to contain 8 B1, 24 B2, and 8 B3 BIP errors. When any of the block-error or coding-violation counters reach maximum count, a bit is set in the interrupt registers and an interrupt is generated. These counters are rollover counters that roll over to zero after the maximum count occurs and an interrupt is generated (see the controller-interface operation section for additional information).

When the receive side enters a LOCA state, a path RDI may need to be sent out the transmit side through the outgoing G1 byte. A path-RDI alarm is declared when a LOCA state is persistent for an amount of time (also known as soak time) that has not yet been specified by any industry standards. To provide maximum flexibility with regard to this unspecified soak time, an 8-bit counter is provided through the controller interface that allows the user to program the amount of soak time for a path-RDI alarm in increments of 125 µs. This counter is preset (when a device reset occurs) to a value of 4 ms, which is the anticipated soak time for a path-RDI alarm.

controller-interface operation

The controller interface provides access to the internal memory locations that contain the control registers, interrupt registers, interrupt-mask registers, and the ID register. Table 3 shows a memory map of the locations of the various registers in the TNETA1500A.

Table 3. TNETA1500A Register-Memory Map

ADDRESS (HEX VALUE)	REGISTER	ADDRESS (HEX VALUE)	REGISTER
00	Interrupt register 1	0D	B1 block-error counter
01	Interrupt register 2	0E	Not implemented
02	Interrupt register 3	0F	B2 block-error counter
03	ID register	10	Not implemented
04	Not implemented	11	B3 block-error counter
05	Control register 1	12	B1 coding-violation counter (LSB)
06	Control register 2	13	B1 coding-violation counter (MSB)
07	Interrupt-mask register 1	14	B2 coding-violation counter (LSB)
08	Interrupt-mask register 2	15	B2 coding-violation counter
09	Interrupt-mask register 3	16	B2 coding-violation counter (MSB)
0A	Multierrored cell counter	17	B3 coding-violation counter (LSB)
0B	Path-RDI soak counter	18	B3 coding-violation counter (MSB)
0C	Not implemented	>18	Not implemented

interrupt registers

The interrupt registers located at hex addresses 00, 01, and 02 contain information on the condition of the receive-data stream that causes $\overline{\text{INTR}}$ to become active low. The coding for the interrupt registers is given in Table 4.

Table 4. Interrupt-Register Coding

CAUSE OF INTERRUPT	IR1 CODING (ADDRESS 00)	IR2 CODING (ADDRESS 01)	IR3 CODING (ADDRESS 02)
B1 parity error	XXXX XXX1	—	—
B2 parity error	XXXX XX1X	—	—
B3 parity error	XXXX X1XX	—	—
Loss of cell alignment	XXXX 1XXX	—	—
Loss of incoming signal	XXX1 XXXX	—	—
Out of frame	XX1X XXXX	—	—
Loss of frame	X1XX XXXX	—	—
Loss of optical carrier	1XXX XXXX	—	—
Line AIS	—	XXXX XXX1	—
Line FERF	—	XXXX XX1X	—
Loss of receive data	—	XXXX X1XX	—
Loss of pointer	—	XXXX 1XXX	—
Path AIS	—	XXX1 XXXX	—
B1 block-error overflow	—	XX1X XXXX	—
B2 block-error overflow	—	X1XX XXXX	—
B3 block-error overflow	—	1XXX XXXX	—
B1 CV overflow	—	—	XXXX XXX1
B2 CV overflow	—	—	XXXX XX1X
B3 CV overflow	—	—	XXXX X1XX
Path RDI	—	—	XXXX 1XXX
Path FERF	—	—	XXX1 XXXX

The alarm conditions or errors set bits in the interrupt register that cause $\overline{\text{INTR}}$ to go active low. All of these conditional actions are associated with the receive-data stream and are described in the following.

LOS, OOF, LOF, LAIS, LOP, LFERF, LOCA, and LOSRD

These alarm conditions cause an external signal to go active and set a bit in one of the interrupt registers (see *Terminal Functions* tables for description of the individual alarms). The status of the bit in the interrupt register for these alarms mirrors the status of the external signal. For example, as long as an LOF condition exists, both LOF and the LOF bit in IR1 (the value for LOF is x1xx xxxx) are set. When the logic in the TNETA1500A detects that the LOF condition has cleared, the external output and the status bit in the interrupt registers are cleared. A change in the status bit in the interrupt registers for these alarms causes $\overline{\text{INTR}}$ to go active low. When the status bit makes a low-to-high transition, $\overline{\text{INTR}}$ goes active low. $\overline{\text{INTR}}$ also goes active low when the status bit makes a high-to-low transition. Reading the interrupt register does not clear the status bit for these particular alarms. However, $\overline{\text{INTR}}$ goes inactive high on a read of any of the interrupt registers.

loss-of-optical carrier, path AIS, path RDI

These alarm conditions cause a status bit in one of the interrupt registers to go active. When the alarm condition exists, the status bit remains set. When the logic in the TNETA1500A detects that the alarm condition has cleared, the status bit is cleared. A change in the status bit in the interrupt registers for these alarms causes $\overline{\text{INTR}}$ to go active low. When the status bit makes a low-to-high transition, $\overline{\text{INTR}}$ goes active low. $\overline{\text{INTR}}$ also goes active low when the status bit makes a high-to-low transition. Reading the interrupt register does not clear the status bit for these particular alarms. However, $\overline{\text{INTR}}$ goes inactive high on a read of any of the interrupt registers.

B1/B2/B3 parity error, B1/B2/B3 block error overflow, B1/B2/B3 CV overflow

The status bits for these errors indicate that the specified error condition has occurred. The status bits in the interrupt registers for these conditions are set when the error conditions occur and remain set until the interrupt register is read. If a B1, B2, or B3 parity error is detected on an incoming frame, the corresponding status bit is set in the interrupt register, $\overline{\text{INTR}}$ goes active low, and the status bit remains set until a read of any interrupt register occurs. Once a read of any interrupt register occurs, the status bit for one of these error conditions is cleared until the next time that this error condition is detected.

interrupt-mask registers

All of the interrupts in the three interrupt registers can be masked by setting bits in the corresponding interrupt-mask registers. The coding for the interrupt-mask registers is the same as the coding for the interrupt registers. To mask only the interrupt associated with a B2 parity error, a value of 0000 0010 is written to interrupt-mask register 1 (IMR1). To mask all the interrupts in interrupt register 1, a value of 1111 1111 is written to interrupt-mask register 1. After reset, all three interrupt-mask registers are cleared (set to 00 hex). Table 5 shows the coding for the interrupt-mask registers.

Table 5. Interrupt-Mask Register Coding

INTERRUPT TO BE MASKED	IMR1 CODING (ADDRESS 07)	IMR2 CODING (ADDRESS 08)	IMR3 CODING (ADDRESS 09)
B1 parity error	XXXX XXX1	—	—
B2 parity error	XXXX XX1X	—	—
B3 parity error	XXXX X1XX	—	—
Loss of cell alignment (LOCA)	XXXX 1XXX	—	—
Loss of incoming signal (LOS)	XXX1 XXXX	—	—
Out of frame (OOF)	XX1X XXXX	—	—
Loss of frame (LOF)	X1XX XXXX	—	—
Loss of optical carrier	1XXX XXXX	—	—
Line AIS	—	XXXX XXX1	—
Line FERF	—	XXXX XX1X	—
Loss of receive data	—	XXXX X1XX	—
Loss of pointer	—	XXXX 1XXX	—
Path AIS	—	XXX1 XXXX	—
B1 block-error overflow	—	XX1X XXXX	—
B2 block-error overflow	—	X1XX XXXX	—
B3 block-error overflow	—	1XXX XXXX	—
B1 CV overflow	—	—	XXXX XXX1
B2 CV overflow	—	—	XXXX XX1X
B3 CV overflow	—	—	XXXX X1XX
Path RDI	—	—	XXXX 1XXX
Path FERF	—	—	XXX1 XXXX

control registers

The control registers are located at addresses 05 and 06 (hex). The control registers provide a means of controlling the operation of the device through the controller interface. A reset operation, initiated either by taking the RESET signal high or by performing a write operation to the ID register, clears both control registers. The bit definition for the two control registers is shown in Table 6.

Table 6. Coding for Control Registers

ACTION	CONTROL REGISTER 1 (ADDRESS 05)	CONTROL REGISTER 2 (ADDRESS 06)
Disable error correction for receive ATM-cell headers	XXXX XXX1	—
Disable transmit ATM-cell header HEC-byte generation	XXXX XX1X	—
Enable terminal loopback (TLB)	XXXX X1XX	—
Enable facility (serial) loopback (FLB)	XXXX 1XXX	—
Disable the dropping of ATM cells with multiple-bit header errors	XXX1 XXXX	—
Disable the dropping of ATM idle cells from the receive-data stream	XX1X XXXX	—
Disable the dropping of ATM unassigned cells from the receive-data stream	X1XX XXXX	—
Transmit STM-1 frame	1XXX XXXX	—
Enable receive-clock looping	—	XXXX XXX1
Transmit ATM unassigned cells as filler	—	XXXX XX1X

Descriptions of the various control functions of the control registers follow:

disable error correction for receive ATM-cell headers

When set to a high level, this bit causes the error-detection and correction block to stop correcting single-bit errors that are detected in the headers of incoming ATM cells. When a reset operation is performed, this bit is cleared (set to 0). The normal operating state of the TNETA1500A provides single-bit error correction on the headers of incoming ATM cells, and an action must be taken to disable this operation.

disable transmit ATM-cell header HEC-byte generation

When set to a high level, this bit causes the transmit section to stop generating the HEC byte in the 5-byte header of ATM cells transmitted. When a reset operation occurs, this bit is cleared (set to 0). The normal operating mode of the TNETA1500A calculates the HEC byte from the first four bytes of the ATM cell transmitted and inserts the calculated value in the HEC-byte location. This bit is used to disable the generation of the HEC byte.

enable terminal loopback (TLB)

When set to a high level, this bit causes the ATM-cells input (through the transmit-cell interface) to loop through the device and be sent out through the receive-cell interface. The receive serial-data stream is blocked when this mode of operation is chosen. However, the transmit section operates normally and the device continues to transmit ATM cells that are inserted in an STS-3c/STM-1 frame. Internally, this bit is logically ORed with the TLB input, which allows a terminal loopback to be enabled through either the external input or through the control register. When a reset operation occurs, the bit in the control register is cleared.

enable facility (serial) loopback (FLB)

When set to a high level, this bit causes the receive serial data and clock inputs to loop through the device and be sent out through the transmit serial data and clock outputs. The transmit serial-data stream is blocked when this mode of operation is chosen. However, the receive section operates normally, and the device continues to extract ATM cells from the incoming STS-3c/STM-1 frame. Internally, this bit is logically ORed with the FLB input, which allows a facility loopback to be enabled through either the external input terminal or through the control register. When a reset operation occurs, the bit in the control register is cleared.

disable the dropping of ATM cells with multiple-bit header errors

When set to a high level, this bit causes the receive section to stop dropping ATM cells that contain multiple-bit header errors. When a reset operation occurs, this bit is cleared. The normal operation of the TNETA1500A drops ATM cells that contain multiple-bit header errors by not placing them in the receive output FIFO.

disable the dropping of ATM idle cells from the receive-data stream

When this bit is set, the receive section does not drop ATM idle cells from the receive-data stream. An idle cell is defined as an ATM cell with the 5-byte header set to a value of 00 00 00 01 52 (hex). When a reset operation occurs, this bit is cleared. The normal operation of the TNETA1500A is to drop idle cells from the receive-data stream.

disable the dropping of ATM unassigned cells from the receive-data stream

When this bit is set, the receive section does not drop ATM unassigned cells from the receive-data stream. An unassigned cell is defined as an ATM cell with the 5-byte header set to a value of 00 00 00 00 55 (hex). When a reset operation occurs, this bit is cleared. The normal operation of the TNETA1500A is to drop unassigned cells from the receive-data stream.

transmit STM-1 frame

When this bit is set, the transmit section transmits an STM-1 frame instead of an STS-3c frame. Internally, this bit is logically ORed with SDHENABLE, which allows this mode of operation to be enabled either through the control register or the external input. When a reset operation occurs, this bit is cleared and causes the TNETA1500A to transmit an STS-3c frame.

enable receive-clock looping

When this bit is set, the receive clock is used as the clock for the transmit side (clock looping). The receive clock is either the receive serial clock or the clock recovered from the receive serial-data stream, depending on the state of CLKRECBP. Internally, this bit is logically ORed with CLKLOOP, which allows the clock-loop function to be enabled either through the control register or the external input. When a reset operation occurs, this bit is cleared, which disables the clock loop.

transmit ATM unassigned cells as filler

When this bit is set, the transmit side sends ATM unassigned cells for cell rate decoupling when a user-data cell is not available in the transmit FIFO. An unassigned cell is defined as a cell with the 5-byte header set to a value of 00 00 00 00 55 (hex). The payload is set to 6A (hex). When this bit is not set, the device sends idle cells as filler cells for cell-rate decoupling. An idle cell is defined as a cell with the 5-byte header set to a value of 00 00 00 01 52 (hex) and the payload set to 6A (hex). When a reset operation occurs, this bit is cleared.

ID register

The ID register is located at address 03 (hex). This register identifies the device revision and also provides a means of performing a software reset. The contents of this register are hardwired to a hexadecimal value of Ax (x denotes the chip revision). A software reset on the TNETA1500A is initiated by writing to the ID register through the controller interface. Since the contents of the ID register are firmware, the write does not change the contents of the register. The software-reset function is logically ORed with RESET. A reset of the TNETA1500A device is initiated through either the external input or the ID register.

multierrored cell-header counter

The multierrored cell-header counter is a saturating 8-bit counter that counts the number of ATM cells that are received with multiple-bit errors in the 5-byte ATM header. This counter resets to zero when the register is read. This counter does not cause $\overline{\text{INTR}}$ to go active low when the counter reaches maximum count. This counter is set to zero when a reset operation occurs.

path-RDI soak counter

This counter provides a count of the amount of time, in increments of 125 μs, that a LOCA condition must be present before a path-RDI condition is sent via the outgoing G1 byte. The amount of time required is not currently specified by any industry standard. This counter is preset to a value of 4 ms when a reset operation occurs. The counter value is modified by writing a new value to the counter through the controller interface. For instance, to set the value in the counter to 1 ms, a value of eight (8×125 μs = 1 ms) is written in the counter. However, the value in the counter is rewritten if a reset operation occurs because the counter is reset to 4 ms.

B1/B2/B3 block-error counters

These counters maintain the total number of frames received with B1, B2, and B3 errors. These counters track the number of frames with errors, not the number of actual B1, B2, and B3 bits in error. All three counters are 8-bit counters. These 8-bit counters are read only and a reset operation clears all three counters. When these counters reach their maximum count, $\overline{\text{INTR}}$ goes active low and a bit is set high in the interrupt register IR2. The host system reads the IR registers to determine the cause of the interrupt. The host reads the counters to reset them to zero, and finally, the host system reads IR2 again to clear the $\overline{\text{INTR}}$ line and the block-error-counter bit on the IR2.

B1/B2/B3 coding-violation counters

These counters maintain the total number of receive B1, B2, and B3 BIP bits that are in error. The B1 and B3 counters are 16-bit counters, and the B2 counter is a 19-bit counter. When one of the counters reaches its maximum count, $\overline{\text{INTR}}$ goes active low and a bit in the interrupt register is set. After the counters reach their maximum count, they roll over and continue to count. To clear the interrupt condition, the host system reads any of the three interrupt registers. After the host reads both counters in this sequence, both LSB and MSB counters are reset to zero. The device clears both counters after the MSB counter is read. Software must read LSB first to obtain its value before the LSB and MSB counters are cleared. A reset operation clears all three counters. Since these counters are read only, a value cannot be written to any of the three counters.

Terminal Functions

high-speed serial differential interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
FLAGC, FLAGT	30, 31	I (PECL)	Loss-of-optical-carrier alarm (true and complement). FLAGC and FLAGT are connected to a fiber-optic receiver loss-of-optical-carrier output to provide an interrupt through the controller interface when the incoming optical signal is lost.
RSCT, RSCC	32, 33	I (PECL)	Receive serial clock (true and complement). RSCT and RSCC are used to clock in serial data on RSDT and RSDC when the clock-recovery phase-lock loop is bypassed by taking CKRECBP high.
RSDT, RSDC	41, 42	I (PECL)	Receive serial data (true and complement). RSDT and RSDC are differential PECL inputs.
TSCT, TSCC	53, 54	O (PECL)	Transmit serial clock (true and complement). TSCT and TSCC provide the transmit serial output clock. This clock is derived from either the receive serial clock, the output of the clock generation phase-lock loop, or the transmit high-speed clock, depending on the state of CKGENBP and CLKLOOP.
TSDT, TSDC	51, 52	O (PECL)	Transmit serial data (true and complement). TSDT and TSDC data is output on TSCT and TSCC.
TXHCKT, TXHCKC	49, 50	I (PECL)	Transmit high-speed clock (true and complement). TXHCKT and TXHCKC (155.52 MHz) provide the transmit serial clock when CKGENBP is high.

alarm indicators

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
B1ERR	125	O	B1 error. A high on B1ERR indicates that a B1 parity-byte error is detected on the incoming frame.
LAIS	122	O	Line alarm-indication signal. A high on LAIS indicates that bits 6–8 of the receive K2 byte are set to 111 for five consecutive frames. The alarm clears when any non-111 pattern is detected in bits 6–8 of the receive K2 byte for five consecutive frames.
LFERF	123	O	Line far-end receive failure. A high on LFERF indicates that bits 6–8 of the receive K2 bytes are set to 110 for five consecutive frames. The alarm clears when any non-110 pattern is detected in bits 6–8 of the receive K2 byte for five consecutive frames.
LOCA	124	O	Loss of cell alignment. A high on LOCA indicates that ATM cells cannot be found in the incoming data stream. LOCA goes inactive when the cell-delineation algorithm finds seven consecutive ATM cells and goes active when no valid ATM cells are found in seven consecutive cell slots.
LOF	133	O	Loss of frame. LOF goes active when the framing circuit is unable to find two consecutive SONET frames for 3 ms. The alarm is cleared when eight consecutive error-free SONET frames are identified.
LOP	121	O	Loss of incoming pointer. LOP goes active to indicate that an invalid pointer was found in the H1, H2 pointer bytes of the incoming frame. LOP also goes active when a new data flag (NDF) is detected for eight consecutive frames. The LOP alarm deactivates when a valid pointer with a normal NDF is detected in three consecutive frames.
LOS	128	O	Loss of signal. LOS goes active when no signal transitions are detected on the incoming serial signal for 3.3 µs. The alarm is cleared when two consecutive valid SONET framing patterns are detected and no transitionless 3.3-µs period is detected.
OOF	129	O	Out of frame. OOF goes active when four consecutive errored SONET frames are received. The alarm clears when two consecutive error-free SONET frames are identified.
LOSRD	116	O	Loss of receive data. LOSRD goes active when the receive output FIFO overflows. The receive output FIFO can store a maximum of three complete ATM cells. If a cell is not sent to the next device before a fourth cell arrives, the newest cell is discarded to make room in the FIFO for the next arriving cell.

Terminal Functions (continued)

control signals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CKGENBP	136	I (TTL)	Clock-generation phase-locked loop bypass. When CKGENBP is high, the clock-generation PLL is bypassed and the high-speed clock input (TXHCKT/ TXHCKC) is used for the transmit clock. When CKGENBP is low, the 19.44-MHz TXREFCK is used to generate the transmit clock.
CKRECBP	135	I (TTL)	Clock-recovery phase-locked loop bypass. When CKRECBP is high, the clock-recovery PLL is bypassed. RSCT/RSCC is used to clock RSDT/RSDC into the device.
CLKLOOP	134	I (TTL)	Receive clock loop. When CLKLOOP is high and CKGENBP is low, the receive-serial clock is looped to the transmit side and used for the transmit-serial clock. The received clock is either the clock recovered from the incoming data stream or RSCT/RSCC as determined by the state of CKRECBP.
FLB	138	I (TTL)	Facility loopback. When FLB is high, the receive-serial data and clock is looped to the transmit-serial clock and data output. The receive-serial clock is either the clock recovered from the incoming data stream or RSCT/RSCC as determined by the state of CKRECBP.
OE	58	I (TTL)	Output enable. When OE is low, all outputs on the TNETA1500A, except for the high-speed PECL outputs, are placed in the high-impedance state. This feature facilitates board-level testing. OE contains an internal pullup resistor so that it can be left open for normal operation.
RESET	142	I (TTL)	Device reset. When RESET goes high, the device is reset. Reset causes the receive side to restart the frame-search algorithm and forces OOF, LOF, and LOCA high. RESET also flushes any ATM cells stored in the input and output FIFOs and causes the transmit side to begin building SONET frames from the A1 byte. The RESET pulse is high for a minimum of 51 ns to reset the TNETA1500A.
SDHENABLE	57	I (TTL)	SDH enable. When SDHENABLE is high, the frame transmitted by the TNETA1500A has the 3 C1 bytes set to the sequence 01 00 00 (hex). In addition, the 3 H1 bytes in the transmit frame set to the values 6A, 9B, 9B (hex). When SDHENABLE is low, the transmit C1 bytes are set to the sequence 01 02 03 (hex) and the H1 bytes are set to the values 62, 93, 93 (hex). These conditions are necessary to comprehend the differences between a SONET STS-3c frame and an SDH STM-1 frame. SDHENABLE has an internal pulldown resistor so that it can be left open for SONET operation.
TLB	137	I (TTL)	Terminal loopback. When TLB is taken high, the data received at the transmit-cell interface is looped through the device and out the receive-cell interface. Data appearing at the receive serial data input is blocked in this mode.
TXREFCK	48	I (TTL)	Transmit-reference clock. TXREFCK is used to provide a 19.44-MHz reference clock to the clock-generation PLL when CKGENBP and CLKLOOP are low. The clock-generation PLL multiplies this clock by eight to generate the 155.52-MHz transmit-serial clock.

Terminal Functions (continued)

receive-cell interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RCKI	120	I (TTL)	Receive clock input. Output signals are clocked out of the receive-cell interface on positive transitions of RCKI when $\overline{\text{RRE}}$ is low.
RD0–RD7	92–95 98–101	O	Receive byte data. The ATM cells are clocked out of the TNETA1500A through RD0 – RD 7 one byte at a time on positive transitions of RCKI, which begins with the first byte of the ATM-cell header.
$\overline{\text{RRE}}$	119	I (TTL)	Receive read enable. A low level on $\overline{\text{RRE}}$ enables the reading of data from the receive-cell interface.
RXCELL	117	O	Receive ATM-cell indicator. RXCELL goes high to identify the first byte (start) of an ATM cell. RXCELL is low during the remainder of the output.
$\overline{\text{RXFE}}$	118	O	Receive FIFO empty. $\overline{\text{RXFE}}$ goes low to denote that the receive FIFO is empty and that the current output byte is not a valid byte. $\overline{\text{RXFE}}$ goes high when a complete ATM cell is available for output.

transmit-cell interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TCKI	65	I (TTL)	Transmit clock input. Input signals are clocked into the transmit-cell interface and output signals are clocked out of the transmit-cell interface on positive transitions of TCKI when $\overline{\text{TWE}}$ is low.
TD0–TD7	68–71 74–77	I (TTL)	Transmit byte data. The ATM cells are clocked into the transmit-cell interface one byte at a time on positive transitions of TCKI when $\overline{\text{TWE}}$ is low.
$\overline{\text{TWE}}$	64	I (TTL)	Transmit write enable. A low level on $\overline{\text{TWE}}$ enables the writing of ATM cells into the transmit-cell interface.
$\overline{\text{TXAF}}$	61	O	Transmit FIFO almost full. $\overline{\text{TXAF}}$ goes low when the transmit cell input FIFO can store only five additional input bytes. $\overline{\text{TXAF}}$ goes high when storage is available in the FIFO to store a complete 53-byte ATM cell.
TXCELL	63	I (TTL)	Transmit start-of-cell indicator. A high level on TXCELL identifies the first byte of an incoming ATM cell. TXCELL should be low during the remainder of the cell input.

controller interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
A0–A7	19–26	I (TTL)	Address lines. A0–A7 provide the address for accessing the internal registers. A7 is the most-significant bit.
D0–D7	1–4 7–10	I/O	Data I/O. D0–D7 provide access to the contents of the device's internal registers. D7 is the most-significant bit.
$\overline{\text{INTR}}$	13	O	Interrupt (open drain). $\overline{\text{INTR}}$ goes low to indicate that a nonmasked interrupt has occurred. A read to any of the interrupt registers makes the $\overline{\text{INTR}}$ signal inactive (high).
RD/$\overline{\text{WR}}$	16	I (TTL)	Read/write control. A high-level input on RD/$\overline{\text{WR}}$ indicates a read operation and a low-level input indicates a write operation.
$\overline{\text{READY}}$	14	O	Ready. $\overline{\text{READY}}$ goes low to indicate that the device is ready to complete the requested transaction.
$\overline{\text{SEL}}$	15	I (TTL)	Device select. A low-level input on $\overline{\text{SEL}}$ enables the access of the device's internal registers.

Terminal Functions (continued)

miscellaneous signals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CGCAP	46		Clock-generation loop-filter external capacitor connection. A 0.01-μF capacitor is connected from CGCAP to ground.
CRCAP	37		Clock-recovery loop-filter external capacitor connection. A 330-pF capacitor is connected from CRCAP to ground.
AGND	35, 38, 39, 44, 45, 56		Analog ground. AGND is the 0-V reference connection for APLLs.
AV_{CC}	34, 36, 40, 43, 47, 55		Analog supply voltage. AV_{CC} is the 5 V ±5% connection for APLLs.
NC	27–29, 80–83, 86–89, 104–107, 110–113		No connection. These terminals are left open.
GND	5, 11, 17, 62, 66, 72, 79, 85, 91, 97, 103, 109, 115, 127, 132, 144		Ground. GND is the 0-V reference for digital logic.
V_{CC}	6, 12, 18, 67, 73, 78, 84, 90, 96, 102, 108, 114, 126, 131, 143		Supply voltage. V_{CC} is the 5-V ±5% supply for digital logic.
TEST0–TEST3	59, 60, 139, 140	I	Manufacturing test. TEST0–TEST3 are connected to V_{CC} for normal operation.
TEST4	141	I	Test. TEST4 is tied low for normal operation.
8KHZREF	130	O	8KHZREF produces a pulse that is synchronized to the receive-side framing bytes. 8KHZREF serves as an indication that a frame is being received. When frames are continuously received, 8KHZREF acts like an 8-kHz clock.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1): TTL . . . . . –0.5 V to 7 V
PECL . . . . . –0.5 V to 7 V
Analog supply voltage range, AV_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, V_I: TTL . . . . . –1.2 V to 7 V
PECL . . . . . 0 V to PV_{CC}
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	TTL	4.75	5.25	V
		PECL	4.75	5.25	
AV_{CC}	Supply voltage, analog		4.75	5.25	V
V_{IH}	High-level input voltage	TTL	2		V
		PECL (see Note 2)	V_{CC}–1.1	V_{CC}–0.8	
V_{IL}	Low-level input voltage	TTL		0.8	V
		PECL (see Note 2)	V_{CC}–1.9	V_{CC}–1.5	
T_A	Operating free-air temperature		0	70	°C

NOTE 2: The algebraic convention, in which the least-positive (most-negative) value is designated minimum, is used for logic-level voltages only.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V, I_{IK} = –18 mA			–1.2	V
V_{OH}	High-level output voltage	TTL	V_{CC} = 4.75 V, I_{OH} = –4 mA	4.25			V
		PECL	PV_{CC} = 5 V, I_{OH} = –22.4 mA	4		4.3	
V_{OL}	Low-level output voltage	TTL	V_{CC} = 4.75 V, I_{OL} = 4 mA			0.5	V
		PECL	PV_{CC} = 5 V, I_{OL} = 7.6 mA	3		3.4	
I_I	Input current	TTL	V_{CC} = 5.25 V, V_I = V_{CC} or GND			±300	µA
I_{IH}	High-level input current	All other PECL inputs	V_{CC} = 5.25 V, V_I = 4.45 V			25	µA
		FLAGT, FLAGC, PECL inputs	V_{CC} = 5.25 V, V_I = 4.45 V			250	
I_{IL}	Low-level input current	All other PECL inputs	V_{CC} = 5.25 V, V_I = 3.35 V			±25	µA
		FLAGT, FLAGC, PECL inputs	V_{CC} = 5.25 V, V_I = 3.35 V			–250	
I_{CC1}	Supply current‡		V_{CC} = 5.25 V, I_O = 0, f = 155.52 Mbits/s		150	180	mA
I_{CC2}	Supply current§		V_{CC} = 5.25 V, f = 155.52 Mbits/s		230	255	mA
C_i	Input capacitance	TTL			4		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ PECL outputs are unterminated.
§ PECL outputs are terminated with a 50-Ω resistor to 3 V.

timing requirements (see Figure 1)

NO.			MIN	MAX	UNIT
1	$t_{w(SELL)}$	Pulse duration, $\overline{SEL}$ low	35		ns
2	$t_{su(RD/WR)}$	Setup time, RD/$\overline{WR}$ high before $\overline{SEL}\downarrow$	3		ns
3	$t_{su(A0–A7)}$	Setup time, A0–A7 valid before $\overline{SEL}\downarrow$	0		ns
4	$t_{h(A0–A7)}$	Hold time, A0–A7 valid after $\overline{SEL}\downarrow$	4		ns
5	$t_{h(RD/WR)}$	Hold time, RD/$\overline{WR}$ high after $\overline{SEL}\downarrow$	35		ns

switching characteristics (see Figure 1)

NO.			MIN	MAX	UNIT
6	$t_{d(SL–DV)}$	Delay time, $\overline{SEL}\downarrow$ to D0–D7 valid	7	25	ns
7	$t_{d(SH–DX)}$	Delay time, $\overline{SEL}\uparrow$ to D0–D7 invalid	5	18	ns
8	$t_{d(SL–RL)}$	Delay time, $\overline{SEL}\downarrow$ to $\overline{READY}\downarrow$	7	26	ns
9	$t_{d(SH–RH)}$	Delay time, $\overline{SEL}\uparrow$ to $\overline{READY}\uparrow$	3	15	ns

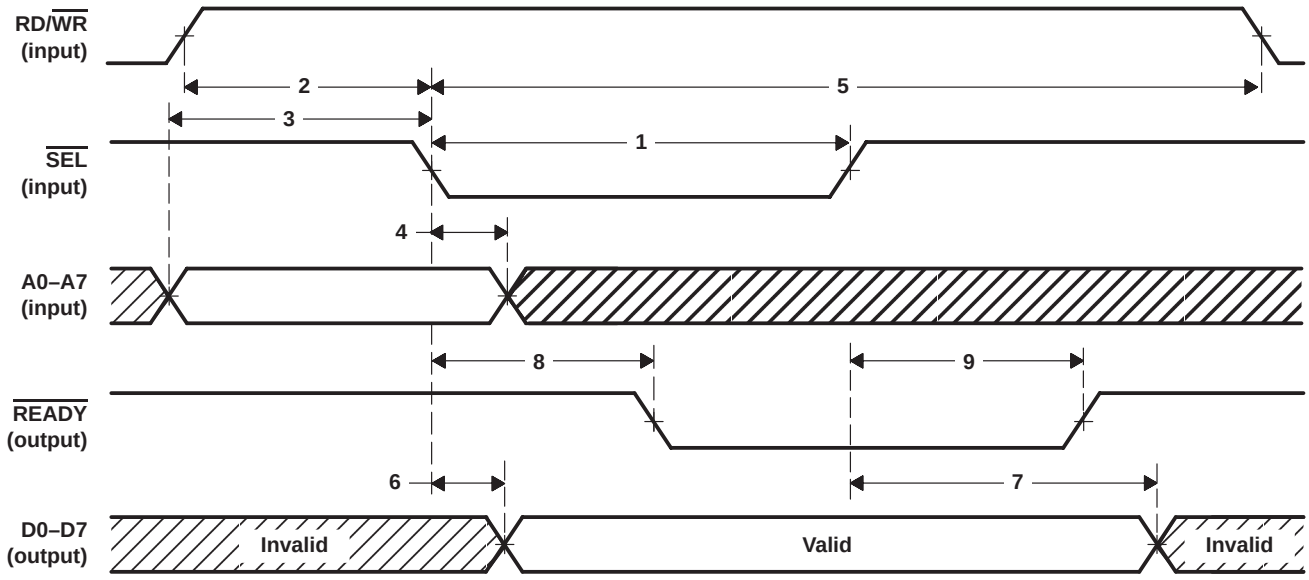


Figure 1. Controller-Interface Read Cycle

timing requirements (see Figure 2)

NO.			MIN	MAX	UNIT
1	$t_{w(SELL)}$	Pulse duration, $\overline{SEL}$ low	35		ns
2	$t_{su(RD/WR)}$	Setup time, RD/$\overline{WR}$ low before $\overline{SEL}\downarrow$	1		ns
3	$t_{su(A0–A7)}$	Setup time, A0–A7 valid before $\overline{SEL}\downarrow$	0		ns
4	$t_{su(D0–D7)}$	Setup time, D0–D7 valid before $\overline{SEL}\uparrow$	5		ns
5	$t_{h(D0–D7)}$	Hold time, D0–D7 valid after $\overline{SEL}\uparrow$	0		ns
6	$t_{h(RD/WR)}$	Hold time, RD/$\overline{WR}$ low after $\overline{SEL}\downarrow$	35		ns

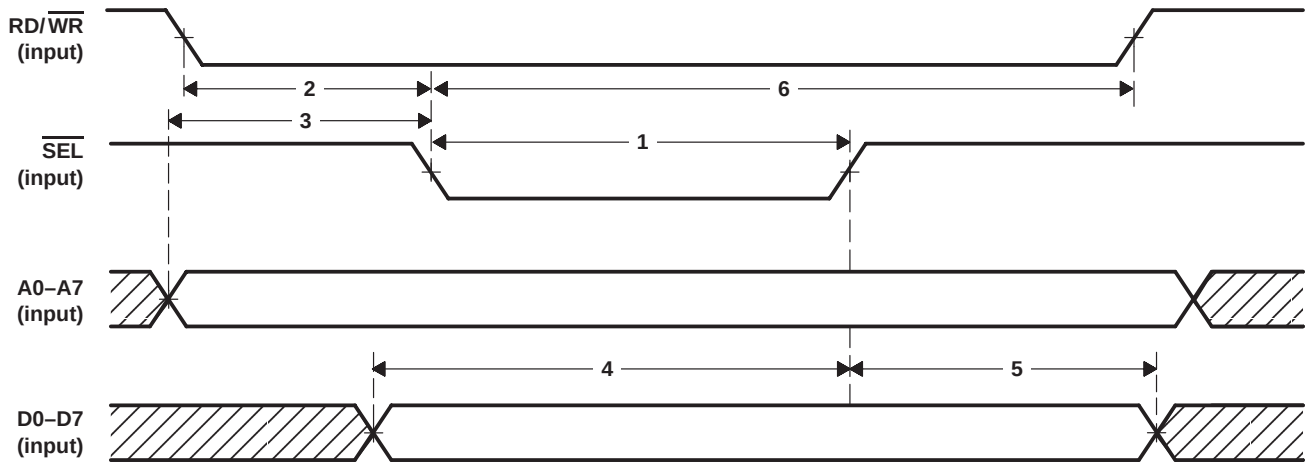


Figure 2. Controller-Interface Write Cycle

timing requirements (see Note 3 and Figure 3)

NO.			MIN	MAX	UNIT
1	$t_{w(RCKIH)}$	Pulse duration, RCKI high	10		ns
2	$t_{w(RCKIL)}$	Pulse duration, RCKI low	10		ns
3	$t_{su(RRE)1}$	Setup time, $\overline{RRE}$ high before RCKI↑	8		ns
4	$t_{su(RRE)2}$	Setup time, $\overline{RRE}$ low before RCKI↑	8		ns
5	$t_{h(RRE)1}$	Hold time, $\overline{RRE}$ high after RCKI↑	0		ns
6	$t_{h(RRE)2}$	Hold time, $\overline{RRE}$ low after RCKI↑	0		ns

NOTE 3: All output signals are generated on the rising edge of RCKI. All input signals are sampled on the rising edge of RCKI.

switching characteristics (see Note 3 and Figure 3)

NO.			MIN	MAX	UNIT
	$f_{max(RCKI)}$	Maximum clock frequency for RCKI	50		MHz
7	$t_{d(RCH–RXCH)}$	Delay time, RCKI↑ to RXCELL↑	5	18	ns
8	$t_{d(RCH–RDV)}$	Delay time, RCKI↑ to RD0–RD7 valid	5	16	ns
9	$t_{d(RCH–RXFH)}$	Delay time, RCKI↑ to $\overline{RXFE}$↑	4	12	ns
10†	$t_{d(RCH–RXFL)}$	Delay time, RCKI↑ to $\overline{RXFE}$↓	5	11	ns
11	$t_{d(RCKI–RXCH)}$	Delay time, RCKI↑ to $\overline{RXCELL}$↓	5	18	ns

† $\overline{RXFE}$ goes active low when no complete cell is available in the receive cell FIFO. When a complete cell is available, $\overline{RXFE}$ is deactivated. The pulse duration of this signal depends on the pulse duration of the RCKI clock and on the cell availability of the FIFO. The minimum pulse duration is equal to the RCKI width. The maximum width is dependent on the RCKI clock pulse duration and cell availability.

NOTE 3: All output signals are generated on the rising edge of RCKI. All input signals are sampled on the rising edge of RCKI.

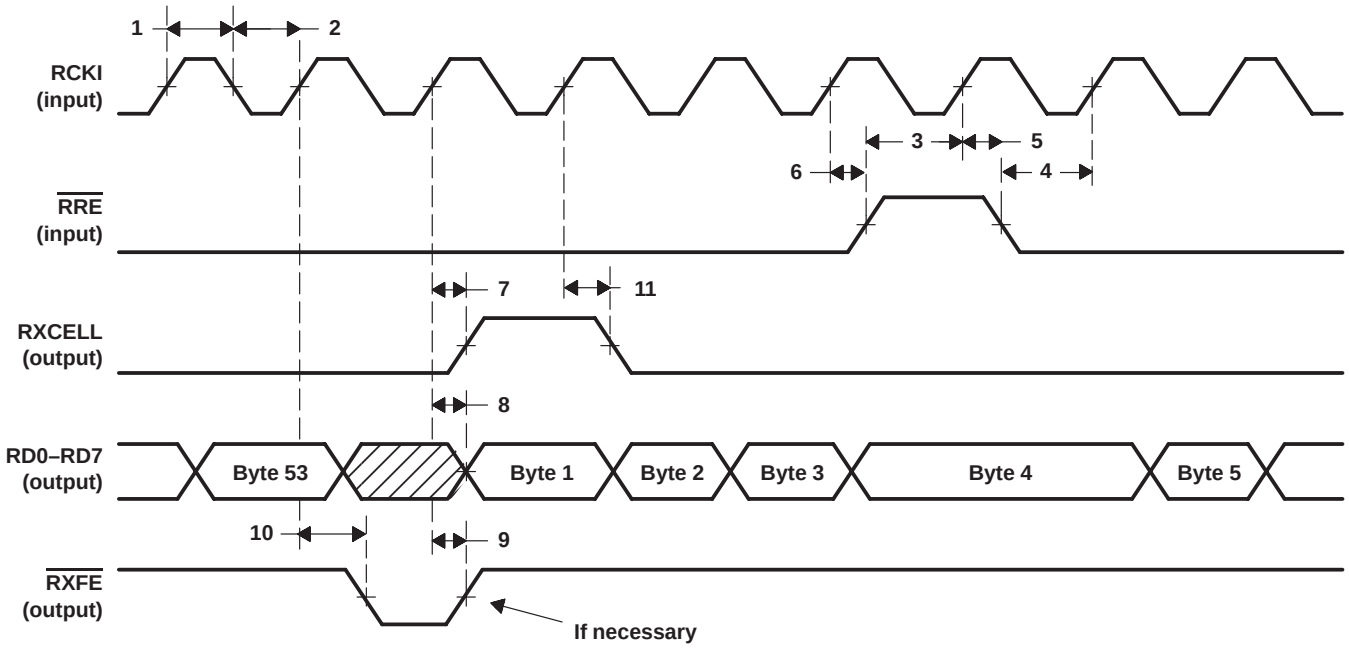


Figure 3. Receive-Cell Interface

timing requirements (see Note 4 and Figure 4)

NO.			MIN	MAX	UNIT
1	$t_{w(TCKIH)}$	Pulse duration, TCKI high	10		ns
2	$t_{w(TCKIL)}$	Pulse duration, TCKI low	10		ns
3	$t_{su(TWE)1}$	Setup time, $\overline{TWE}$ high before TCKI↑	12		ns
4	$t_{su(TXCELL)1}$	Setup time, TXCELL high before TCKI↑	12		ns
5	$t_{su(TD0–TD7)}$	Setup time, TD0–TD7 valid before TCKI↑	12		ns
6	$t_{su(TWE)2}$	Setup time, TWE low before TCKI↑	12		ns
7	$t_{su(TXCELL)2}$	Setup time TXCELL low before TCKI↑	12		ns
8	$t_{h(TWE)1}$	Hold time, $\overline{TWE}$ high after TCKI↑	0		ns
9	$t_{h(TXCELL)1}$	Hold time, TXCELL high after TCKI↑	0		ns
10	$t_{h(TD0–TD7)}$	Hold time, TD0–TD7 valid after TCKI↑	0		ns
11	$t_{h(TWE)2}$	Hold time, TWE low after TCKI↑	0		ns
12	$t_{h(TXCELL)2}$	Hold time, TXCELL low after TCKI↑	0		ns

NOTE 4: All output signals are generated on the rising edge of TCKI. All input signals are sampled on the rising edge of TCKI.

switching characteristics (see Note 4 and Figure 4)

NO.			MIN	MAX	UNIT
	$f_{max(TCKI)}$	Maximum clock frequency for TCKI	50		MHz
13	$t_{d(TCH–TXAF)}$	Delay time, TCKI↑ to $\overline{TXAF}$↓	4	12	ns
14	$t_{d(TCKI–TXAF)}$	Delay time, TCKI↑ to $\overline{TXAF}$↑	4	12	ns

NOTE 4: All output signals are generated on the rising edge of TCKI. All input signals are sampled on the rising edge of TCKI.

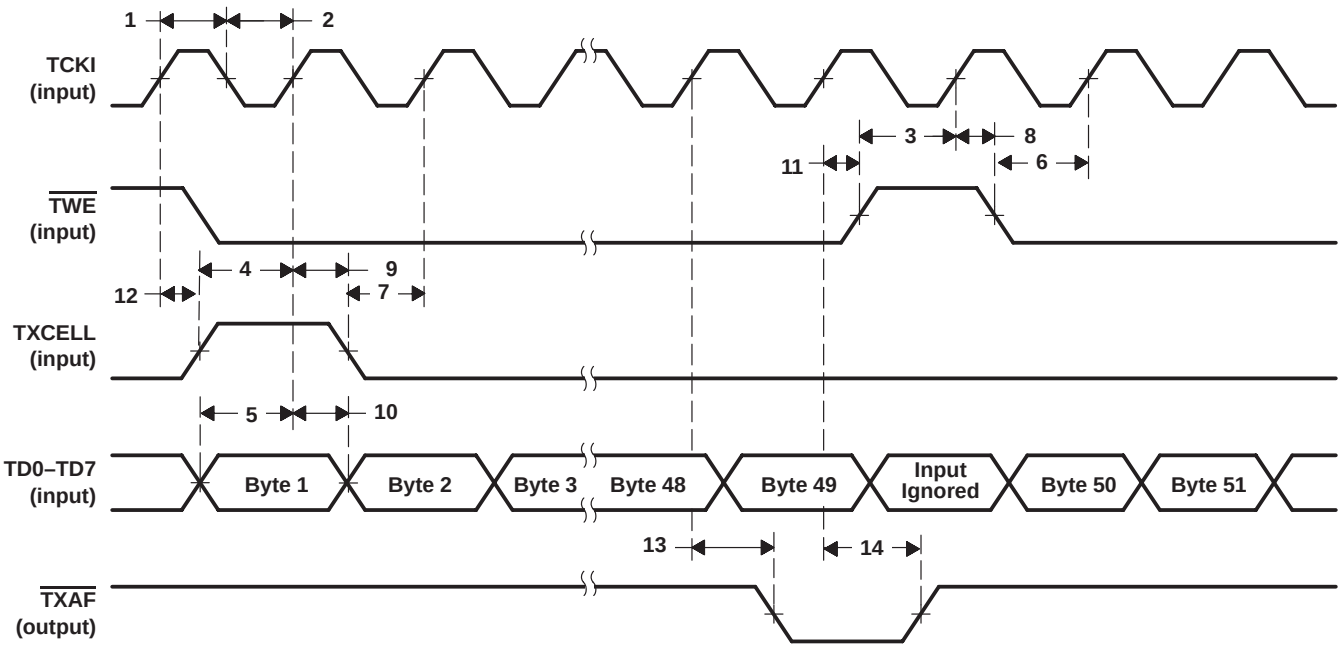


Figure 4. Transmit-Cell Interface

switching characteristics (see Figure 5)

NO.		MIN	MAX	UNIT
1	$t_{w(8KHZREFL)}$ Pulse duration, 8KHZREF low	22	27	ns

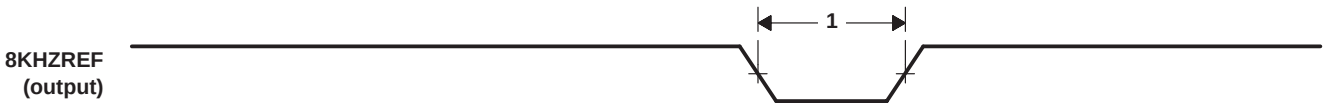


Figure 5. 8-kHz Reference Signal

APPLICATION INFORMATION

introduction

The TNETA1500A SONET/SDH ATM receiver/transmitter is designed to insert/extract ATM cells into/from a 155.52-Mbit/s STS-3c/STM-1 frame. The device contains two APLLs and the digital logic necessary to process the incoming frame and build the output frame. The two APLLs are used to:

- Recover a 155.52-MHz receive clock from the incoming serial-data stream
- Generate a 155.52-MHz transmit clock from an external 19.44-MHz signal

The device is fabricated from a 0.8-μm BiCMOS process. The BiCMOS process provides the capability of designing true differential PECL (ECL referenced to 5 V instead of ground) serial inputs and outputs. The advantages of providing true PECL inputs and outputs are:

- The device interfaces directly to fiber-optic receivers and transmitters and UTP-5 transceivers without external buffering.
- The device outputs can directly drive a 50-Ω line terminated with 50 Ω to 3 V or the Thevenin equivalent (121 Ω to ground and 82 Ω to V_{CC}). This eliminates transmission-line reflections and improves performance.
- The differential PECL inputs provide a high common-mode noise-rejection ratio (CMRR), which improves noise immunity of the device.
- The reduced output voltage swing of the differential PECL outputs (approximately 800 mV) reduces the internal noise generated when the high-speed serial outputs switch. This is especially important since the outputs are switching at 155.52 Mbits/s.

Internally, the two APLLs are isolated from each other and the digital logic blocks (see Figure 6). Each APLL has its own V_{CC} and ground connections that are not connected internally to the V_{CC} and ground connections of the other blocks. From a power and ground connection viewpoint, this forms three blocks: the digital logic block, the analog clock-recovery block, and the analog clock-generation block.

APPLICATION INFORMATION

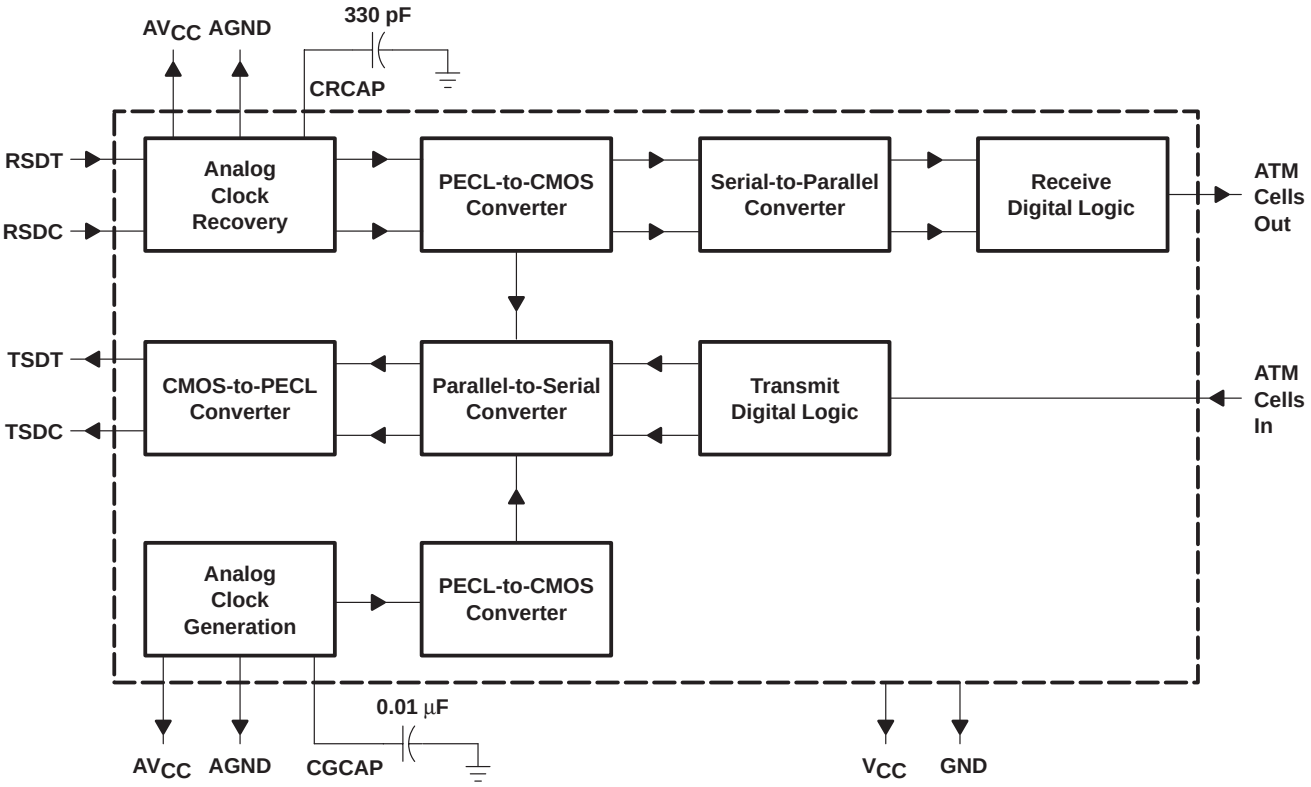


Figure 6. Analog and Digital Blocks in the TNETA1500A

APPLICATION INFORMATION

general layout considerations for the TNETA1500A

The major considerations in laying out a board for the TNETA1500A are:

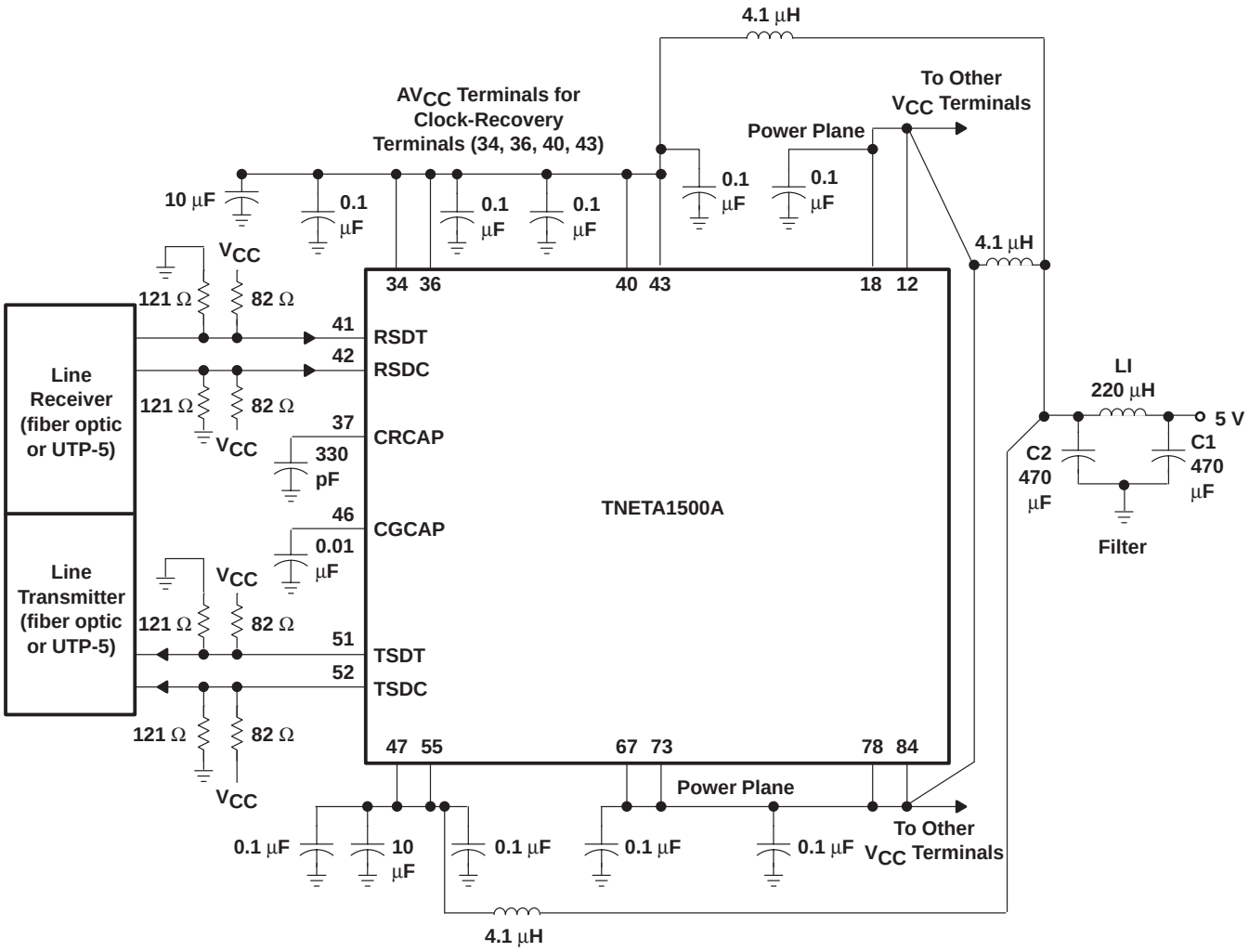
- Decouple the analog power supply (AV_{CC} terminals) from the digital power supply (V_{CC} terminals) using an inductor or ferrite bead. For example:
  - Connect the AV_{CC} terminals for the clock-recovery block together and use an inductor/ferrite bead to connect them through inductor LI to 5 V. Then, connect the AV_{CC} terminals for the clock-generation block together and use a second inductor/ferrite bead to connect these terminals through inductor LI to 5 V.
- Use low-inductance bypass capacitors, such as 0.1-μF surface-mount devices, to reduce V_{CC} noise due to output switching. The recommended bypassing is one bypass capacitor for each AV_{CC} terminal and one bypass capacitor for each two V_{CC} terminals. For more filtering, an additional 10-μF surface-mount capacitor is recommended between each analog section and ground.
- The TNETA1500A supply should be filtered from the main power supply. This can be accomplished with a pi filter consisting of two 470-μF capacitors and a 220-μH inductor. To maintain a small voltage drop across the inductor, the inductor should have a low dc resistance. A voltage regulator can be used if a higher voltage (> 5 V) is available.
- There are many ways to physically lay out the planes that are described. One method is to cut each isolated AV_{CC} plane out of the V_{CC} plane. These isolated planes are placed directly under the associated portions of the device for easy connection to the pins. The ground plane can remain solid, with no cutouts under the isolated V_{CC} planes.

The PECL inputs to the device are terminated using a split-resistor termination of 121 Ω to ground and 82 Ω to V_{CC}. Placing the termination resistors close to the input terminals reduces the possibility of signal reflections and maintains the integrity of the signal waveform. The PECL outputs also are terminated using a split-resistor termination of 121 Ω to ground and 82 Ω to V_{CC}. The termination resistors should be placed as close as possible to the input terminals of the device that the TNETA1500A is driving to prevent reflections and maintain signal integrity.

External capacitors connected to terminals CGCAP and CRCAP must be connected to the APLLs to provide the loop-filter capacitance. One capacitor is required for each APLL. The recommended values of the capacitors connected to CRCAP and CGCAP terminals are 330 pF and 0.01 μF, respectively.

Figure 7 shows a typical connection between the TNETA1500A and fiber-optic or UTP-5 transceiver with PECL inputs and outputs. In this diagram, the AV_{CC} terminals are broken out between the analog clock-recovery block and the analog clock-generation block.

APPLICATION INFORMATION



NOTES: A. If TXHCKT, TXHCKC, RSCT, and RSCC are not used, they should be terminated as follows:
TXHCKT (terminal 49) – 1-kΩ resistor to V_{CC}
TSHCKC (terminal 50) – 1-kΩ resistor to GND
RSCT (terminal 32) – 1-kΩ resistor to V_{CC}
RSCC (terminal 33) – 1-kΩ resistor to GND

B. FLAGT and FLAGC contain internal pullup/pulldown resistors and can be left open.

C. All AGND and GND terminals are connected to the same ground plane.

D. It is recommended that one 0.1-µF capacitor be used for each two V_{CC} terminals (digital-power terminals).

E. Ferrite beads can be used in place of the 4.1-µH inductors. The following are part numbers of beads from Fair-Rite Corporation that can be used. Other beads from other manufacturers may work as well:
Surface-mount ferrite beads:
Fair-Rite P/N 2743021447 (long bead)
Fair-Rite P/N 2743019447 (short bead)
Leaded ferrite bead:
Fair-Rite P/N 2743002111

F. Inductor LI – Toko 622LY–221K (Toko 822LY–221K)

G. Capacitors C1 and C2 – Panasonic ECE–A1AFS471 (radial) and Panasonic ECE–V1AA471 (surface mount)

Figure 7. Board Layout for the TNETA1500A

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.