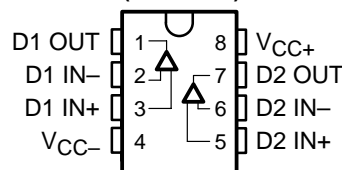


# THS6092, THS6093 275 mA, +12 V ADSL CPE LINE DRIVERS

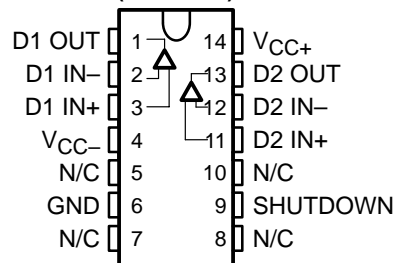
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- **Remote Terminal ADSL Line Driver**
  - Ideal for Both Full Rate ADSL and G.Lite
  - Compatible With 1:2 Transformer Ratio
- **Wide Supply Voltage Range +5 V to +14 V**
  - Ideal for Single Supply +12-V Operation
- **Low 2.1 pA/√Hz Noninverting Current Noise**
  - Reduces Noise Feedback Through Hybrid Into Downstream Channel
- **Wide Output Swing**
  - 18.4 Vpp Differential Output Voltage,  $R_L = 50 \Omega$ , 12-V Single Supply
- **High Output Current**
  - 275 mA (typ)
- **High Speed**
  - 100 MHz (–3 dB,  $G=1$ , 12-V Single Supply)
  - 600 V/μs Slew Rate ( $G = 4$ , 12-V Single Supply)
- **Low Distortion, Single-Ended,  $G = 4$** 
  - –72 dBc (250 kHz, 2 Vpp, 25 Ω load)
  - –78 dBc (250 kHz, 2 Vpp, 100 Ω load)
- **Low Power Shutdown (THS6093)**
  - 300 μA Total Standby Current
- **Thermal Shutdown and Short Circuit Protection**
- **Standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD™ Package**
- **Evaluation Module Available**

THS6092  
SOIC (D) AND  
SOIC PowerPAD™ (DDA) PACKAGE  
(TOP VIEW)

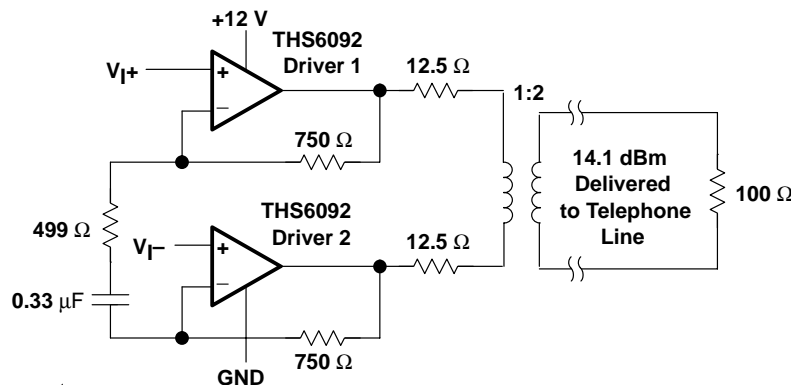


THS6093  
SOIC (D) AND  
TSSOP PowerPAD™ (PWP) PACKAGE  
(TOP VIEW)



## description

The THS6092/3 is a high-speed line driver ideal for driving signals from the remote terminal to the central office in asymmetrical digital subscriber line (ADSL) applications. It can operate from a single +12-V supply voltage while drawing only 7.3 mA of supply current per channel. It offers low –72 dBc total harmonic distortion driving a 25-Ω load (2 Vpp). The THS6092/3 offers a high 18.4-Vpp differential output swing across a 50-Ω load from a single +12-V supply. The THS6093 features a low-power shutdown mode, consuming only 300 μA quiescent current per channel. The THS6092/3 is packaged in a standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD™ package.



## RELATED PRODUCTS

DEVICE	DESCRIPTION
THS6042/3	350-mA, ±12 ADSL CPE line driver
THS6052/3	175-mA, ±12 V ADSL CPE line driver
OPA2677	380-mA, +12 V ADSL CPE line driver
THS6062	Low noise ADSL receiver



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PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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# THS6092, THS6093

## 275 mA, +12 V ADSL CPE LINE DRIVERS

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### AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGED DEVICE				EVALUATION MODULES
	SOIC-8† (D)	SOIC-8† PowerPAD (DDA)	SOIC-14† (D)	TSSOP-14† PowerPAD (PWP)	
0°C to 70°C	THS6092CD	THS6092CDDA	THS6093CD	THS6093CPWP	THS6092EVM THS6093EVM
–40°C to 85°C	THS6092ID	THS6092IDDA	THS6093ID	THS6093IPWP	—

† All packages are available taped and reeled. Add an R-suffix to the device type (i.e., THS6092IDR).

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V <sub>CC+</sub> to V <sub>CC–</sub>	14.7 V
Input voltage	± V <sub>CC</sub>
Output current (see Note 1)	350 mA
Differential input voltage	± 3 V
Maximum junction temperature	150°C
Total power dissipation at (or below) 25°C free-air temperature	See Dissipation Ratings Table
Operating free-air temperature, T <sub>A</sub> : Commercial	0°C to 70°C
Industrial	–40°C to 85°C
Storage temperature, T <sub>stg</sub> : Commercial	–65°C to 125°C
Industrial	–65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS6092 and THS6093 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD™ thermally enhanced package.

### DISSIPATION RATING TABLE

PACKAGE	θ <sub>JA</sub>	θ <sub>JC</sub>	T <sub>A</sub> = 25°C§ POWER RATING	T <sub>A</sub> = 70°C§ POWER RATING	T <sub>A</sub> = 85°C§ POWER RATING
D-8	95°C/W‡	38.3°C/W‡	1.1 W	0.63 W	0.47 W
DDA	45.8°C/W	9.2°C/W	2.3 W	1.31 W	0.98 W
D-14	66.6°C/W‡	26.9°C/W‡	1.6 W	0.90 W	0.68 W
PWP	37.5°C/W	1.4°C/W	2.8 W	1.60 W	1.20 W

‡ This data was taken using the JEDEC proposed high-K test PCB. For the JEDEC low-K test PCB, the θ<sub>JA</sub> is 168°C/W for the D–8 package and 122.3°C/W for the D–14 package.

§ Power rating is determined with a junction temperature of 130°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC+</sub> to V <sub>CC–</sub>	Dual supply	±2.5		±7	V
	Single supply	+5		+14	
Operating free-air temperature, T <sub>A</sub>	C-suffix	0		70	°C
	I-suffix	–40		85	



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**electrical characteristics over recommended operating free-air temperature range,  $T_A = 25^\circ\text{C}$ ,  $V_{CC+} = 12\text{ V}$ ,  $V_{CC-} = \text{GND}$ ,  $R_{\text{FEEDBACK}} = 750\ \Omega$ ,  $R_L = 25\ \Omega$  (unless otherwise noted)**

**dynamic performance**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (–3 dB) $G=1$	$V_{CC} = 12\text{ V}$		100		MHz
		$V_{CC} = 5\text{ V}$		90		
SR	Slew rate (see Note 2)	$V_{CC} = 12\text{ V}$		600		V/ $\mu\text{s}$
		$V_{CC} = 5\text{ V}$		400		

NOTE 2: Slew rate is defined from the 25% to the 75% output levels.

**noise/distortion performance**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD	Total harmonic distortion (single-ended configuration)	Gain = 4, $R_L = 25\ \Omega$ , $V_{CC} = 5\text{ V}$ , $f = 250\text{ kHz}$		$V_{O(pp)} = 2\text{ V}$	–70	dBc
		Gain = 4, $R_L = 25\ \Omega$ , $V_{CC} = 12\text{ V}$ , $f = 250\text{ kHz}$		$V_{O(pp)} = 2\text{ V}$	–72	
				$V_{O(pp)} = 7\text{ V}$	–68	
$V_n$	Input voltage noise	$V_{CC} = 12\text{ V}$ , $5\text{ V}$ , $f = 10\text{ kHz}$		2.1		nV/ $\sqrt{\text{Hz}}$
$I_n$	Input current noise	$V_{CC} = 12\text{ V}$ , $5\text{ V}$ , $f = 10\text{ kHz}$		2.1		pA/ $\sqrt{\text{Hz}}$
				10.9		
$X_T$	Crosstalk	$f = 250\text{ kHz}$ , $V_O = 2\text{ Vpp}$ , $G = 4$ , $R_L = 25\ \Omega$		$V_{CC} = 5\text{ V}$	–65	dBc
				$V_{CC} = 12\text{ V}$	–63	

**dc performance**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>OS</sub>	Input offset voltage	V <sub>CC</sub> = 12 V, 5 V	T <sub>A</sub> = 25°C		6	16	mV
			T <sub>A</sub> = full range			21	
	Differential offset voltage		T <sub>A</sub> = 25°C		1	6	
			T <sub>A</sub> = full range			8	
	Offset drift			T <sub>A</sub> = full range		20	
I <sub>IB</sub>	– Input bias current	V <sub>CC</sub> = 12 V, 5 V	T <sub>A</sub> = 25°C		3	10	μA
			T <sub>A</sub> = full range			12	
	+ Input bias current		T <sub>A</sub> = 25°C		1	6	
			T <sub>A</sub> = full range			7	
	Differential input bias current		T <sub>A</sub> = 25°C		3	10	
			T <sub>A</sub> = full range			12	
Z <sub>OL</sub>	Open loop transimpedance	R <sub>L</sub> = 1 kΩ	V <sub>CC</sub> = 12 V, 5 V		0.9		MΩ

# THS6092, THS6093

## 275 mA, +12 V ADSL CPE LINE DRIVERS

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electrical characteristics over recommended operating free-air temperature range,  $T_A = 25^\circ\text{C}$ ,  $V_{CC+} = 12\text{ V}$ ,  $V_{CC-} = \text{GND}$ ,  $R_{\text{FEEDBACK}} = 750\ \Omega$ ,  $R_L = 25\ \Omega$  (unless otherwise noted) (continued)

### input characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{\text{ICR}}$	Input common-mode voltage range	$V_{\text{CC}} = 5\text{ V}$	$T_A = 25^\circ\text{C}$	1.5 to 3.5	1.1 to 3.9		V
			$T_A = \text{full range}$	1.6 to 3.4			
		$V_{\text{CC}} = 12\text{ V}$	$T_A = 25^\circ\text{C}$	2.3 to 9.7	1.8 to 10.2		
			$T_A = \text{full range}$	2.4 to 9.6			
$\text{CMRR}$	Common-mode rejection ratio	$V_{\text{CC}} = 5\text{ V}$	$T_A = 25^\circ\text{C}$	56	63		dB
			$T_A = \text{full range}$	54			
		$V_{\text{CC}} = 12\text{ V}$	$T_A = 25^\circ\text{C}$	50	56		
			$T_A = \text{full range}$	48			
$R_{\text{I}}$	Input resistance	+ Input			1		$\text{M}\Omega$
		–Input			15		$\Omega$
$C_{\text{I}}$	Input capacitance				2		pF

### output characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{\text{O}}$	Output voltage swing	$R_L = 25\ \Omega$	$V_{\text{CC}} = 5\text{ V}$	1.4 to 3.6	1.1 to 3.9		V
			$V_{\text{CC}} = 12\text{ V}$	1.9 to 10.1	1.4 to 10.6		
		$R_L = 100\ \Omega$	$V_{\text{CC}} = 5\text{ V}$	1.3 to 3.7	1.05 to 3.95		
			$V_{\text{CC}} = 12\text{ V}$	1.5 to 10.5	1.1 to 10.9		
$I_{\text{O}}$	Output current	$R_L = 3.6\ \Omega$ , $V_{\text{CC}} = 5\text{ V}$			240		mA
		$R_L = 10\ \Omega$ , $V_{\text{CC}} = 12\text{ V}$		240	275		
$I_{\text{SC}}$	Short-circuit current	$R_L = 0\ \Omega$ , $V_{\text{CC}} = 12\text{ V}$			325		mA
	Output resistance	Open loop			15		$\Omega$

### power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{\text{CC}}$	Operating range	Dual supply		$\pm 2.25$		$\pm 7$	V
		Single supply		4.5		14	
$I_{\text{CC}}$	Quiescent current (each driver)	$V_{\text{CC}} = 5\text{ V}$	$T_A = 25^\circ\text{C}$		6.7	8.8	mA
			$T_A = \text{full range}$			10	
		$V_{\text{CC}} = 12\text{ V}$	$T_A = 25^\circ\text{C}$		7.3	9.5	mA
			$T_A = \text{full range}$			10.5	
$\text{PSRR}$	Power supply rejection ratio	$V_{\text{CC}} = 5\text{ V}$	$T_A = 25^\circ\text{C}$	-54	-58		dB
			$T_A = \text{full range}$	-46	–		
		$V_{\text{CC}} = 12\text{ V}$	$T_A = 25^\circ\text{C}$	-58	-70		
			$T_A = \text{full range}$	-50			



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**electrical characteristics over recommended operating free-air temperature range,  $T_A = 25^\circ\text{C}$ ,  $V_{CC+} = 12\text{ V}$ ,  $V_{CC-} = \text{GND}$ ,  $R_{\text{FEEDBACK}} = 750\ \Omega$ ,  $R_L = 25\ \Omega$  (unless otherwise noted) (continued)**

**shutdown characteristics (THS6093 only)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{IL}}(\text{SHDN})$	Shutdown pin voltage for power up	$V_{\text{CC}} = 12\text{ V}$ , $\text{GND} = 6\text{ V}$ (GND Pin as Reference)			0.8	V
$V_{\text{IH}}(\text{SHDN})$	Shutdown pin voltage for power down	$V_{\text{CC}} = 12\text{ V}$ , $\text{GND} = 6\text{ V}$ (GND Pin as Reference)	2			V
$I_{\text{CC}}(\text{SHDN})$	Total quiescent current when in shutdown state	$V_{\text{SHDN}} = 8\text{ V}$ , $V_{\text{GND}} = 6\text{ V}$ , $V_{\text{CC}} = 12\text{ V}$		0.3	0.7	mA
$t_{\text{DIS}}$	Disable time (see Note 3)	$V_{\text{CC}} = 12\text{ V}$		0.2		$\mu\text{s}$
$t_{\text{EN}}$	Enable time (see Note 3)	$V_{\text{CC}} = 12\text{ V}$		0.5		$\mu\text{s}$
$I_{\text{IL}}(\text{SHDN})$	Shutdown pin input bias current for power up	$V_{\text{SHDN}} = 6\text{ V}$ , $V_{\text{GND}} = 6\text{ V}$ , $V_{\text{CC}} = 12\text{ V}$		40	100	$\mu\text{A}$
$I_{\text{IH}}(\text{SHDN})$	Shutdown pin input bias current for power down	$V_{\text{SHDN}} = 9.3\text{ V}$ , $V_{\text{GND}} = 6\text{ V}$ , $V_{\text{CC}} = 12\text{ V}$		50	100	$\mu\text{A}$

NOTE 3: Disable/enable time is defined as the time from when the shutdown signal is applied to the SHDN pin to when the supply current has reached half of its final value.

# THS6092, THS6093 275 mA, +12 V ADSL CPE LINE DRIVERS

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## APPLICATION INFORMATION

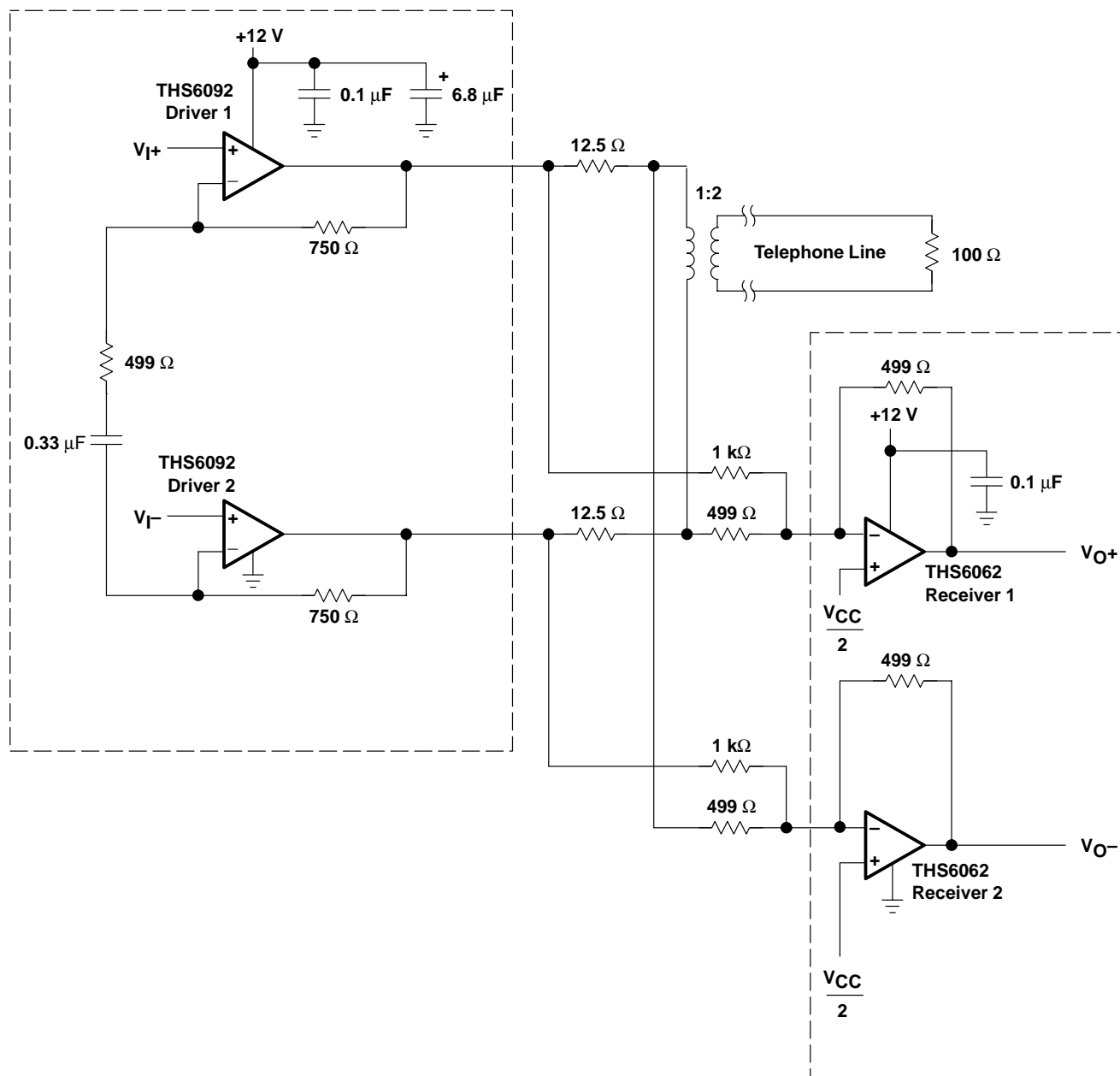


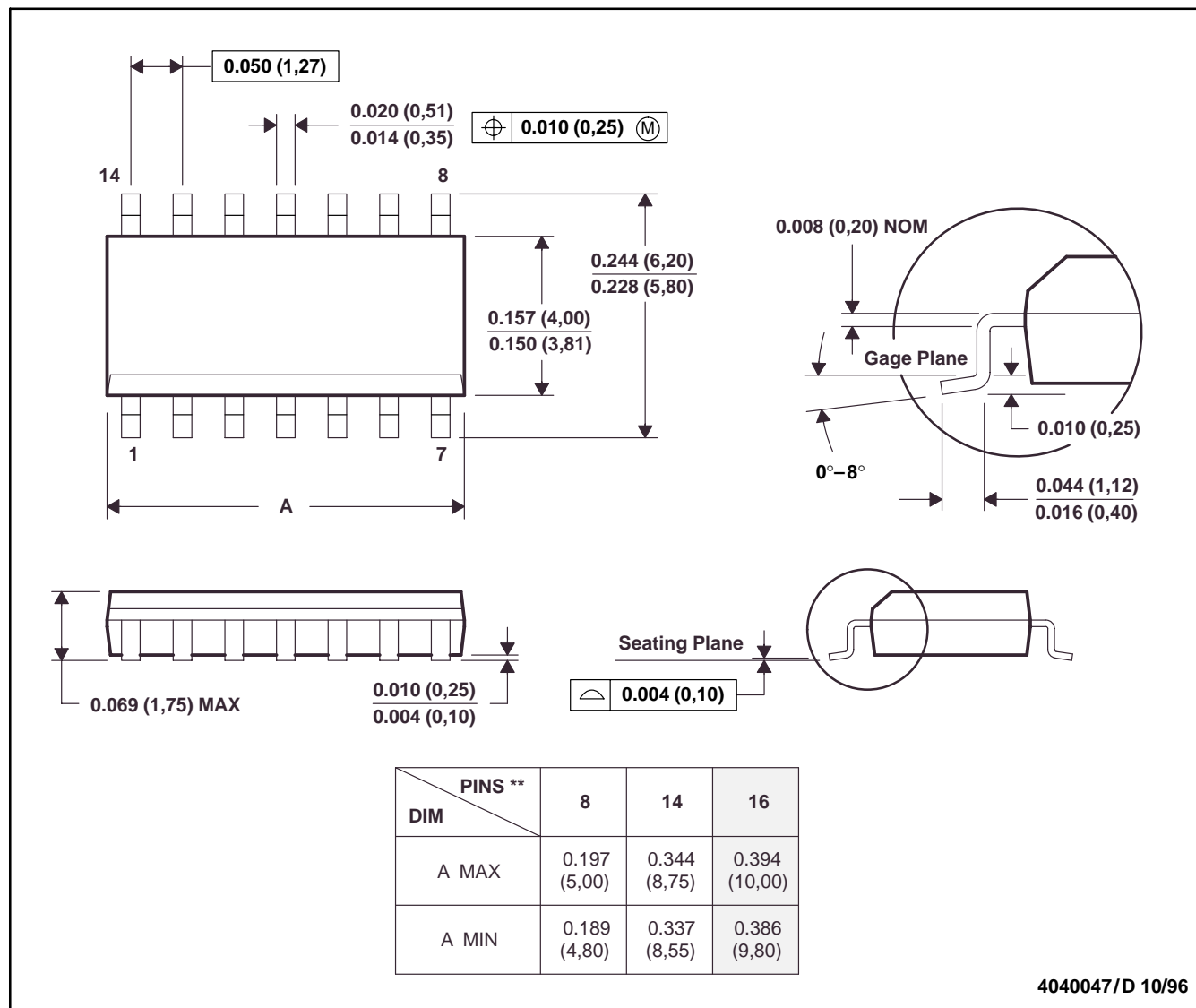
Figure 1. THS6092 ADSL Application With 1:2 Transformer Ratio

# MECHANICAL DATA

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-012

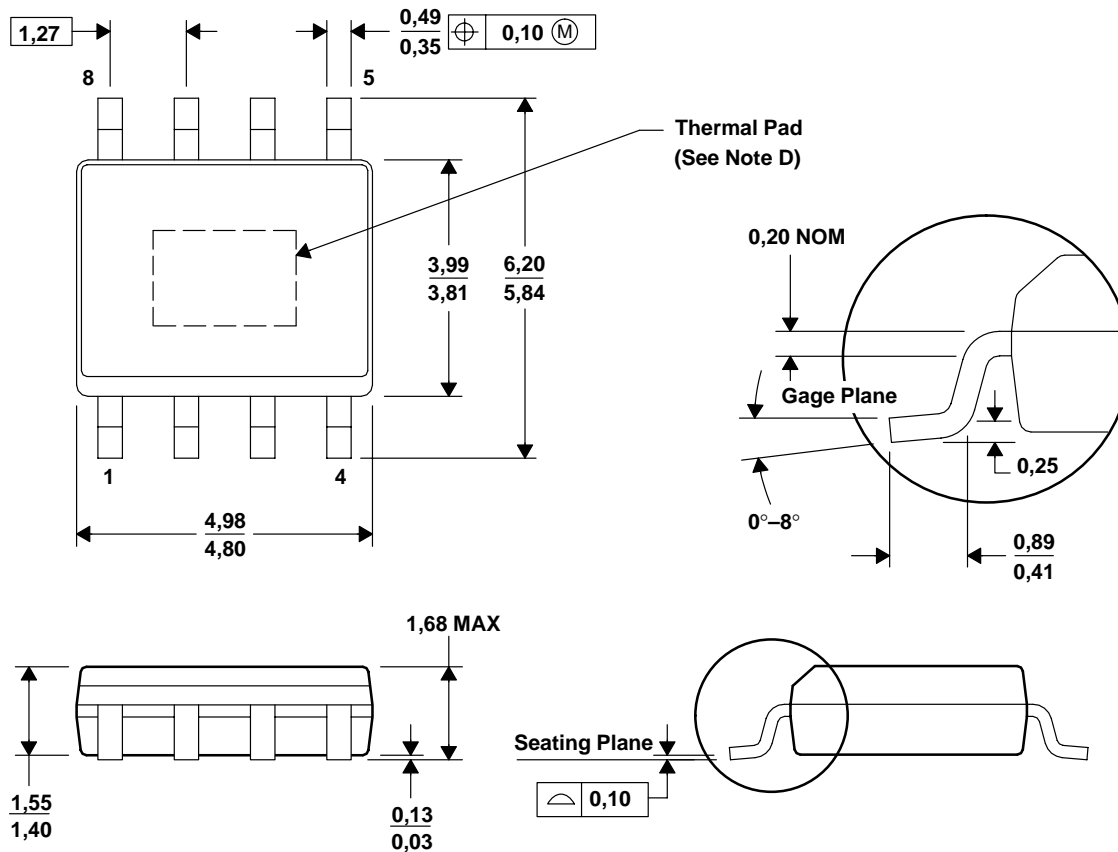
**THS6092, THS6093**  
**275 mA, +12 V ADSL CPE LINE DRIVERS**

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**MECHANICAL DATA**

**DDA (S-PDSO-G8)**

**Power PAD™ PLASTIC SMALL-OUTLINE**



4202561/A 02/01

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.

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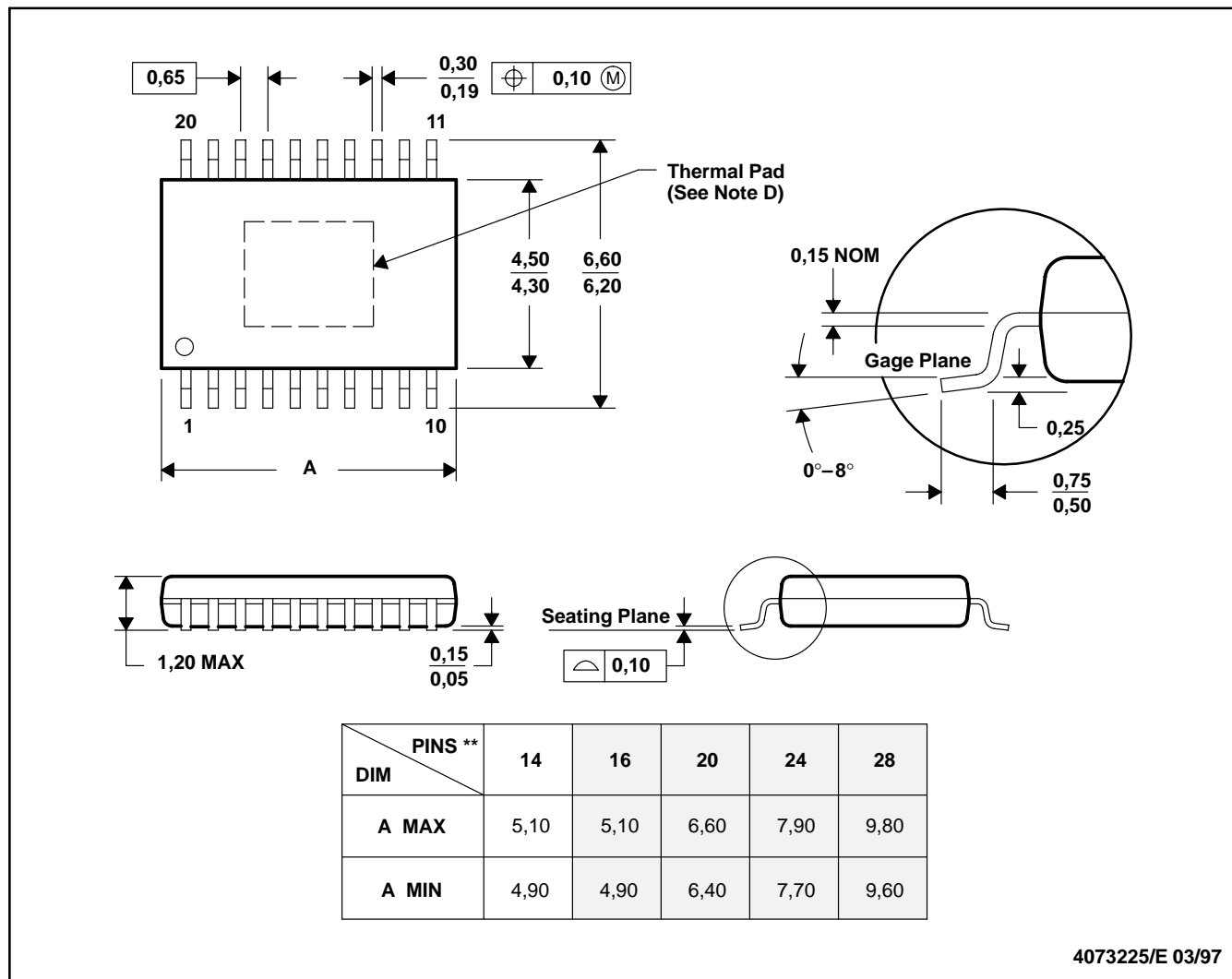


## MECHANICAL INFORMATION

PWP (R-PDSO-G\*\*)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20-PIN SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusions.
  - D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
  - E. Falls within JEDEC MO-153

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