L3M Device
Level 3 Mapper
TXC-03452

DATA SHEET
Product Preview

PRODUCT PREVIEW

FEATURES

- Maps the following line formats into SDH/SONET format:
  - -DS3 to/from STS-3/STS-1 SPE or STS-1 SPE
  - -E3 to/from STM-1/TUG-3
- SDH/SONET bus access:
  - -Drop/add data byte access (with clock, C1J1, SPE, and parity)
  - -Add bus interface timing derived from drop bus, add bus, or external timing
- Path overhead byte processing:
  - -Processor or external interface
  - -B3 generation and detection with test mask
  - -B3 performance counter (16 bit) and block error counter (8 bit)
  - -C2 mismatch and unequipped detection
  - -G1 processing
- Microprocessor access:
  - -Motorola or Intel compatible (pin selectable)
  - -Hardware/software interrupt capability
- Line Interface
  - -Transmit and receive NRZ or rail operation with split operation capability
- Testing functions:
  - -SONET, facility, or line loopback
  - -Transmit and receive 2^{15}-1 or 2^{23}-1 generator & analyzer
  - -Boundary scan capability

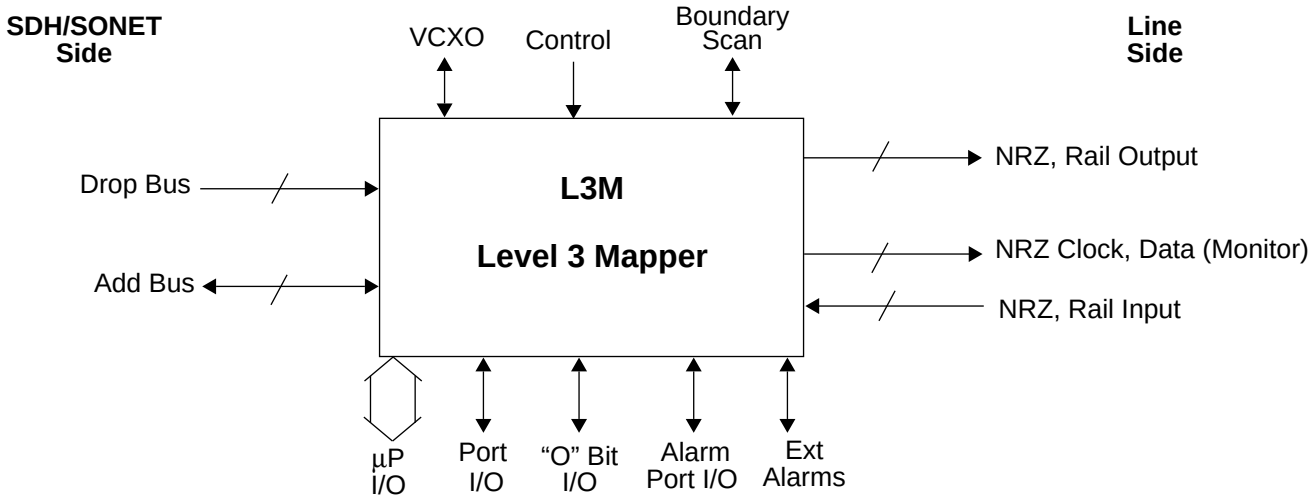
DESCRIPTION

The L3M maps a DS3 or E3 line signal into an STM-1/STS-3/STS-1 formatted signal. The L3M provides a TUG-3 formatted signal for STM-1 operation, or an STS SPE for STS-3 or STS-1 operation. The SDH/SONET signal is transmitted via an add bus with timing derived from the drop side, add side or from external timing (STS-1 only). An option is provided to generate the A1, A2 framing pattern, C1 byte and H1, H2 pointer towards the add bus when external timing mode is selected.

Individual POH bytes for the transmitted SDH/SONET signal are mapped from the L3M memory map or an external interface. An option is provided to generate an unequipped status or TUG-3 path AIS signal. External accesses are provided for the communications channel "O"-bit and alarms for ring operation. The received signal is desynchronized from drop bus STM-1/TUG-3, STS-3/STS SPE, or STS-1 signal. Internal pointer processing is performed for the TUG-3 signal. All POH bytes are provided for the microprocessor.

APPLICATIONS

- Add/drop multiplexers
- Digital cross-connect systems
- Broadband switching systems
- Transmission equipment



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BLOCK DIAGRAM

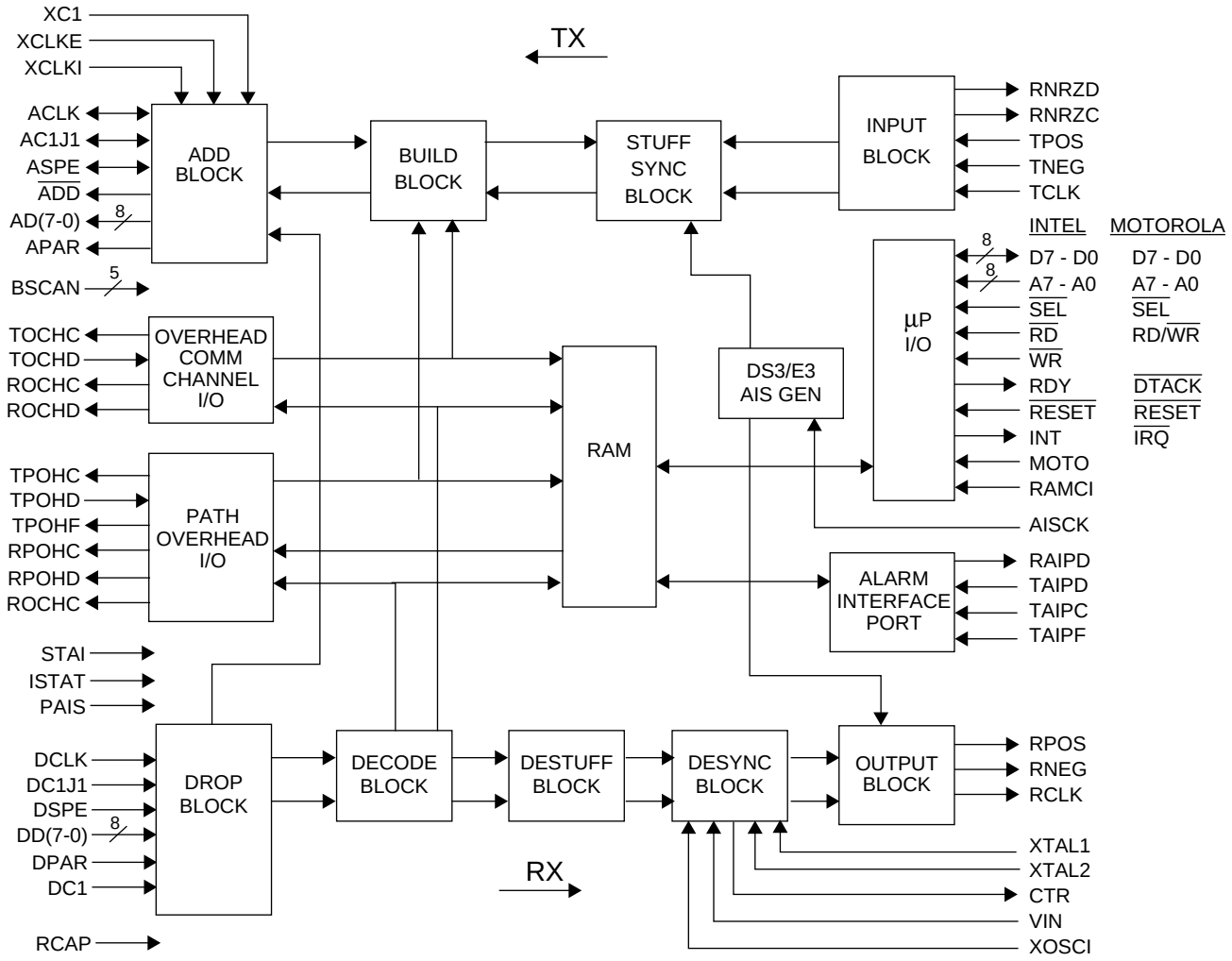


Figure 1. L3M Block Diagram

BLOCK DIAGRAM DESCRIPTION

A simplified block diagram of the L3M is shown in Figure 1. A 44.736 (DS3) or 34.368 (E3) Mbit/s NRZ or a Positive/Negative rail clock and data signal is connected to the Input Block. The transmit line input is independent of the receiver, and consists of positive rail/NRZ signal lead (TPOS), negative rail signal lead (TNEG), and input clock (TCLK). A control bit is provided in software that inverts the clock signal if required. The Input Block performs either a HDB3 or B3ZS decoder function if the input line termination is a rail signal. Separate NRZ data (RNRZD) and clock (RNRZC) signals are provided for external performance monitoring circuits. Illegal coding violations are counted in a 16-bit performance counter. When the line termination is NRZ, the negative rail signal lead (TNEG), can be used to clock illegal coding violations from an external device into the 16-bit performance counter. The transmit signal and clock are both monitored for operation, and alarms reported for failure conditions. Control bits are provided that enable the L3M to send a line AIS when either failure is detected. The Input Block also monitors the line signal for an E3 AIS. The Input block also has a 2^{15}-1 or 2^{23}-1 pseudo-random test generator for testing.

The Stuff/Sync Block and Build Blocks work together for mapping a DS3 or E3 signal into an STS-1 SPE or TUG-3. The mapped formats are shown in Figures 2 and 3. The stuffing algorithm for the DS3 signal format uses one set of five control bits (C-bits) with one stuff opportunity bit (S-bit) for frequency justification, per subframe (9 subframes). The E3 format uses two sets of five control bits (C1, C2 bits) to control two stuff opportunity bits (S1 and S2), per subframe (one subframe per three rows for a total of three subframes per frame). A read clock and timing indications are given by the Build Block for reading the transmit FIFO. A FIFO overflow or underflow alarm indication is provided. Should an underflow/overflow condition occur, the FIFO is immediately reset to the start-up preset value. The transmit FIFO also tracks the incoming line signal that can have an average frequency error as high as +/- 20 ppm, and simultaneously accepts this signal with up to 5 UI Peak-to-Peak jitter (where UI = 1/f).

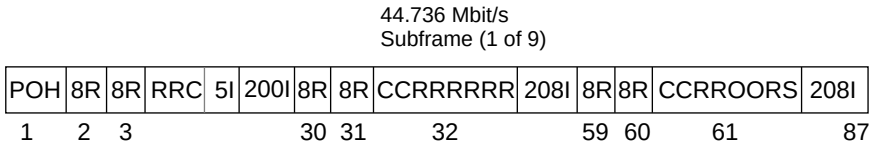


Figure 2. AU-3/STS SPE Build Format

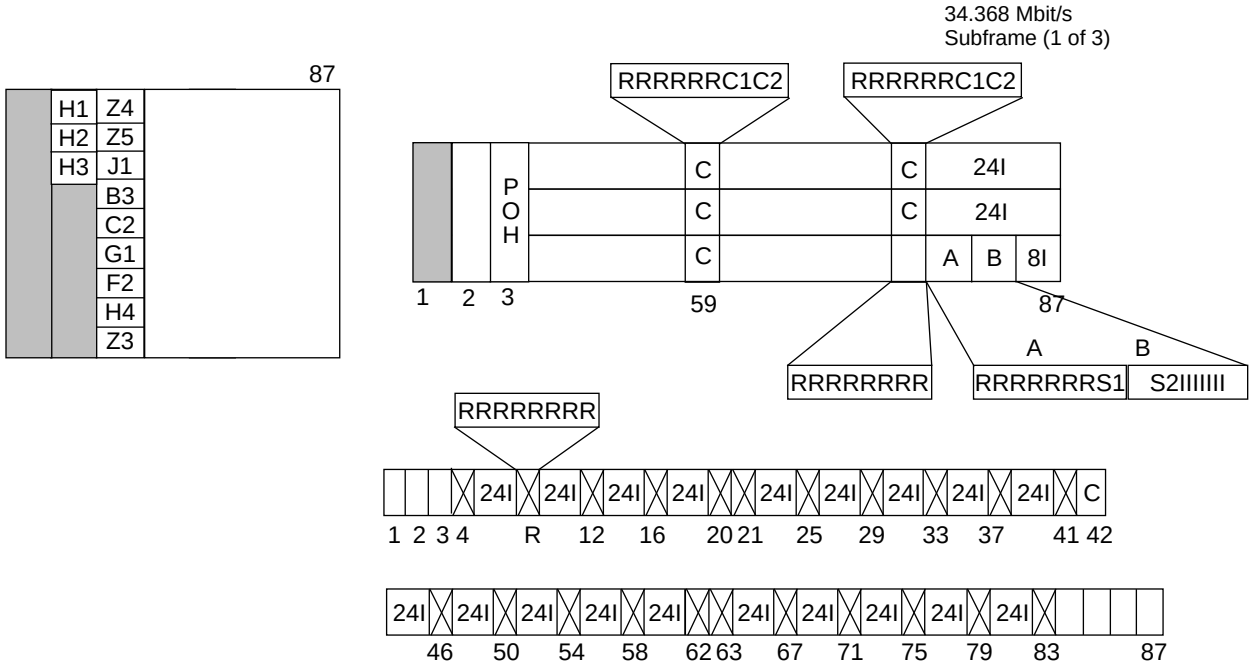


Figure 3. TUG-3 Build Format

The Build Block, with signals exchanged between itself and the Stuff/Sync Block, constructs one of two 87 column by 9 row formats: a CCITT TUG-3 or an STS-1 (for STS-3) signal. A fixed pointer value of 6800H is used when building a CCITT TUG-3 format. Please note that, when the CCITT TUG-3 mode is selected, the pointer value will change when there is a pointer increment or decrement. However, this feature may be disabled. An O-bit serial interface, or two bits in RAM are used for mapping the two "O" bits into the DS3 SONET format subframes. The O-bit interface consists of an output clock (TOCHC) and an input data lead (TOCHD). The

nine Path Overhead bytes are mapped individually into the SONET format from either the POH interface (except the B3 byte), from microprocessor written RAM positions, or from internal logic (such as the path RDI state in bit 5 of G1). The POH interface consists of an output clock (TPOHC), and framing pulse (TPOHF), and an input data lead (TPOHD). A control bit enables the POH interface bytes to be written into RAM when transmitted. Enable bits are provided for controlling the FEBE and path RDI states as a result of local alarms or remote status information received during ring operation. A B3 test mask or fixed byte can also be transmitted. Control bits are provided for generating a TUG-3 path AIS, or an unequipped status condition (payload and POH bytes are equal to zero). An alarm interface provides a FEBE, and path FERF input indication from a mate L3M for ring operation. The alarm interface leads consist of input data (TAIPD), framing pulse (TAIPF), and clock signal (TAIPC).

The Add Block uses an external byte rate clock signal (XCLKI), or the Add or Drop bus clock, SPE and C1J1 timing signals for building and adding a TUG-3, STS-3/STS-1 SPE, or STS-1 SPE to the Add bus. The Add Block supports the STM-1/STS-3 bus signal rate of 19.44 MHz and the STS-1 signal rate of 6.48 MHz. The external clock is enabled by placing a high on the external clock enable lead (XCLKE), and is intended for STS-1 operation. The external clock generates the bus clock (ACLK), C1J1 indication (AC1J1), and SPE indication (ASPE). The output data to the bus is 3-state, active true. A software control bit enables the transport overhead A1, A2, C1, and H1/H2 bytes to be generated. The H1 and H2 bytes will carry the value of 6800 hex and the C1 byte carries the value of 01 hex. An optional C1 signal (XC1 signal lead) can be applied to the L3M to align the start of the frame (A1, A2 bytes).

When add bus timing is selected, the clock (ACLK), C1J1 indication (AC1J1), and SPE indication (ASPE) become input signals from the add bus. When Drop timing is selected, the L3M supports DC1J1 pointer movements on the Drop bus, and adjusts the pointer value in the TUG-3s accordingly. An active low Add indicator is also provided to indicate the location of all time slots that are added to the bus (e.g. TUG-3 A, B or C) by the L3M. The selected clock is monitored for operation, and an odd parity signal (APAR) is calculated for the bus data including the SPE and C1J1 signals when these signals are outputs (e.g. external timing mode).

The Drop Block supports the STM-1/STS-3 bus signaling rate of 19.44 MHz and the STS-1 signal rate of 6.48 MHz. The Drop Block uses the clock (DCLK), C1J1 indication (DC1J1) (and a separate DC1 signal if required), and SPE indication (DSPE) from a Drop bus for determining the location of the Path overhead J1 byte in the VC-4, the three J1 bytes in the three STS-1 SPEs in the STS-3 signal, and the single SPE for STS-1 operation. The C1 pulse is required, and is synchronous with the first C1 byte in the STM-1 Section Overhead bytes, STS-3, or STS-1 Transport Overhead Bytes. The C1 pulse provides a framing indication for determining the location of the E1 byte corresponding to the TUG-3 or STS-1 selected, and is also used by the desynchronizer as a frame reference. The C1 pulse can be present in the DC1J1 signal or provided as a separate signal (DC1). The Drop SPE (DSPE) is active during the POH and payload byte times. The Drop Bus clock, and composite C1J1 signal are monitored for operation, and odd parity calculated and compared against the incoming parity bit.

The Decode Block contains the logic for performing pointer justification for the selected TUG-3 signal, removing the Path Overhead bytes, and Overhead Communication bits, and the detection of the E1 byte for an upstream AIS detection. The E1 byte carries an AIS indication from the SOT-3 or SOT-1 device. The SOT-3 (and SOT-1) generates an AIS signal in each of the three E1 bytes (corresponding to the three STS-1s/TUG-3s) when a loss of frame, loss of pointer, loss of signal, or line AIS detected. This indication is used by L3M to generate a Path RDI indication, and for generating a received DS3 or E3 AIS. In place of the E1 byte AIS, the L3M also supports an alarm indication provided on the ISTAT and PAIS signal leads. The TUG-3 pointer is monitored for loss of pointer, New Data Flag, and Path AIS. Performance counters are provided for monitoring pointer movements. All POH bytes are written into RAM locations and are also provided at the POH interface. The POH interface consists of an output data lead (RPOHD), framing pulse (ROCHF), and clock signal (TPOHC). The L3M also provides a microprocessor written location for performing C2 mismatch detection, and unequipped detection based on ANSI and CCITT standards. The received O-bits are available at an external interface and a 2-bit RAM location updated each frame. The O-bit interface consists of a data lead (ROCHD), and clock signal (ROCHC). An alarm indication port is provided for ring operation. The alarm indication port

consists of a data lead (RAIPD), and the POH interface framing pulse (ROCHF), and clock signal (ROCHC). The signal on the data lead (RAIPD) consists of the FEBE count and a path RDI status indication.

The De-Synchronize Block removes the effect on the output DS3 or E3 signals of systemic jitter due to signal mapping and pointer movements. The output is an average frequency equal to the source frequency, and has jitter characteristics that meet CCITT and ANSI standards. The De-Synchronize Block consists of two circuits, a Pointer Leak Block, and a Digital Phase Locked Loop Block. The function of the Pointer Leak Block is to absorb the immediate effect of up to eight consecutive pointer movements (any combination of SPE or TUG-3 pointer movements) in either direction, and filter them out in time. A single pointer adjustment is an 8 Unit Interval (UI) phase step. The Pointer Leak Block turns the phase step into eight 1 UI steps, widely spaced in time, allowing the Phase Lock Loop block to track. In normal operation, the output is one data bit and one clock cycle for each input bit. When a negative stuff occurs 8 extra bits are pulled from the signal and absorbed. Following this operation, the normal operation of one bit in for one bit out continues except that one extra bit is pulled from the FIFO every n frames. In this way, the pointer step is leaked out in 8 x n frames. The value of n is programmed via the microprocessor.

The output block provides either a positive (RPOS) and negative rail (RNEG) line signal or NRZ signal (RPOS), and a clock signal (RCLK). The HDB3/B3ZS coder operates independent of the transmitter. For interface flexibility, a control bit is provided for inverting the output clock. The receive data and clock outputs can be forced to a high impedance state for the purpose of tying two L3M chips together for ring operation, or redundancy. An additional 2^{15}-1 or 2^{23}-1 pseudo-random test generator is provided. The Output Block and the Input Block share a 2^{15}-1 or 2^{23}-1 analyzer that can compare the desynchronizer output or transmit data against a fixed pattern. An alarm is provided when the analyzer and incoming data are not synchronous. Errors are counted in the 16-bit coding violation counter. Loopbacks between the Input and Output blocks facilitate board and network debugging.

All of the control registers, performance counters, status and alarm indications are accessible through the L3M microprocessor bus interface. The L3M supports both an Intel and Motorola microprocessor bus interface, with both hardware and software interrupt capability. The Motorola compatible microprocessor interface is selected by placing a high on the MOTO signal lead.

PIN DIAGRAM

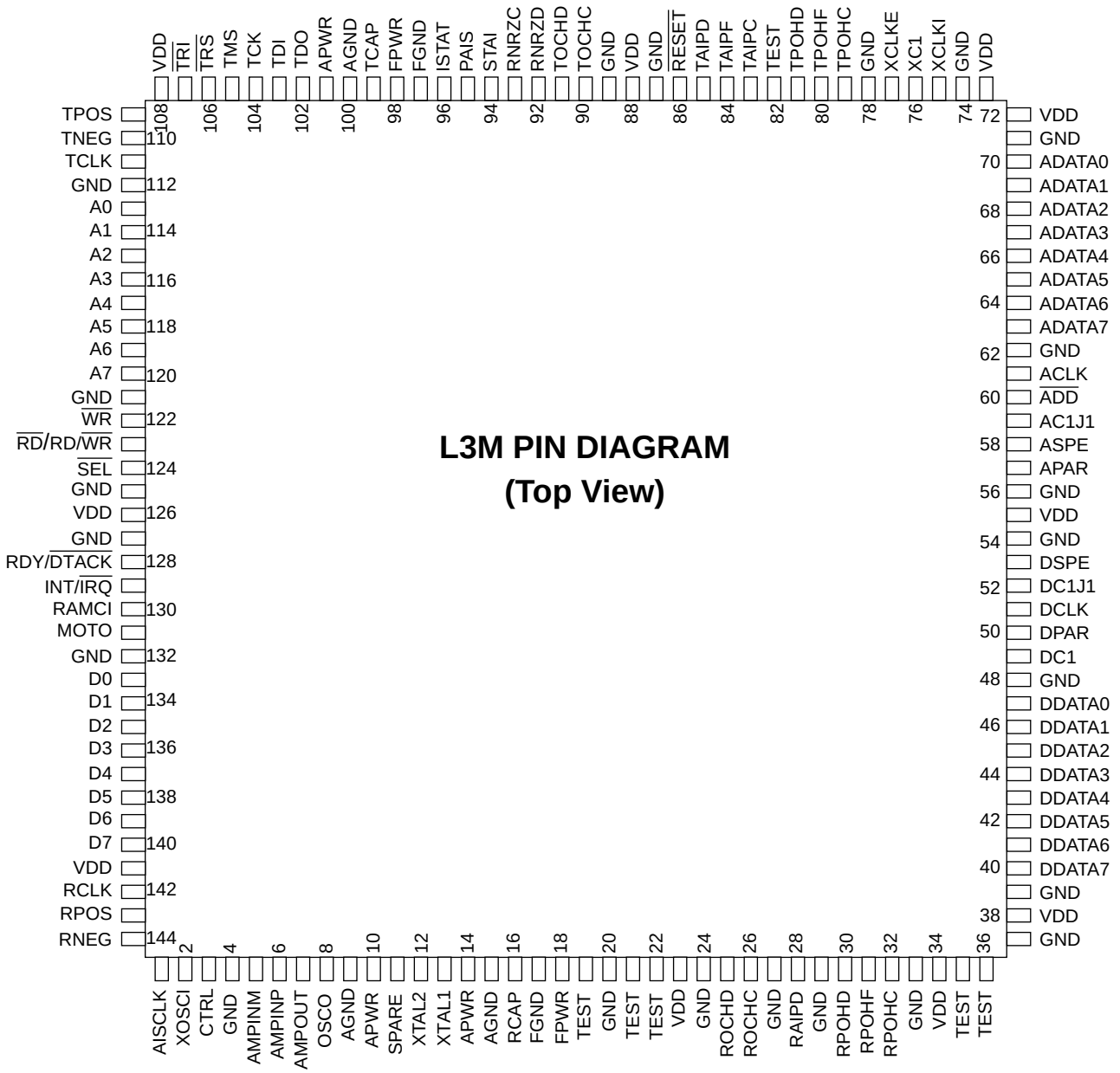


Figure 4. L3M Pin Diagram

PIN DESCRIPTIONS

Power Supply and Ground:

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	23,34,38,55, 72,73,88, 108,126,141	P		**VDD:** +5 volt supply voltage, +/- 5%
GND	4,20,24,27, 29,33,37,39, 48,54,56,62, 71,74,78,87, 89,112,121, 125,127,132	P		**Ground.**
SPARE	11			**Spare:** No connection.

*Note: I = Input; O = Output; P = Power

Line Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
RNRZD	92	O	CMOS4mA	**Receive Line NRZ Data:** Additional output provided for an optional external performance monitoring circuit. This serial encoded NRZ output is provided after the decoder (transmit direction) independent of whether the input is NRZ or rail. Data is clocked out on positive transitions of clock (RNRZC). This lead goes to a high impedance state when control bit L3Z is written with a 1.
RNRZC	93	O	CMOS4mA	**Receive Line Clock:** NRZ data on lead RNRZD is clocked out of the L3M on positive transitions of this clock. This lead goes to a high impedance state when control bit L3Z is written with a 1.
TPOS	109	I	CMOS	**Transmit NRZ Line Data/Positive Rail Data:** Serial NRZ input for the 44.736 or 34.368 Mbit/s asynchronous line data. This lead also provides the positive rail data input for an internal decoder.
TNEG	110	I	CMOS	**Transmit Negative Rail Data:** This lead provides a negative rail input for the internal decoder. In the NRZ mode, this lead can be used as an input for counting the number of coding violations from an external line interface device. The decoder coding violation counter is used. When this pin is not used, it should be grounded.
TCLK	111	I	CMOS	**Transmit Line Clock:** NRZ or rail data is clocked into the L3M using the TPOS/TNEG signal leads on positive transitions of this clock when control bit INVCI is 0. NRZ or rail data is clocked in on negative transitions when control bit INVCI is a 1.

Symbol	Pin No.	I/O/P	Type	Name/Function
RCLK	142	O	CMOS4mA	**Receive Line Clock:** Line data present on the RPOS/RNEG signal leads (44.736 or 34.368 Mbit/s) is clocked out of the L3M on negative transitions of this clock when control bit INVCI is 0. NRZ or rail data is clocked out on positive transitions of this clock when control bit INVCO is written with a 1. This lead goes to a high impedance state when control bit L3Z is equal to 1.
RPOS	143	O	CMOS4mA	**Receive Line NRZ Data/Positive Rail Data:** Serial NRZ output for the 44.736 or 34.368 Mbit/s asynchronous line data. This lead also provides the positive rail output when the rail interface is selected. This lead goes to a high impedance state when control bit L3Z is equal to 1.
RNEG	144	O	CMOS4mA	**Receive Negative Rail Data:** This lead provides a negative rail interface from the internal coder. This lead goes to a high impedance state when control bit L3Z is equal to 1. When the NRZ interface is selected, this lead is unused.

Microprocessor Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
A(7-0)	120 - 113	I	TTL	**Address Bus:** These are active high address line inputs that are used by the microprocessor for accessing an L3M RAM location for a read/write cycle. A0 is the least significant bit.
$\overline{WR}$	122	I	TTL	**Write (I mode):** Intel Mode - An active low signal generated by the microprocessor for writing to the L3M RAM locations. Motorola Mode - Not used.
$\overline{RD}$ RD/$\overline{WR}$	123	I	TTL	**Read (I mode) or Read/Write (M mode):** Intel Mode - An active low signal generated by the microprocessor for reading the L3M RAM locations. Motorola Mode - An active high signal generated by the microprocessor for reading the L3M RAM locations. A low signal is used to write to L3M RAM locations.
$\overline{SEL}$	124	I	TTLp	**Select:** A low enables data transfers between the microprocessor and the L3M during a read/write cycle.
RDY/ $\overline{DTACK}$	128	O 3-state	TTL8mA	**Ready (I mode) or Data Transfer Acknowledge (M mode):** Intel Mode - A high is an acknowledgment from the addressed RAM location that the transfer can be completed. A low shall indicate that the L3M cannot complete the transfer cycle, and microprocessor wait states must be generated. Motorola Mode - During a read bus cycle, a low signal shall indicate the information on the data bus is valid. During a write bus cycle, a low signal acknowledges the acceptance of data.

Symbol	Pin No.	I/O/P	Type	Name/Function
INT/$\overline{IRQ}$	129	O	TTL4mA	**Interrupt:** Intel Mode - A high on this output pin signals an interrupt request to the microprocessor. Motorola Mode - A low on this pin signals an interrupt request for the microprocessor.
RAMCI	130	I	CMOS	**RAM Clock Input:** Clock input for the internal RAM. This clock allows an outside clock to provide an arbitrator function for accessing the internal RAM structure. This clock has an operating rate between 12 and 25 MHz and a duty cycle of +/- 10 percent. This clock and microprocessor timing signals may operate asynchronously with respect to each other.
MOTO	131	I	TTL	**Motorola/Intel Microprocessor Select:** A high selects the Motorola microprocessor compatible bus interface. A low selects the Intel microprocessor compatible bus interface.
D(7-0)	140 - 133	I/O	TTL8mA	**Data Bus:** Bi-directional data lines used for transferring data between the L3M and an external processor. D0 is the least significant bit.

Drop Bus Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
DDATA (7-0)	40 - 47	I	TTL	**Drop Data Byte:** Byte data that corresponds to the STM-3/STS-3/STS-1 signal from the drop bus. The first bit received corresponds to bit 7.
DC1	49	I	TTL	**Drop C1 Pulse:** External positive C1 pulse that may be provided on this pin instead of in the DC1J1 signal. This signal is ORed internally with the DC1J1 signal to form a composite C1J1 signal. If this lead is not used it must be grounded.
DPAR	50	I	TTL	**Drop Bus Parity Bit:** This is an odd parity input for each data byte, the DSPE signal, and the composite DC1J1 pulses.
DCLK	51	I	TTL	**Drop Bus Clock:** This clock operates at 19.44 MHz for STM-1/STS-3 operation, and 6.48 MHz for STS-1 bus operation. Drop bus byte wide data (DDATA7-0), parity (DPAR), payload indicator (DSPE), and C1/J1 (DC1J1 and DC1) are clocked into the L3M on negative transitions of this clock.
DC1J1	52	I	TTL	**Drop Bus C1 and J1 Indicator:** The C1 pulse is an active high, one clock cycle wide timing pulse that indicates the location of the first C1 time slot in the STM-1 or STS-3 frame. If the C1 pulse is not present in this signal, it must be provided at the DC1 lead. A J1 pulse, also one clock cycle wide, identifies the location of the J1 byte.

Symbol	Pin No.	I/O/P	Type	Name/Function
DSPE	53	I	TTL	**Drop Bus SPE Indicator:** A signal that is high during the STM-1 VC-4, and the STS-3/STS-1 SPE period.

Add Bus Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
APAR	57	O 3-state	TTL4mA	**Add Bus Parity Bit:** This output bit represents the odd parity calculation for each data byte in the add timing and drop timing modes. In the external timing mode, the parity calculation also includes the ASPE and AC1J1 signals which become outputs. This lead is forced to a high impedance state when the control bit ADDZ is written with a 1, or when $\overline{ADD}$ is inactive (high).
ASPE	58	I/O 3-state	TTL4mA	**Add Bus SPE Indicator:** An input signal that is active high during the STM-1 VC-4 period, and STS-3/STS-1 SPE period. When enabled by the external clock enable (XCLKE) control pin, this signal becomes an output. This lead is forced to a high impedance state when the control bit ADDZ is written with a 1, or when the drop timing mode is selected.
AC1J1	59	I/O 3-state	TTL4mA	**Add Bus C1 and J1 Indicator:** The C1 pulse is an active high, one clock cycle wide input timing pulse that identifies the location of the first C1 time slot in the STM-1 or STS-3 frame. A J1 pulse, also one clock cycle wide, identifies the location of the J1 byte. When enabled by the external clock enable (XCLKE) control pin, this signal becomes an output. This lead goes to a high impedance state when control bit ADDZ is written with a 1, or, when the drop timing mode is selected.
$\overline{ADD}$	60	O 3-state	TTL4mA	**Add Indicator:** An active low signal that identifies the position of the data time slots being mapped onto the add bus. The time slots may be fixed stuff or data, as determined by the L3M. This lead is forced to the high impedance state when the control bit ADDZ is written with a 1.
ACLK	61	I/O	TTL4mA	**Add Bus Clock:** This clock operates at 19.44 MHz for STM-1/STS-3 operation, and at 6.48 MHz for STS-1 bus operation. The add clock is used for build timing and for sourcing the add bus byte wide data (AD7-0), parity (APAR), and add indicator. When enabled by the external clock enable (XCLKE) control lead, this signal becomes an output. This lead goes to a high impedance state when control bit ADDZ is written with a 1.

Symbol	Pin No.	I/O/P	Type	Name/Function
ADATA (7-0)	63 - 70	O 3-state	TTL4mA	**Add Data Byte:** Byte-wide data that corresponds to the STM-3/STS-3/STS-1 time slots that are placed on the add bus. Bit 7 corresponds to bit 1 in the STM-1/ SONET transmission format. This bus is forced to a high impedance state when the control bit ADDZ is written with a 1, or when $\overline{ADD}$ is inactive (high).

Overhead Comm Channel Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
ROCHD	25	O	TTL4mA	**Receive Overhead Comm Channel Data:** Unaligned data output for the overhead communications channel O-bits from the DS3 format. The O-bits are clocked out of the L3M on negative transitions of the ROCHC clock signal.
ROCHC	26	O	TTL4mA	**Receive Overhead Comm Channel Clock:** A gapped 720 kHz output clock with an average frequency of 144 kHz for outputting the transmit overhead communications channel bits to external circuitry.
TOCHC	90	O	TTL4mA	**Transmit Overhead Comm Channel Clock:** A gapped 720 kHz output clock with an average frequency of 144 kHz for sourcing the transmit overhead communications channel bits from external circuitry.
TOCHD	91	I	TTL	**Transmit Overhead Comm Channel Data:** Data input for the overhead communications channel in the DS3 format. Data is clocked into the L3M on positive transitions of the TOCHC clock signal. The bits are multiplexed into the O-bit positions unaligned regarding bit position and subframe number.

Path Overhead Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
RPOHD	30	O	TTL4mA	**Receive Path Overhead Data:** The serial output for the nine path overhead bytes. The POH bytes are clocked out on negative transitions of the clock signal (RPOHC).
RPOHF	31	O	TTL4mA	**Receive Path Overhead Framing:** A positive one clock cycle (RPOHC) wide output framing pulse that is synchronous with the J1 byte. This signal is also used as the framing pulse for the receive alarm indication port data (RAIPD).
RPOHC	32	O	TTL4mA	**Receive Path Overhead Clock:** A gapped clock used for clocking out the path overhead bytes, and receive alarm indication port data (RAIPD).
TPOHC	79	O	TTL4mA	**Transmit Path Overhead Clock:** A gapped clock used for clocking the path overhead bytes from an external circuit into the L3M.
TPOHF	80	O	TTL4mA	**Transmit Path Overhead Framing:** A positive one clock cycle (TPOHC) wide output framing pulse that determines the start of the J1 byte.
TPOHD	81	I	TTL	**Transmit Path Overhead Data:** A serial input for the following path overhead bytes: J1, G1, C2, F2, H4, Z3, Z4, and Z5 bytes. The POH bytes are clocked into the L3M on positive transitions of the TPOHC clock signal. Eight bits are clocked in during the B3 byte time, but they are ignored by the L3M.

Alarm Indication Port

Symbol	Pin No.	I/O/P	Type	Name/Function
RAIPD	28	O	TTL4mA	**Receive Alarm Indication Port Data:** A serial output that provides the 4-bit FEBE count (B3 error count) and Path RDI alarm indication to a mate L3M for ring operation. This lead is normally connected to the TAIPD lead at the mate L3M. The RPOHC signal is used to clock this signal out of the L3M. The RPOHF signal provides the frame reference signal. The bits are sent in the following format: Bits: 1 2 3 4 | 5 | 6 7 8 B3 Count | RDI | 0 0 1 Bit 1 is the MSB and is sent first in the bit stream.

Symbol	Pin No.	I/O/P	Type	Name/Function
TAIPC	83	I	TTL	**Transmit Alarm Indication Port Clock:** This clock input is normally connected to the RPOHC clock lead at the mate L3M for ring operation. Transmit alarm data (TAIPD) is clocked into the L3M on positive transitions of the RPOHC clock.
TAIPF	84	I	TTL	**Transmit Alarm Indication Port Framing Pulse:** Normally connected to RPOHF lead at the mate L3M for ring operation. Used to indicate the first bit in the first byte for the external alarm indications.
TAIPD	85	I	TTL	**Transmit Alarm Indication Port Data:** This serial input lead is normally connected to the RAIPD lead at the mate L3M for ring operation. Provides an input for the four bit FEBE count (B3 error count), and Path RDI alarm indication.

Additional Signals

Symbol	Pin No.	I/O/P	Type	Name/Function
AISCLK	1	I	CMOS	**AIS Clock Input:** Clock input for the L3M AIS generator. This clock must be present in order for the AIS generator to function. The clock must have the operating line rate of either 44.736 or 34.368 MHz, and have a frequency stability of at least +/- 20 ppm.
TEST	21,22, 35,36			**TranSwitch Test Pins:** No connections; do not use.
XCLKI	75	I	CMOS	**External Clock Input:** Used to derive output timing and data for the add bus. Enabled by placing a high on the lead labeled XCLKE. A byte clock frequency of 6.48 MHz is required for STS-1 operation. This clock is monitored for loss of clock when the external timing mode is selected.
XC1	76	I	TTL	**External C1 Input:** Optional C1 input signal used to synchronize the frame start when the external timing mode is selected for the add bus.
XCLKE	77	I	TTL	**External Clock Enable:** A high on this lead enables add bus timing to be derived from the XCKLI lead (external clock signal). The ASPE, AC1J1, and ACLK signal leads become output leads.
$\overline{\text{RESET}}$	86	I	TTLp	**Hardware Reset:** A low clears all counters and datapaths. This pin is provided with an internal pull-up resistor. The reset signal must be low for a minimum of 200 nanoseconds. The bus clocks and VCXO clocks must be present.

Symbol	Pin No.	I/O/P	Type	Name/Function
STAI	94	I	TTL	**STS Network Alarm Indication:** A high on this lead will generate a count of 9 in bits 1 through 4 of G1 when control bit FEBE9EN is equal to 1. An indication is also provided as the XSTAI alarm.
PAIS	95	I	TTL	**External Path AIS Indication:** A high on this lead indicates an external Path AIS has occurred. An indication is also provided as the XPAIS alarm. The alarm actions taken by this pin are enabled when a 1 is written to control bit XALM2AIS. When enabled, the alarm actions taken by detecting an AIS in the E1 byte are disabled.
ISTAT	96	I	TTL	**External STS-1 Alarm Indication:** A high on this lead indicates an external SONET alarm has occurred. An indication is also provided as the XISTAT alarm. The alarm actions taken by this pin are enabled when a 1 is written to control bit XALM2AIS. When enabled, the alarm actions taken by detecting an AIS in the E1 byte are disabled.
$\overline{\text{TRI}}$	107	I	TTLp	**High Impedance Enable:** A low causes all L3M outputs and bi-directional pins to a high impedance state for test purposes. This pin is provided with an internal pull-up resistor.

Receive and Transmit Phase Locked Loops

Symbol	Pin No.	I/O/P	Type	Name/Function
RCAP	16	I	Analog	**Receiver Internal Phase Locked Loop Capacitor:** Optional capacitor used for an internal receive phase lock loop.
TEST	19	I/O		**TranSwitch Test for Receive PLL:** Do not use.
TEST	82	I/O		**TranSwitch Test for Transmit PLL:** Do not use
TCAP	99	I	Analog	**Transmitter Internal Phase Locked Loop Capacitor:** Optional capacitor used for an internal transmit phase lock loop.

Receive Desynchronizer

Symbol	Pin No.	I/O/P	Type	Name/Function
XOSCI	2	I	CMOS	**External Oscillator Input:** This input is connected to the output of the external VCXO, as shown in the VCXO application in this data sheet. The external VCXO is selected by writing a 1 to control bit XVCXO.

Symbol	Pin No.	I/O/P	Type	Name/Function
CTRL	3	O	TTL8mA	**Phase Detector Output**: Normally connected to the external low pass filter consisting of external components and the internal amplifier.
AMPINM	5	I	Analog	**Low Pass Filter Internal Amplifier - Negative Port Input:** Negative port of an internal amplifier which is used as a low pass filter.
AMPINP	6	I	Analog	**Low Pass Filter Internal Amplifier - Positive Port Input:** Positive port of an internal amplifier which is used as a low pass filter.
AMPOUT	7	O	Analog	**Low Pass Filter Internal Amplifier, Output.**
OSCO	8	O	CMOS4mA	**Internal VCXO Oscillator Output:** Internal VCXO oscillator output provided for testing purposes only.
XTAL2	12	I	CMOS	**Internal VCXO Crystal Input:** Required if the internal VCXO is used.
XTAL1	13	I	CMOS	**Internal VCXO Crystal Input:** Required if the internal VCXO is used. The following are the crystal characteristics: DS3: Mode: Fundamental, parallel redundant Frequency: 44736000 Hz Cm: 22fF ± 10% Rm: < 20 ohms Cl: 10.5 pF Tolerance: ± 50 ppm Drive Level: 500 µW RMS E3: Mode: Fundamental, parallel redundant Frequency: 34368000 Hz (E3) Cm: 20 fF ± 10% Rm: < 20 ohms Cl: 10.5 pF Tolerance: ± 60 ppm Drive Level: 500 µW RMS
APWR	10,14,101	P		**Analog VDD:** +5 Volts
AGND	9,15,100	P		**Analog Ground.**
FPWR	18,98	P		**Analog VDD2:** +5 Volts
FGND	17,97	P		**Analog Ground2.**

Boundary Scan Testing

Symbol	Pin No.	I/O/P	Type	Name/Function
TDO	102	O	TTL4mA	**Boundary Scan Data Output:** Serial data clocked out on negative transitions of TCK.
TDI	103	I	TTL	**Boundary Scan Data Input:** Serial data input for boundary scan test messages.
TCK	104	I	TTL	**Boundary Scan Clock:** The input clock for boundary scan testing. The TDI and TMS states are clocked in on positive transitions.
TMS	105	I	TTL	**Boundary Scan Mode Select:** The signal present on this lead is used to control test operations.
$\overline{\text{TRS}}$	106	I	TTLp	**Boundary Scan Reset:** When a low signal is applied to this pin, the L3M Test Access Port (TAP) controller resets, and the boundary scan capability is disabled. The controller is also reset by holding the TMS signal lead high for at least five rising clock transitions of TCK. When the boundary scan feature is not used, this pin must be held low.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	7.0	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Continuous power dissipation	P_C		0.5	Watts
Ambient operating temperature	T_A	-40	85	^oC
Operating junction temperature	T_J		125	^oC
Storage temperature range	T_S	-55	125	^oC

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal res - junc to ambient			34	$^oC/W$	
Thermal res - junc to case		12		$^oC/W$	

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5	5.25	V	
I_{DD}			190	mA	
P_{DD}			997.5	mW	Inputs switching
Analog V_{DD}	4.75	5	5.25	V	
Analog I_{DD}			30	mA	
Filtered V_{DD}	4.75	5	5.25	V	
Filtered I_{DD}					

INPUT, OUTPUT, AND I/O PARAMETERS

Input Parameters For CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			1.65	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	
Input capacitance		3.5		pF	

Input Parameters For TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		0.5	1.4	mA	$V_{DD} = 5.25$; Input = 0 volts
Input capacitance		3.5		pF	

Output Parameters For CMOS4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -4.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 4.0$
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	1.2	2.8	5.0	ns	$C_{LOAD} = 15pF$
t_{FALL}	0.9	2.0	4.1	ns	$C_{LOAD} = 15pF$

Input/Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -2.0$ mA
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 4.0$ mA
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.5	5.5	10.0	ns	$C_{LOAD} = 15$pF
t_{FALL}	1.0	2.0	4.0	ns	$C_{LOAD} = 15$pF

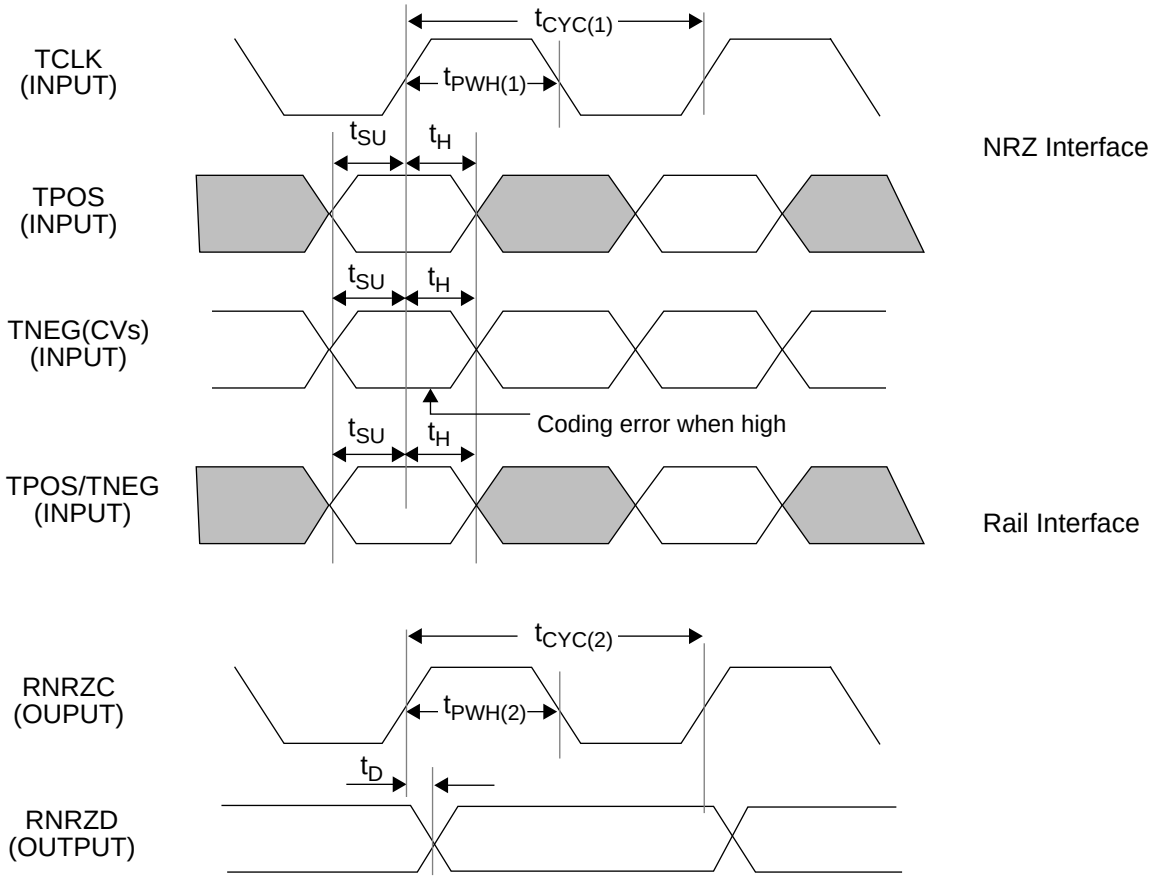
Input/Output Parameters For TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -4.0$ mA
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 8.0$ mA
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	1.9	4.5	8.0	ns	$C_{LOAD} = 25$pF
t_{FALL}	0.8	1.5	3.1	ns	$C_{LOAD} = 25$pF

TIMING CHARACTERISTICS

Detailed timing diagrams for the L3M are illustrated in Figures 5 through 26, with values of the timing intervals following each figure. All output times are measured with a maximum 25 pF load capacitance. Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

Figure 5. Line Side Transmit Timing

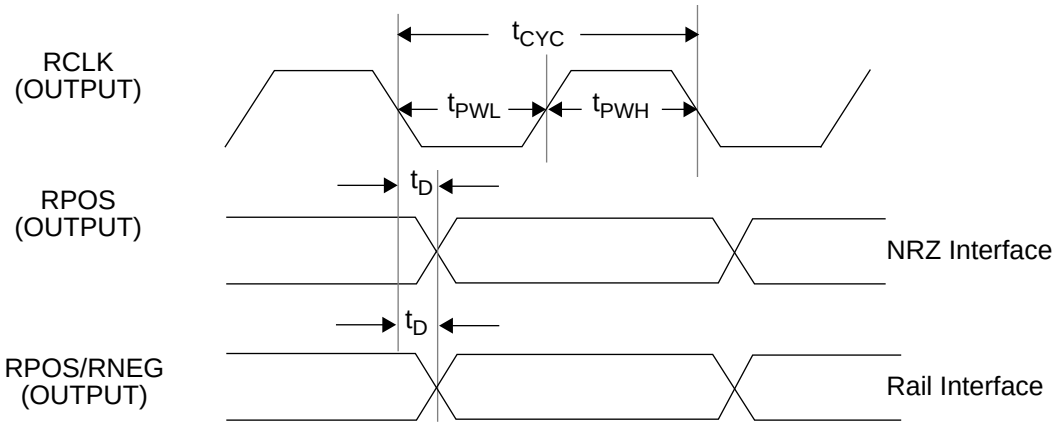


Note: Shown for TINVC equal to 0; data is clocked in on the negative edge when TINVC equals 1. RNRZD is always clocked out on the positive transitions of RNRZC. The delay between the input clock TCLK and output clock RNRZC is not specified.

Parameter	Symbol	Min	Typ	Max	Unit
TCLK clock period	$t_{CYC(1)}$		*		ns
TCLK duty cycle ($t_{PWH(1)}/t_{CYC(1)}$)	--	40	50	60	%
Input set-up time to TCLK↑	t_{SU}	4.0			ns
Input hold time after TCKL↑	t_H	2.0			ns
RNRZC clock period	$t_{CYC(2)}$		*		ns
RNRZC duty cycle ($t_{PWH(2)}/t_{CYC(2)}$)	--	40	50	60	%
RNRZD output delay after RNRZC↑	t_D	-2.0		5.0	ns

* 22.35 ns (DS3) or 29.10 ns (E3).

Figure 6. Line Side Receive Timing

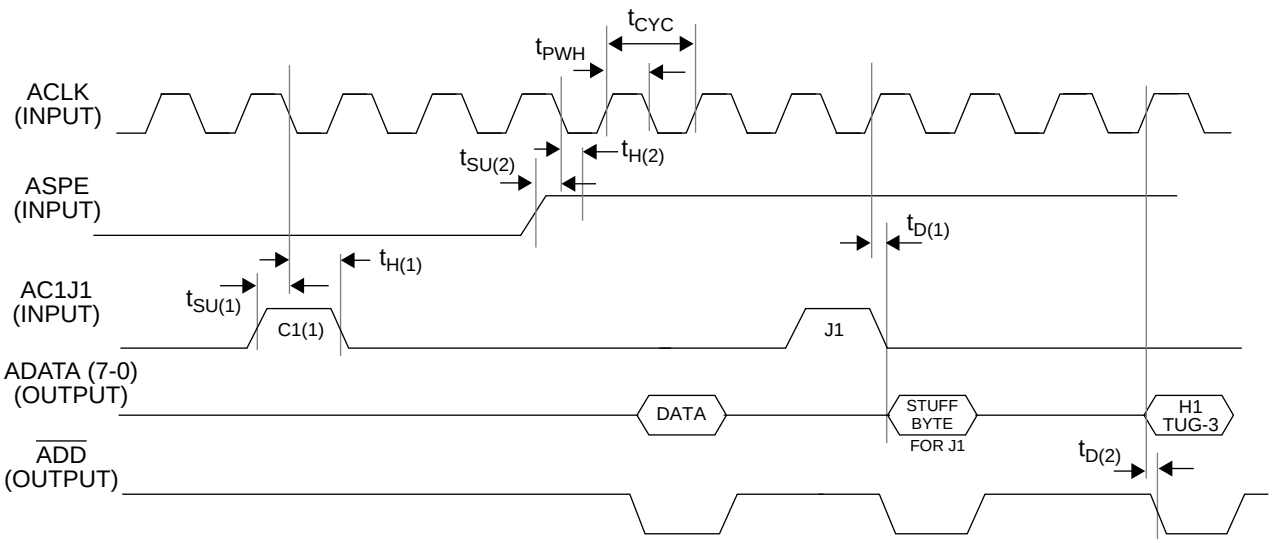


Note: Shown for RINVC equal to 0; data is clocked out on the positive edge when RINVC equals 1. The three signals are forced to a high impedance state when control bit L3Z is written with a 1.

Parameter	Symbol	Min	Typ	Max	Unit
RCLK clock period	t_{CYC}		*		ns
RCLK high time	t_{PWH}		$t_{CYC}/2$		ns
RCLK low time	t_{PWL}		$t_{CYC}/2$		ns
Data output delay after RCLK↓	t_D	-2.0		5.0	ns

*22.35 ns (DS3) or 29.10 ns (E3).

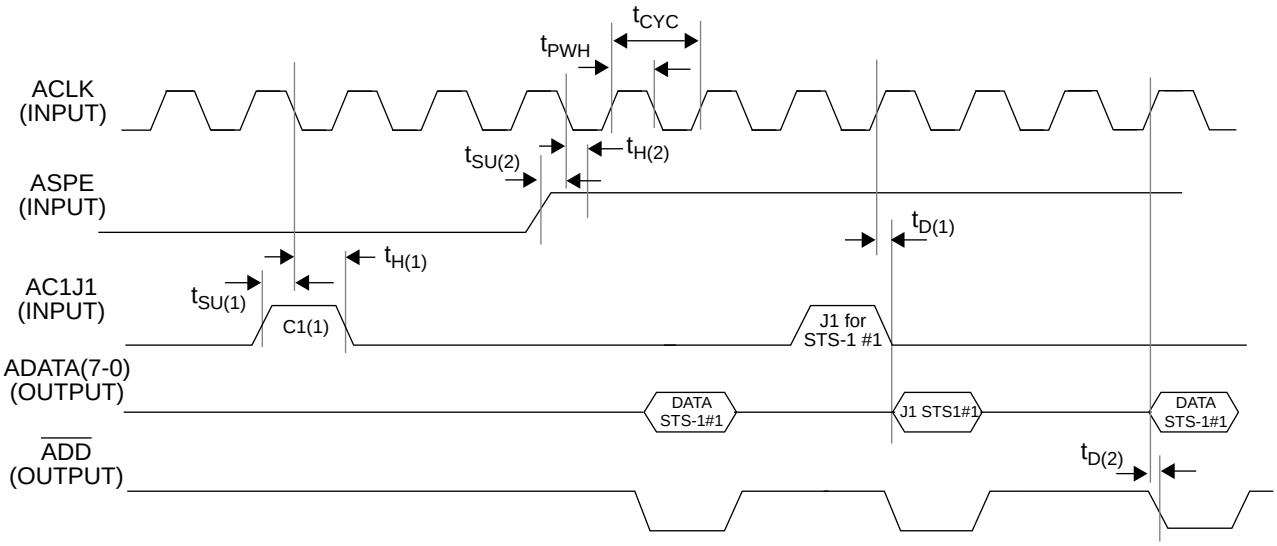
Figure 7. STM-1 Add Bus Derived Interface Timing



Note: The relationship between J1 and the SPE signal is shown for illustration purposes only. For the STM-1 format, there will be one J1 pulse which indicates the start of the VC-4 that carries the three TUG-3s. The TUG-3 added to the bus is shown for TUG-3 designated as A. TUG-3 B will occur one clock cycle later.

Parameter	Symbol	Min	Typ	Max	Unit
ACLK clock period	t_{CYC}		51.44		ns
ACLK duty cycle (t_{PWH}/t_{CYC})	--	40	50	60	%
AC1J1 set-up time to ACLK↓	$t_{SU(1)}$	7.0			ns
AC1J1 hold time after ACLK↓	$t_{H(1)}$	3.0			ns
ASPE set-up time to ACLK↓	$t_{SU(2)}$	10.0			ns
ASPE hold time after ACLK↓	$t_{H(2)}$	5.0			ns
Data output delay from ACLK↑	$t_{D(1)}$			30.0	ns
Add low output delay from ACLK↑	$t_{D(2)}$			15.0	ns

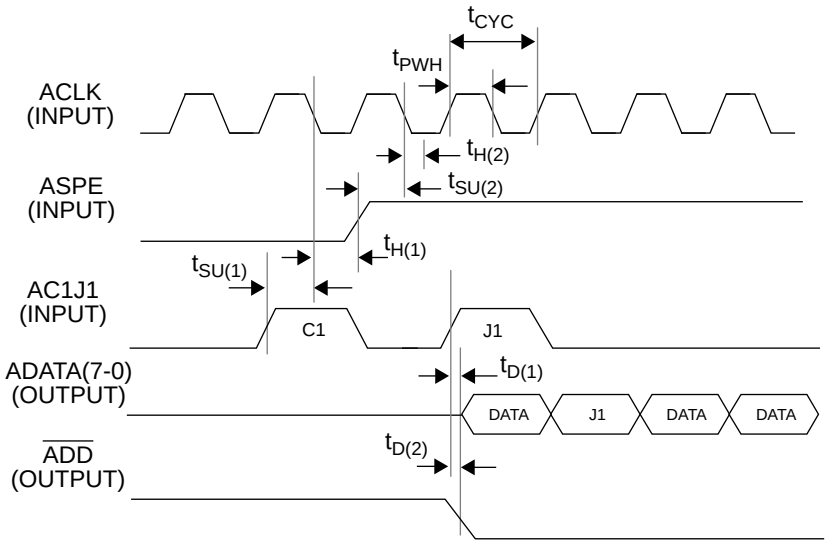
Figure 8. STS-3 Add Bus Derived Interface Timing



Note: The relationship between J1 and the SPE signal is shown for illustration purposes only. For the STS-3 format, there will be three J1 pulses which indicate the start of each of the STS-1 SPEs. The STS-1 SPE added to the bus is shown for STS-1 number 1. STS-1 number 2 will occur one clock cycle later. There is always a one byte delay between the output ADATA and AC1J1/ASPE inputs.

Parameter	Symbol	Min	Typ	Max	Unit
ACLK clock period	t_{CYC}		51.44		ns
ACLK duty cycle (t_{PWH}/t_{CYC})	--	40	50	60	%
AC1J1 set-up time to ACLK↓	$t_{SU(1)}$	7.0			ns
AC1J1 hold time after ACLK↓	$t_{H(1)}$	3.0			ns
ASPE set-up time to ACLK↓	$t_{SU(2)}$	10.0			ns
ASPE hold time after ACLK↓	$t_{H(2)}$	5.0			ns
Data output delay from ACLK↑	$t_{D(1)}$			30.0	ns
Add low output delay from ACLK↑	$t_{D(2)}$			15.0	ns

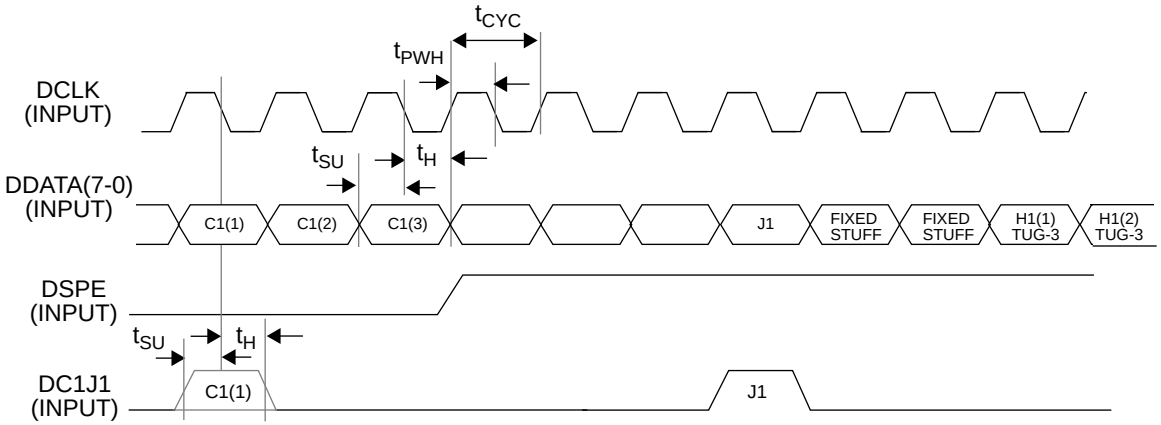
Figure 9. STS-1 Add Bus Derived Interface Timing



Note: The relationship between J1 and the SPE signal is shown for illustration purposes only. There is always a one byte delay between the output ADATA and AC1J1/ASPE inputs.

Parameter	Symbol	Min	Typ	Max	Unit
ACLK clock period	t_{CYC}		154.32		ns
ACLK duty cycle (t_{PWH}/t_{CYC})	--	40	50	60	%
AC1J1 set-up time to ACLK↓	$t_{SU(1)}$	7.0			ns
AC1J1 hold time after ACLK↓	$t_{H(1)}$	3.0			ns
ASPE set-up time to ACLK↓	$t_{SU(2)}$	10.0			ns
ASPE hold time after ACLK↓	$t_{H(2)}$	5.0			ns
Data output delay from ACLK↑	$t_{D(1)}$			30.0	ns
Add low output delay from ACLK↑	$t_{D(2)}$			15.0	ns

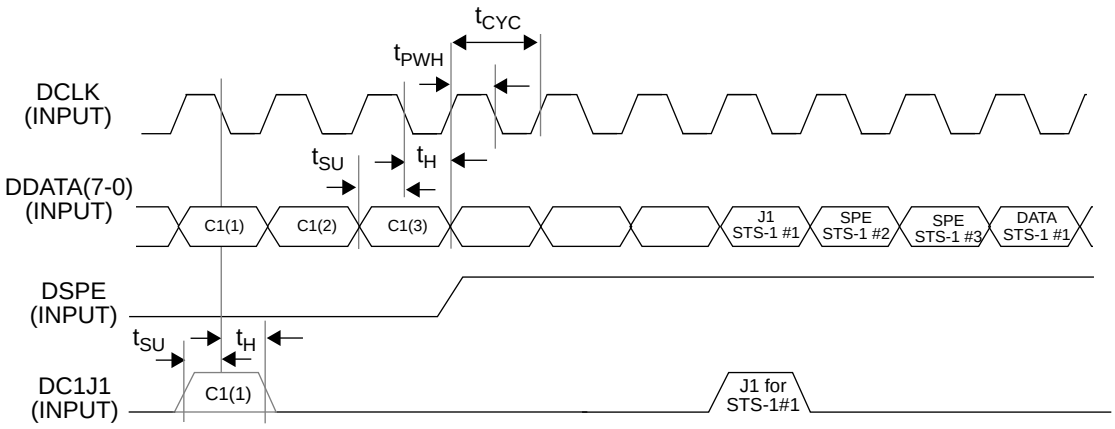
Figure 10. STM-1 Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STM-1 format, there will be one J1 pulse which indicates the start of the VC-4 that carries the three TUG-3s. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		51.44		ns
DCLK duty cycle (t_{PWH}/t_{CYC})	--	40	50	60	%
Data/DC1J1 set-up time to DCLK↓	t_{SU}	7.0			ns
Data/DC1J1 hold time after DCLK↓	t_H	3.0			ns

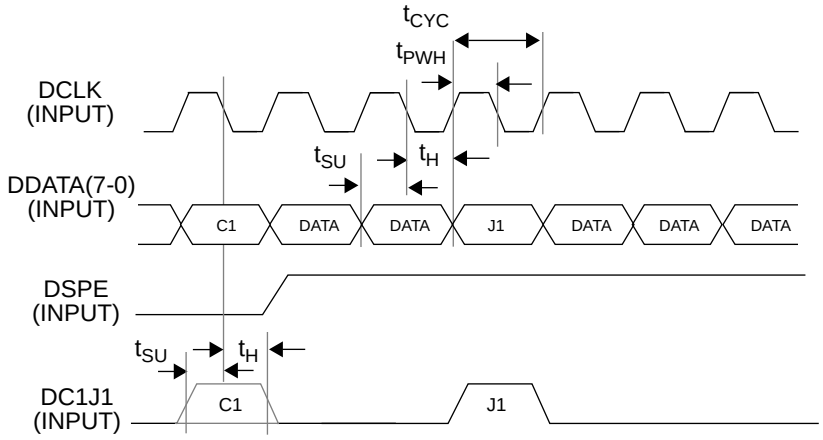
Figure 11. STS-3 Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STS-3 format, there will be three J1 pulses which indicate the start of each of the STS-1 SPEs. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		51.44		ns
DCLK duty cycle (t_{PWH}/t_{CYC})	--	40	50	60	%
Data/DC1J1 set-up time to DCLK↓	t_{SU}	7.0			ns
Data/DC1J1 hold time after DCLK↓	t_H	3.0			ns

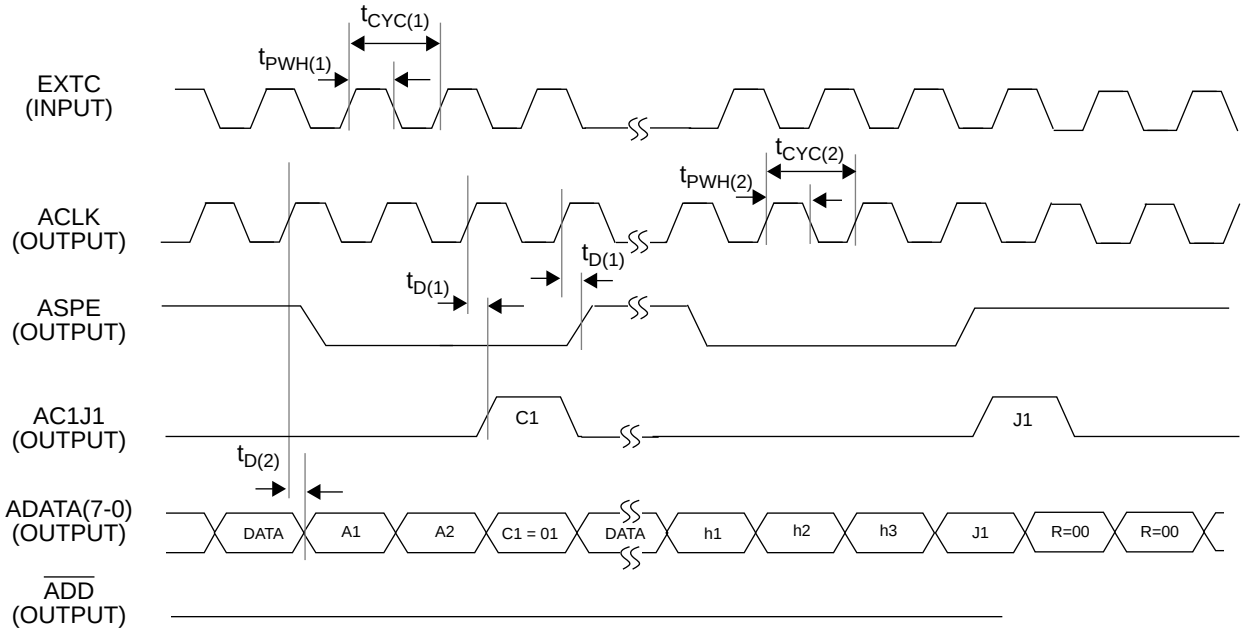
Figure 12. STS-1 Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STS-1 format, there will be one J1 pulse which indicates the start of the STS-1 SPE. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		154.32		ns
DCLK duty cycle (t_{PWH}/t_{CYC})	--	40	50	60	%
Data/DC1J1 set-up time to DCLK↓	t_{SU}	7.0			ns
Data/DC1J1 hold time after DCLK↓	t_H	3.0			ns

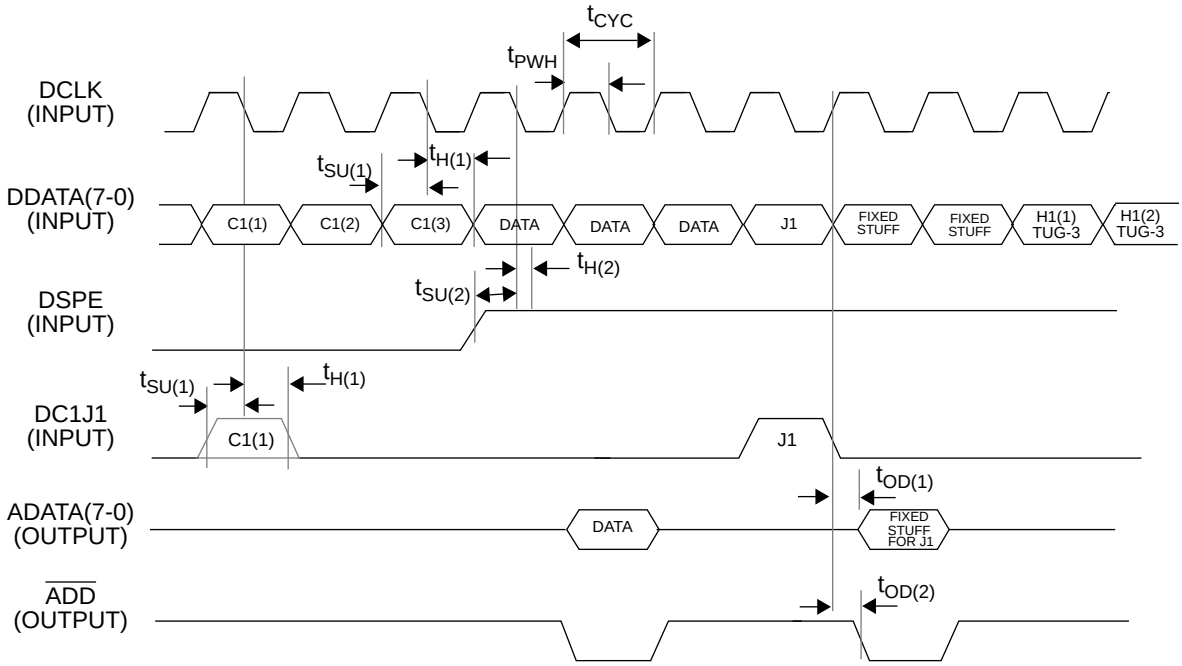
Figure 13. STS-1 Add Bus Interface Timing Using An External Clock



Note: Timing is shown for STS-1 signal. Pointer value is transmitted with a value equal to 0. When the TOHOUT bit is written with a 1, the A1, A2, C1, H1, and H2 bytes are generated. Different from add/drop mode, output AC1J1/ ASPE and ADATA are synchronous in the EXT clock mode.

Parameter	Symbol	Min	Typ	Max	Unit
EXTC clock period	$t_{CYC(1)}$		154.32		ns
EXTC duty cycle ($t_{PWH(1)}/t_{CYC}$)	--	40	50	60	%
ACLK clock period	$t_{CYC(2)}$		154.32		ns
ACLK duty cycle ($t_{PWH(2)}/t_{CYC}$)	--	40	50	60	%
AC1J1/ASPE delay after ACLK↑	$t_{D(1)}$	0		5.0	ns
Data delay after ACLK↑	$t_{D(2)}$			30.0	ns

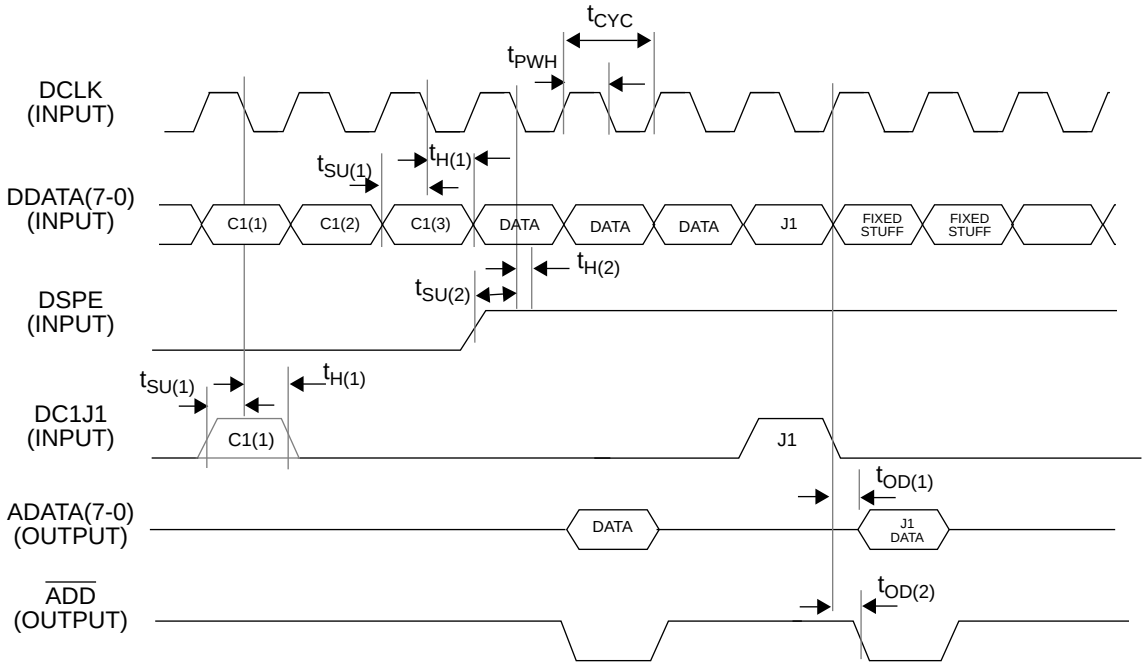
Figure 14. STM-1 Add/Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STM-1 format, there will be one J1 pulse which indicates the start of the VC-4 that carries the three TUG-3s. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded. Shown is TUG-3 A being added to the Add bus.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		51.44		ns
DCLK duty cycle (t_{PWH}/t_{CYC})	--	40	50	60	%
Data/DC1J1 set-up time to DCLK↓	$t_{SU(1)}$	7.0			ns
Data/DC1J1 hold time after DCLK↓	$t_{H(1)}$	3.0			ns
DSPE set-up time to DCLK↓	$t_{SU(2)}$	10.0			ns
DSPE hold time after DCLK↓	$t_{H(2)}$	5.0			ns
Data out delayed after DCLK↑	$t_{OD(1)}$			30.0	ns
Add indicator delayed after DCLK↑	$t_{OD(2)}$			15.0	ns

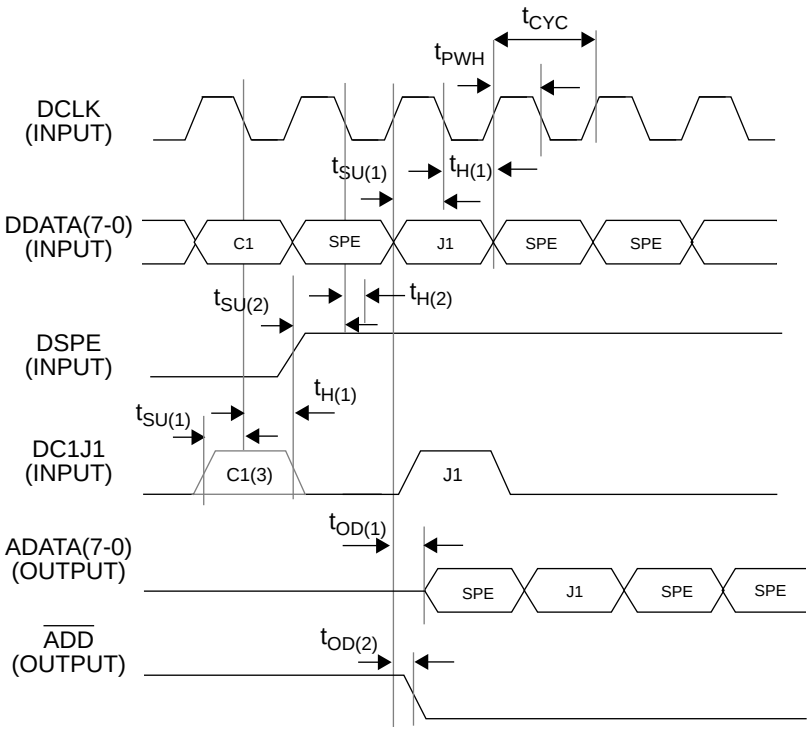
Figure 15. STS-3 Add/Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STS-3 format, there will be three J1 pulses with each J1 pulse indicating the start of an STS-1. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded. Shown is STS-1 number 1 being added to the Add bus.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		51.44		ns
DCLK duty cycle (t_{PWH}/t_{CYC})	--	40	50	60	%
Data/DC1J1 set-up time to DCLK↓	$t_{SU(1)}$	7.0			ns
Data/DC1J1 hold time after DCLK↓	$t_{H(1)}$	3.0			ns
DSPE set-up time to DCLK↓	$t_{SU(2)}$	10.0			ns
DSPE hold time after DCLK↓	$t_{H(2)}$	5.0			ns
Data out delayed after DCLK↑	$t_{OD(1)}$			30.0	ns
Add indicator delayed after DCLK↑	$t_{OD(2)}$			15.0	ns

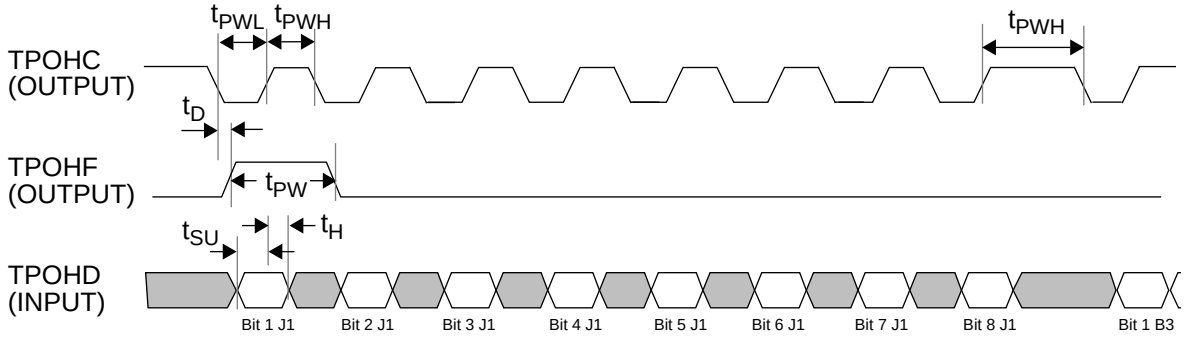
Figure 16. STS-1 Add/Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STS-1 format, there will be one J1 pulse which indicates the start of the STS-1. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		154.32		ns
DCLK duty cycle (t_{PWH}/t_{CYC})	--	40	50	60	%
Data/DC1J1 set-up time to DCLK↓	$t_{SU(1)}$	7.0			ns
Data/DC1J1 hold time after DCLK↓	$t_{H(1)}$	3.0			ns
DSPE set-up time to DCLK↓	$t_{SU(2)}$	10.0			ns
DSPE hold time after DCLK↓	$t_{H(2)}$	5.0			ns
Data out delayed after DCLK↑	$t_{OD(1)}$			30.0	ns
Add indicator delayed after DCLK↑	$t_{OD(2)}$			15.0	ns

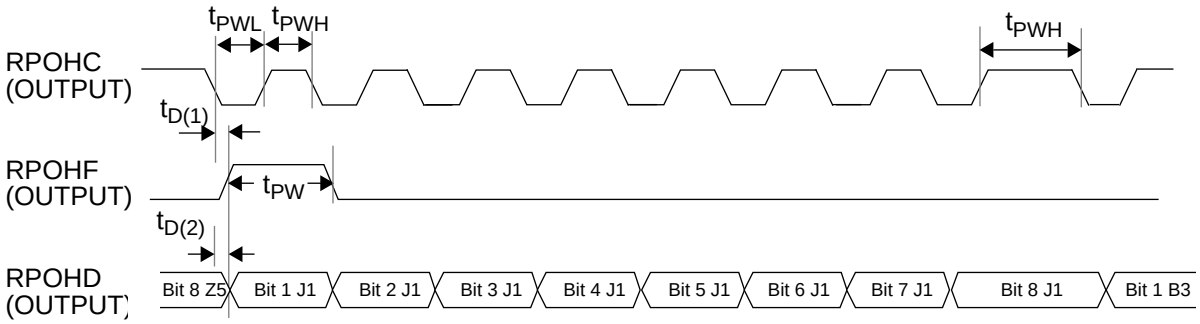
Figure 17. Transmit Path Overhead Timing



Note: The clock cycle that corresponds to bit 8 in each overhead byte is stretched.

Parameter	Symbol	Min	Typ	Max	Unit
TPOHC high time	t_{PWH}	617		3395	ns
TPOHC low time	t_{PWL}		771.7		ns
TPOHF output delay after TPOHC↓	t_D	-2.0		5.0	ns
TPOHD set-up time to TPOHC↑	t_{SU}	7.0			ns
TPOHD data hold time after TPOHC↑	t_H	3.0			ns
TPOHF pulse width	t_{PW}		1388.9		ns

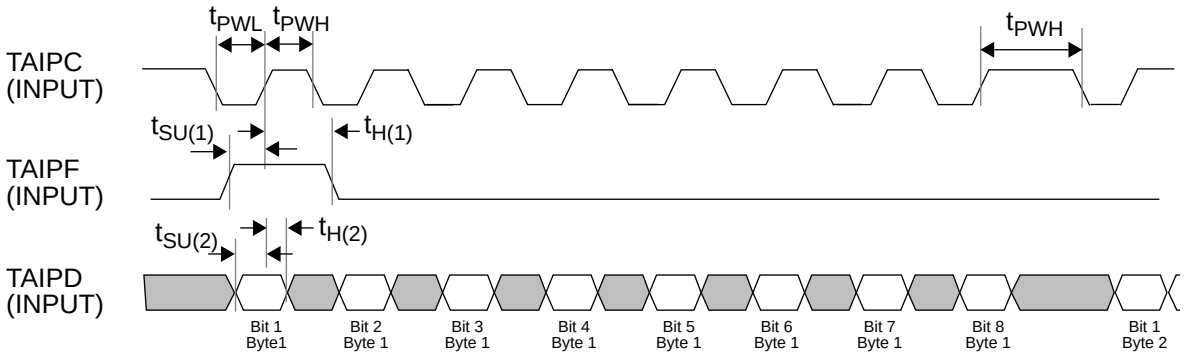
Figure 18. Receive Path Overhead Timing



Note: The clock cycle that corresponds to bit 8 in each overhead byte is stretched.

Parameter	Symbol	Min	Typ	Max	Unit
RPOHC high time	t_{PWH}	617		3395	ns
RPOHC low time	t_{PWL}		771.7		ns
RPOHF output delay after RPOHC↓	$t_{D(1)}$	-2.0		5.0	ns
RPOHD output delay after RPOHC↓	$t_{D(2)}$	-2.0		5.0	ns
RPOHF pulse width	t_{PW}		1388.9		ns

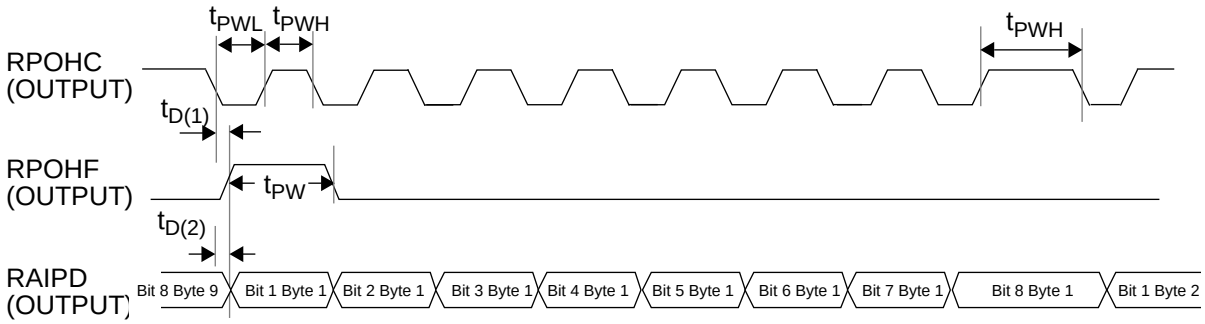
Figure 19. Transmit Alarm Indication Port Timing



Note: Alarm indication byte consists of eight bits repeated nine times. Bit 8 in each byte is stretched. The first four bits correspond to the FEBE count (bits 1 through 4 in G1), bit 5 is the path RDI value, and bits 6 and 7 are set to 0, while bit 8 is set to 1.

Parameter	Symbol	Min	Typ	Max	Unit
TAIPC high time	t_{PWH}	617		3395	ns
TAIPC low time	t_{PWL}		771.7		ns
TAIPF set-up time to TAIPC↑	$t_{SU(1)}$	7.0			ns
TAIPF hold time after TAIPC↑	$t_{H(1)}$	3.0			ns
TAIPD set-up time to TAIPC↑	$t_{SU(2)}$	7.0			ns
TAIPD set-up time after TAIPC↑	$t_{H(2)}$	3.0			ns

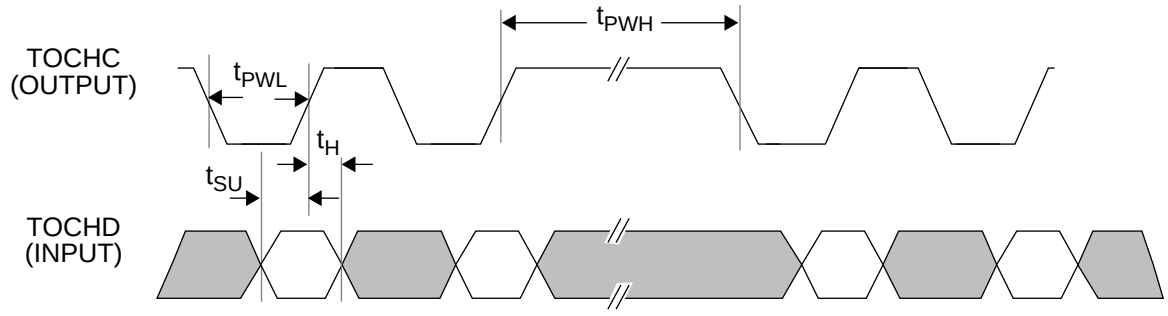
Figure 20. Receive Alarm Indication Port Timing



Note: Alarm indication byte consists of eight bits repeated nine times. Bit 8 in each byte is stretched. The first four bits correspond to the FEBE count (bits1 through 4 in G1), bit 5 is the path RDI value, and bits 6 and 7 are set to 0, while bit 8 is set to 1.

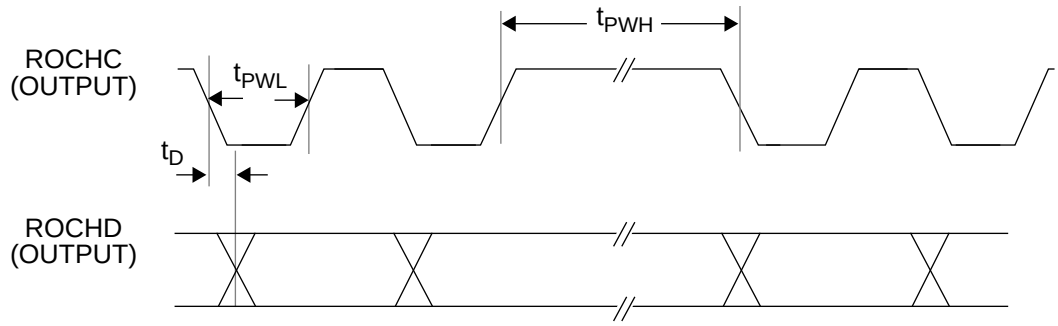
Parameter	Symbol	Min	Typ	Max	Unit
RPOHC high time	t_{PWH}	617		3395	ns
RPOHC low time	t_{PWL}		771.7		ns
RPOHF output delay after RPOHC↓	$t_{D(1)}$	-2.0		5.0	ns
RAIPD output delay after RPOHC↓	$t_{D(2)}$	-2.0		5.0	ns
RPOHF pulse width	t_{PW}		1388.9		ns

Figure 21. Transmit Overhead Communications Channel Timing



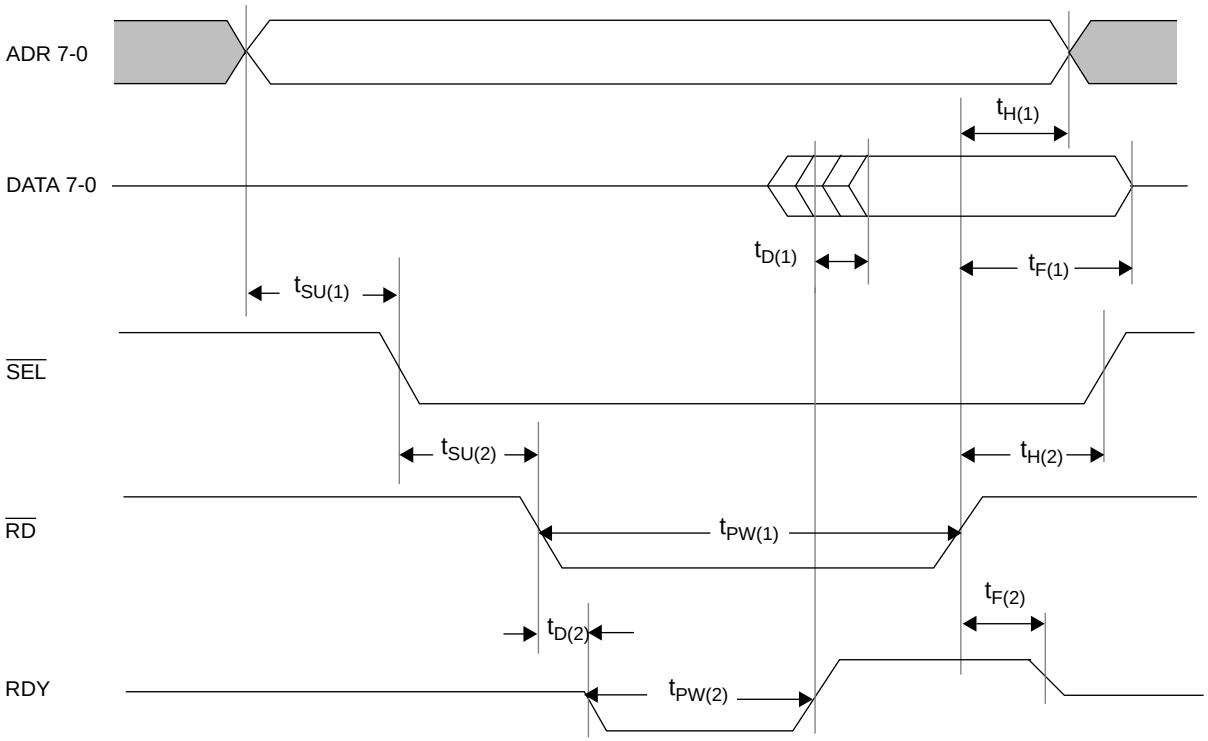
Parameter	Symbol	Min	Typ	Max	Unit
TOCHC high time	t_{PWH}	617		11729	ns
TOCHC low time	t_{PWL}		771.2		ns
TOCHD set-up time to TOCHC↑	t_{SU}	7.0			ns
TOCHD hold time after TOCHC↑	t_H	3.0			ns

Figure 22. Receive Overhead Communications Channel Interface Timing



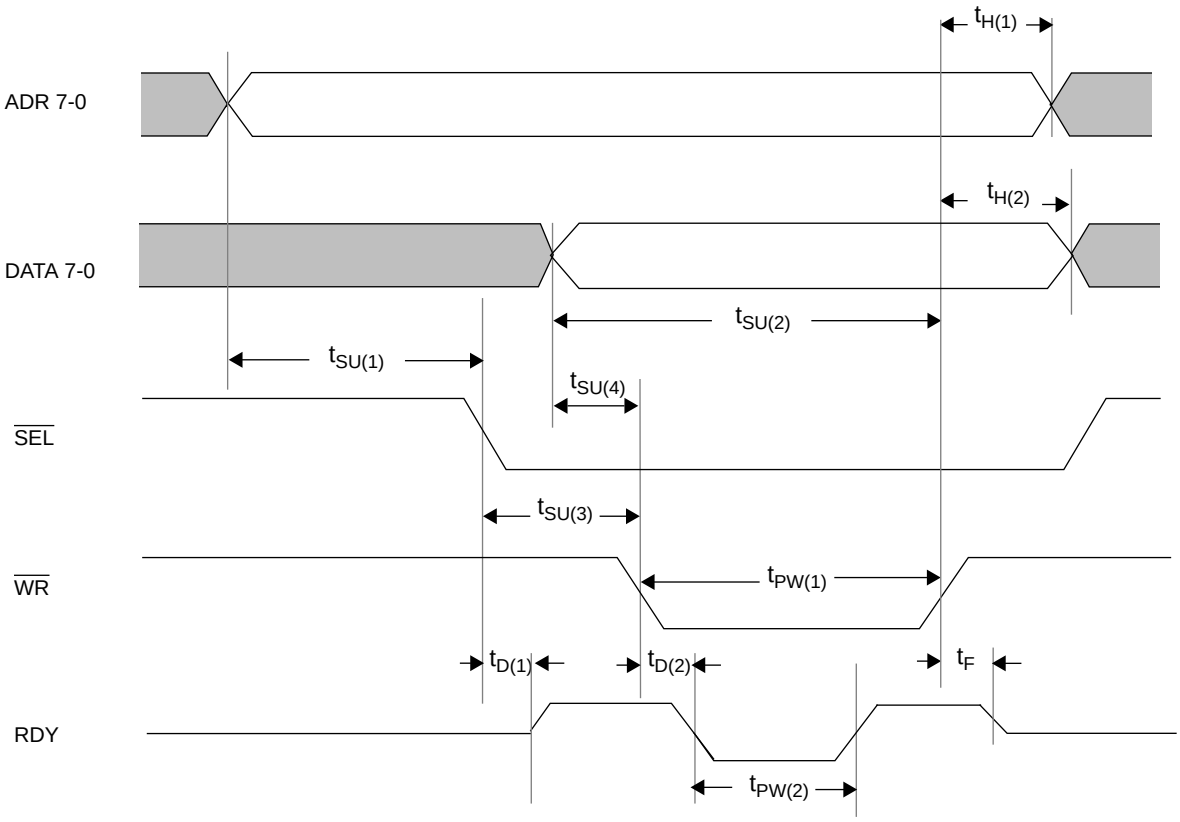
Parameter	Symbol	Min	Typ	Max	Unit
ROCHC high time	t_{PWH}	617		11729	ns
ROCHC low time	t_{PWL}		771.2		ns
ROCHD output delay after ROCHC↓	t_D	-2.0		-5.0	ns

Figure 23. Intel Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
ADR hold time after $\overline{RD}\uparrow$	$t_{H(1)}$	0.0			ns
ADR set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	10.0			ns
DATA valid delay after RDY$\uparrow$	$t_{D(1)}$			2.0	ns
DATA float time after $\overline{RD}\uparrow$	$t_{F(1)}$			5.0	ns
$\overline{RD}$ pulse width	$t_{PW(1)}$	40.0			ns
$\overline{SEL}\downarrow$ set-up time to $\overline{RD}\downarrow$	$t_{SU(2)}$	0.0			ns
$\overline{SEL}\uparrow$ hold time after $\overline{RD}\uparrow$	$t_{H(2)}$	0.0			ns
RDY$\downarrow$ delay after $\overline{RD}\downarrow$	$t_{D(2)}$			5.0	ns
RDY pulse width	$t_{PW(2)}$	0.0		4.0	µs
RDY float time after $\overline{RD}\uparrow$	$t_{F(2)}$			3.0	ns

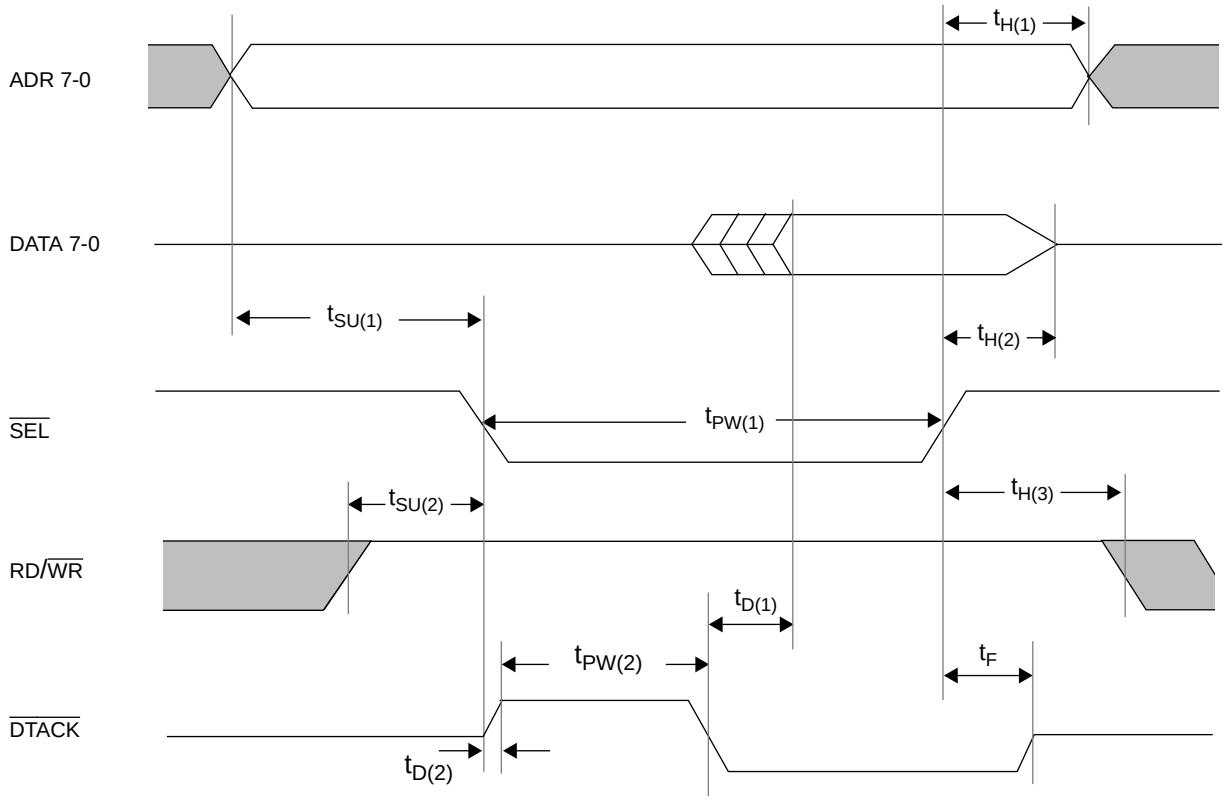
Figure 24. Intel MIcroprocessor Write Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
ADR hold time after $\overline{WR}\uparrow$	$t_{H(1)}$	0.0			ns
ADR set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
DATA valid set-up time to $\overline{WR}\uparrow$	$t_{SU(2)}$	20.0			ns
DATA hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	5.0			ns
$\overline{SEL}\downarrow$ set-up time to $\overline{WR}\downarrow$	$t_{SU(3)}$	10.0			ns
$\overline{WR}$ pulse width	$t_{PW(1)}$	40.0			ns
RDY$\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(1)}$			5.0	ns
RDY$\downarrow$ delay after $\overline{WR}\downarrow$	$t_{D(2)}$			5.0	ns
RDY pulse width	$t_{PW(2)}$	0.0		48 * Rcyc	ns
RDY float time after $\overline{WR}\uparrow$	t_F			3.0	ns
RAM cycle DATA valid set-up time to $\overline{WR}\downarrow$	$t_{SU(4)}$	-2 * Rcyc			ns

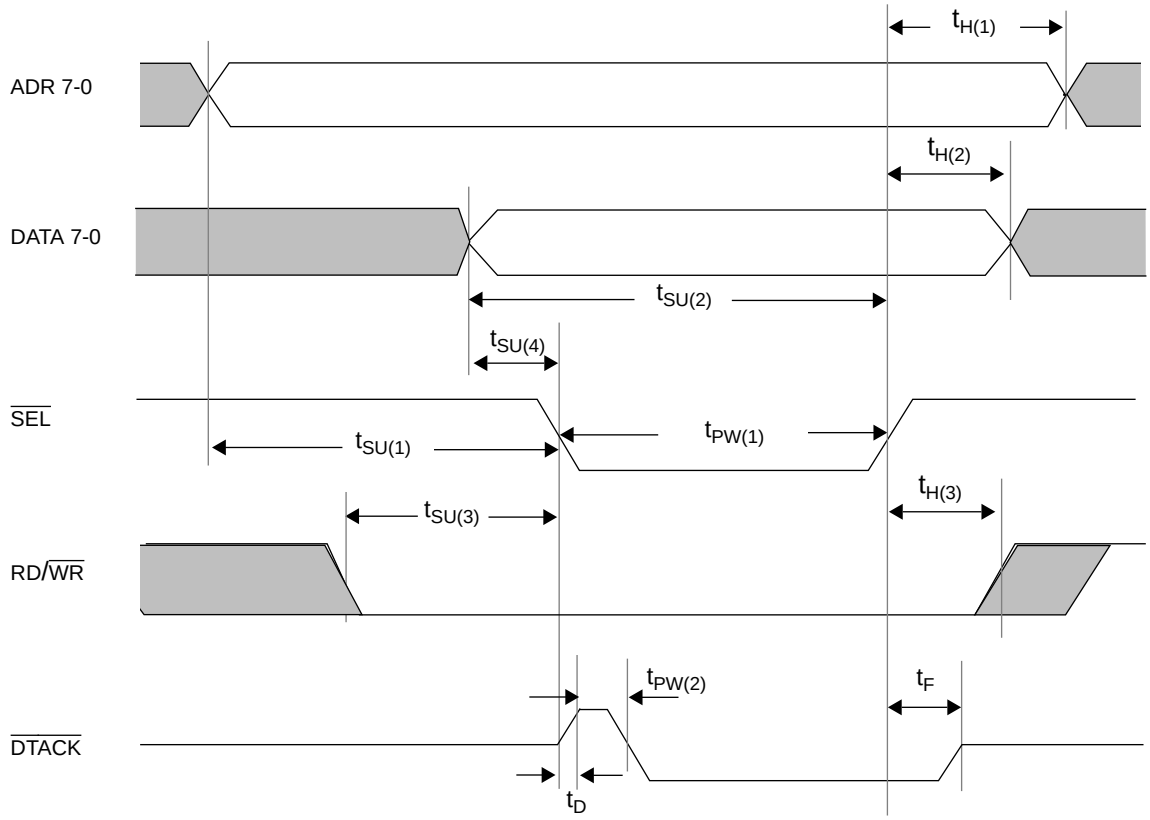
Note: Rcyc is the period, in nanoseconds, of the RAM clock (RCLK) [ie. RCLK @ 25MHz yields:
Tsu(4)=-80ns, Tpw(2)=1.92µs]

Figure 25. Motorola Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
ADR hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0.0			ns
ADR valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	10.0			ns
DATA valid delay after $\overline{DTACK}\downarrow$	$t_{D(1)}$	0.0			ns
DATA hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	5.0			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	40			ns
RD/$\overline{WR}\uparrow$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	5.0			ns
RD/$\overline{WR}\downarrow$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0.0			ns
$\overline{DTACK}\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$			5.0	ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	0.0		4.0	µs
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F			3.0	ns

Figure 26. Motorola Microprocessor Write Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
ADR hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0.0			ns
ADR valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	10.0			ns
DATA valid set-up time to $\overline{SEL}\uparrow$	$t_{SU(2)}$	20.0			ns
DATA hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	5.0			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	40.0			ns
RD/$\overline{WR}\downarrow$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(3)}$	5.0			ns
RD/$\overline{WR}\uparrow$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0.0			ns
$\overline{DTACK}\uparrow$ delay after $\overline{SEL}\downarrow$	t_D			5.0	ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	0.0		48 * Rcyc	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F			5.0	ns
RAM cycle DATA valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(4)}$	-2 * Rcyc			ns

Note: Rcyc is the period, in nanoseconds, of the RAM clock (RCLK) [ie. RCLK @ 25MHz yields:
Tsu(4)=-80ns, Tpw(2)=1.92µs]

OPERATION

L3M MEMORY MAP

Control Bits

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C0	R/W	MAP1	MAP0	DPOS1	DPOS0	APOS1	APOS0	FORM1	FORM0
C1	R/W	DECODE	CODE	INVCI	INVCO	RING	FLBK	L3LBK	SLBK
C2	R/W	ALM2AIS	ALM2FB9	TLAISGN	TPAISGN	TPAIS00	TEST	ADDZ	L3Z
C3	R/W	EXZ5	EXZ4	EXZ3	EXH4	EXF2	EXG1	EXC2	EXJ1
C4	R/W	EXOO	FEBE9EN	RAMRDI	FEBEEN	XALM2AIS	TEST	TLOC2AIS	TLOS2AIS
C5	R/W	COR	XVCXO	DROPT	POH2RAM	RAISGN	RAISEN	WGDEC	PSL2AIS
C6	R/W	FASTPTR	TOHOUT	H4CTR	PAT23	ENANA	TXANA	TPRBS	RPRBS
C7	R/W	TESTB3	FIXPTR	CCITT	TEST	TEST	TXRST	RXRST	RESETC
C8	R/W	C2 Comparison							
C9	R/W	TEST BYTE							

Status Bits

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B0	R	DLOC	DLOJ1	BUSERR	E1AIS	LOP	PAIS	PSLERR	C2EQ0
B1	R/W(L)	DLOC	DLOJ1	BUSERR	E1AIS	LOP	PAIS	PSLERR	C2EQ0
B2	R	RDI	L3LOS	L3LOC	TOVFL	L3AIS	RAMLOC	ALOC	ALOJ1
B3	R/W(L)	RDI	L3LOS	L3LOC	TOVFL	L3AIS	RAMLOC	ALOC	ALOJ1
B4	R	SINT	FEBE9	NEW	TUG3NEW	ROVFL	XSTAI	XISTAT	XPAIS
B5	R/W(L)	Reserved	FEBE9	NEW	TUG3NEW	ROVFL	XSTAI	XISTAT	XPAIS
B6	R		LOVFL	RFRST	TFRST	VCXOLOC	TPLOC	RPLOC	OOL
B7	R/W(L)		LOVFL	RFRST	TFRST	VCXOLOC	TPLOC	RPLOC	OOL

Interrupt Mask Bits

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BA	R/W	DLOC	DLOJ1	BUSERR	E1AIS	LOP	PAIS	PSLERR	C2EQ0
BB	R/W	RDI	L3LOS	L3LOC	TOVFL	L3AIS	UPLOC	ALOC	ALOJ1
BC	R/W	HINT	FEBE9	NEW	TUG3NEW	ROVFL	XSTAI	XISTAT	XPAIS
BD	R/W		LOVFL	RFRST	TFRST	VCXOLOC	TPLOC	RPLOC	OOL

*R/W: Read/write; R: Read only; R/W(L): Read/Write - latched register.

Transmit POH Byte & O Bits

J1	B3 Error Mask and Test	C2	G1	F2	H4	Z3	Z4	Z5	Not used	O-bits
00-3F	40	41	42	43	44	45	46	47	48	49 Bits 1-0

Receive POH Bytes, TUG-3 H1/H2 Bytes & O Bits

J1	B3	C2	G1	F2	H4	Z3	Z4	Z5	H1	H2	O-bits
50-8F	90	91	92	93	94	95	96	97	98	99	9A Bits 1-0

Performance Counter & FIFO Leak

RCV Frame Count	Not used	FIFO Leak Rate	INC Count	DEC Count	New Count	TUG-3 INC Count	TUG-3 DEC Count
A0	A1	A2	A3	A4	A5	A6	A7

TUG-3 New Data Flag Count	B3 Block Error Count	FEBE Count	B3 Error Count	Line CV/ PRBS Error Count	Common High Byte (B3, FEBE, CVs)
A8	A9	AA AB	AC AD	AE AF	FF

ID

The manufacturer ID, part ID, mask level, and the revision level of the L3M is implemented with read only capability. The format is based on that which is specified in IEEE standard 1149.1 on boundary scan. The manufacturer ID is 107, and has been assigned by the Solid State Products Engineering Council (JEDEC). This field, 11 bits in length, plus parity, is assigned to bits 7 through 0 of F0, and bits 3 through 0 of F1. Bit 1 in F0 is assigned as a fixed parity bit by JEDEC. The part number field is 16 bits long. The part number for the L3M is 03452 in binary, and is assigned to bits 7 through 4 in F1, bits 7 through 0 in F2, and bits 3 through 0 in F3. Bit 4 in F1 is the LSB.

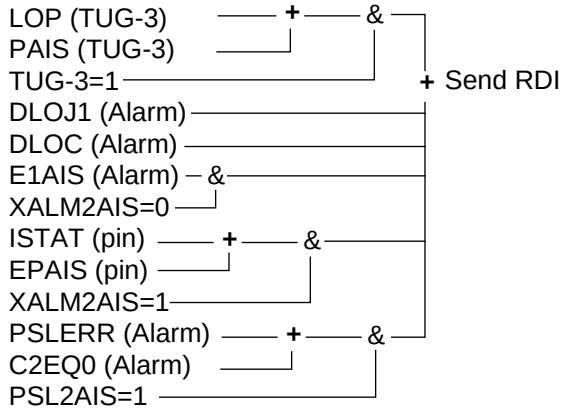
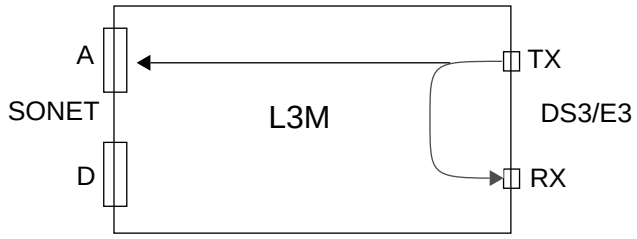
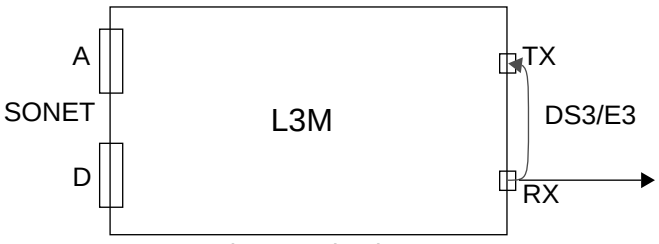
Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F4	R	Mask Level				Growth			
F3	R	Revision (Version) Level				0	0	0	0
F2	R	1	1	0	1	0	1	1	1
F1	R	1	1	0	0	0	0	0	0
F0	R	0	1	1	0	1	0	1	1

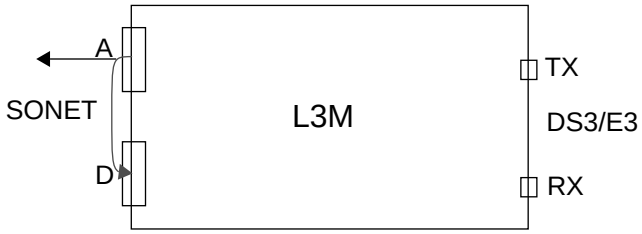
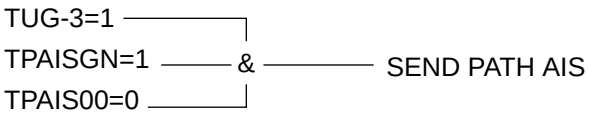
L3M REGISTER MEMORY MAP DESCRIPTIONS

Control Bits

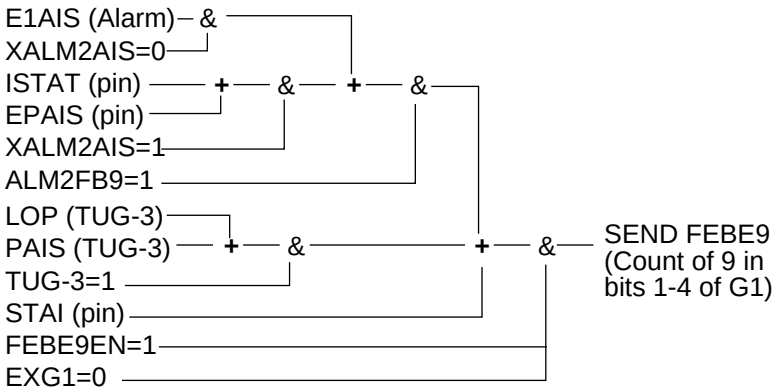
On power-up, the control bits will be a 1 or 0. The microprocessor must perform a read/write cycle to set the control bits to the required system status.

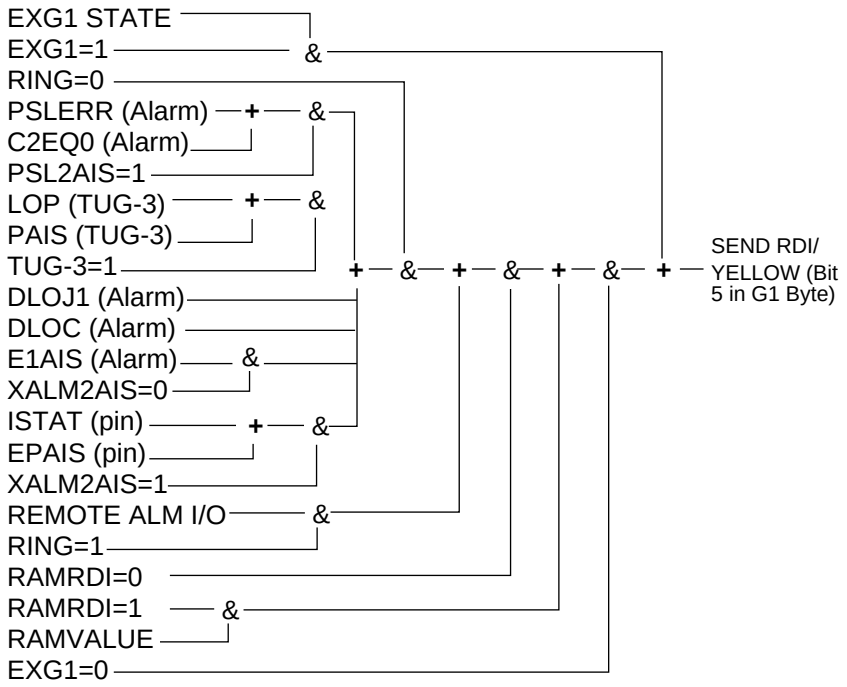
Address	Bit	Symbol	Description
C0	7-6	MAP1,0	**Mapping Control:** Determines the mappings according to the table given below: MAP1 MAP0 Map 0 0 STS-1 (DS3 Mapping) 0 1 STS-3 (DS3 Mapping) 1 0 STM-1 (Future use) 1 1 TUG-3 (E3 Mapping)
	5-4	DPOS1,0	**Drop Positions 1 and 0:** Determines the locations of the AUG-3/STS-SPEs and TUG-3s dropped from the STM-1/STS-3 according to the table given below: DPOS1 DPOS0 Mapping 0 0 CCITT position A (or STS-1 #1) 0 1 CCITT position B (or STS-1 #2) 1 0 CCITT position C (or STS-1 #3) 1 1 Undefined
	3-2	APOS1,0	**Add Positions 1 and 0:** Determines the locations of the AUG-3/STS-SPEs and TUG-3s to be added to the STM-1/STS-3 according to the table given below: APOS1 APOS0 Mapping 0 0 CCITT position A (or STS-1 #1) 0 1 CCITT position B (or STS-1 #2) 1 0 CCITT position C (or STS-1 #3) 1 1 Undefined
	1-0	FORM1,0	**Mode 1 and 0:** Determines the operating mode of the Mapper according to the table given below: MOD1 MOD0 Rate 0 0 E3 (34.368 Mb/s) X 1 DS3 (44.736 Mb/s) 1 0 Future use
C1	7	DECODE	**Transmit Decoder Enabled:** A 1 enables the transmit HDB3/ B3ZS decoder for rail operation. A 0 disables the decoder for NRZ operation.
	6	CODE	**Receive Coder Enabled:** A 1 enables the receive HDB3/B3ZS coder. A 0 disables the coder for NRZ operation.
	5	INVCI	**Invert Transmit Line Clock Input:** When written with a 0, the DS3 or E3 line signals are clocked into the L3M on positive transitions of the clock (TCLK). A 1 enables the line signal to be clocked into the L3M on negative transitions of the clock.

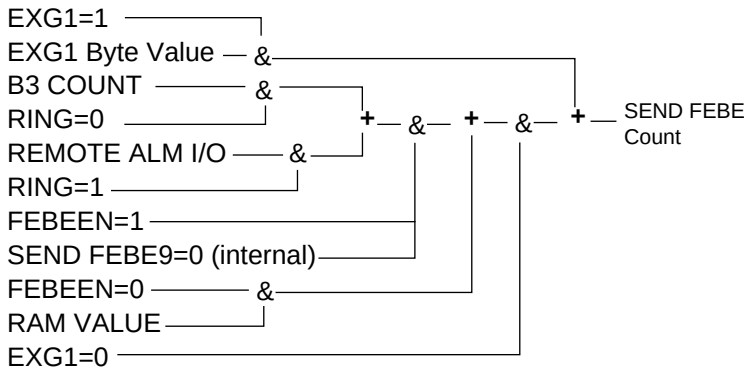
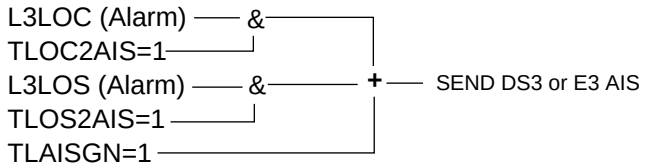
Address	Bit	Symbol	Description
C1	4	INVCO	**Invert Receive Line Clock Output:** When written with a 0, the DS3 or E3 line signals are clocked out of the L3M on negative transitions of the clock (RCLK). A 1 enables the line signal to be clocked into the Mapper on positive transitions of the clock.
	3	RING	**Ring Operating Mode:** A 1 enables the external alarm interface FEBE count and RDI alarm indication from another L3M to be transmitted in the G1 byte. This byte is overwritten if the external POH G1 byte is selected. The alarm conditions at the other L3M that may cause RDI are shown below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 
	v	FLBK	**Facility Loopback:** A 1 enables the transmit line data and clock signals to be looped back as the receive data and clock line signal.  Facility Loopback
	1	L3LBK	**Mapper E3/DS3 Loopback:** A 1 enables the receive line signal to be looped back as the transmit line signal. The receive data and clock are at the receive line interface.  Line Loopback

Address	Bit	Symbol	Description
C1	0	SLBK	**SONET Loopback:** A 1 enables the add SONET signal to be looped back as the drop signal. The drop signals from the bus are disabled, and add data and clock are at the bus interface. Valid only in the add timing and external timing modes.  SONET Loopback
C2	7	ALM2AIS	**External Alarm Enable AIS:** A 1 enables an AIS detected in an E1 byte (when control bit XALM2AIS = 0) or a high on either the ISTAT or PAIS leads (when control bit XALM2AIS = 1) to generate a line AIS in the receive direction when control bit RAISEN is a 1.
	6	ALM2FB9	**External Alarm Enable FEBE9:** A 1 enables an AIS detected in an E1 byte (when control bit XALM2AIS = 0) or a high on either the ISTAT or PAIS leads (when control bit XALM2AIS = 1) to generate a count of 9 in bits 1 through 9 of the transmitted G1 byte when control bit FEBE9EN is a 1.
	5	TLAISGN	**Generate Transmit Line AIS:** A 1 written into this position generates and transmits a DS3 or E3 AIS towards the SONET bus.
	4	TPAISGN	**Transmit Zeros or AIS Enable:** A 1 enables the Mapper to transmit an SPE with zeros (and valid pointer) or a TUG-3 AIS towards the SONET bus, depending on the state of TPAIS00. The logic diagram for sending path AIS is given below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 
	3	TPAIS00	**Transmit SPE with Zeros:** When enabled by writing a 1 to control bit TPAISGN, a 1 written into this location causes the SPE (POH bytes and payload) to be transmitted with zeros, but with a valid pointer. A 0 causes a TUG-3 AIS to be transmitted towards the SONET bus.
	2	TEST	**TranSwitch Test:** A 0 is normally written into this bit position.
	1	ADDZ	**Add Bus High Impedance Enable:** A 1 causes the Add bus data, and Add Parity bits to a high impedance state. When the external timing mode is selected, the clock, SPE, and C1J1 signals are also forced to a high impedance state.
	0	L3Z	**Receive Output High Impedance Enable:** A 1 forces the receive interface clock (RCLK) and data signals (RPOS and RNEG), and NRZ outputs (RNRZC and RNRZD) to a high impedance state.

Address	Bit	Symbol	Description
C3	7	EXZ5	**Transmit External Interface Z5 byte:** A 1 enables the Z5 byte from the POH I/O to be transmitted. A 0 enables the RAM location to be transmitted.
	6	EXZ4	**Transmit External Interface Z4 byte:** A 1 enables the Z4 byte from the POH I/O to be transmitted. A 0 enables the RAM location to be transmitted.
	5	EXZ3	**Transmit External Interface Z3 byte:** A 1 enables the Z3 byte from the POH I/O to be transmitted. A 0 enables the RAM location to be transmitted.
	4	EXH4	**Transmit External Interface H4 byte:** A 1 enables the H4 byte from the POH I/O to be transmitted. A 0 enables the RAM location to be transmitted.
	3	EXF2	**Transmit External Interface F2 byte:** A 1 enables the F2 byte from the POH I/O to be transmitted. A 0 enables the RAM location to be transmitted.
	2	EXG1	**Transmit External Interface G1 Byte:** A 1 enables bits 1 through 8 in the G1 byte from the POH I/O to be transmitted. A 0 enables the RAM location or internal logic/alarms to control the transmitted state of FEBE, RDI, and the unassigned bits.
	1	EXC2	**Transmit External Interface C2 Byte:** A 1 enables the C2 byte from the POH I/O to be transmitted. A 0 enables the RAM location to be transmitted.
	0	EXJ1	**Transmit External Interface J1 Byte:** A 1 enables the J1 byte from the POH I/O to be transmitted. A 0 enables the RAM segment to be transmitted.

Address	Bit	Symbol	Description
C4	7	EXOO	**External "O" Bit Select:** A 1 selects the two Overhead Communication Bits ("O" bits) from the external interface as the two "O" bits transmitted in each of the nine subframes of the DS3 format, instead of the RAM "O" bits.
	6	FEBE9EN	**FEBE9 Enable:** Enable bit for generating a FEBE count of 9. When EXG1 is a 0 and FEBE9EN is a 1, a FEBE count of 9 is generated when: - Either the ISTAT or PAIS input lead is a high, and the external alarm enable control bit XALM2AIS is a 1 and ALM2FB9 is 1; - An AIS is detected in the E1 byte, and XALM2AIS is 0 and ALM2FB9 is 1; - Either the TUG-3 PAIS or LOP alarms occur; - The STAI lead is a 1. The logic diagram for sending RDI is given below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 

Address	Bit	Symbol	Description
C4	5	RAMRDI	**Remote Defect Indication (Yellow alarm) Enabled:** Enable bit for controlling the generation of RDI (bit 5 in G1). When control bits RING and EXG1 are 0, and RAMRDI is a 0, RDI is generated when the following alarms or conditions occur: - Drop bus loss of J1 (DLOJ1) - Drop bus loss of clock (DLOC) - Loss of pointer (LOP) (TUG-3 operation) - Path AIS detected (PAIS) (TUG-3 operation) - Received E1 byte has a majority of 1s and control bit XALM2AIS is 0 - Either the ISTAT or PAIS input lead is a high and control bit XALM2AIS is a 1 - PSLERR or C2EQ0 alarm, and Path Signal Label Error Enable AIS control bit (PSL2AIS) is a 1 When control bit RING is a 1, EXG1 is a 0, and RAMRDI is a 0, the RDI state is controlled via the external alarm indication port. The microprocessor controls the RDI state when RAMRDI is a 1 and EXG1 is a 0. Note: writing a 1 to the RAMRDI bit will disable the local alarms and the alarm indication port RDI in the ring mode from controlling the state of the transmitted RDI bit. The logic diagram for sending RDI is given below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 

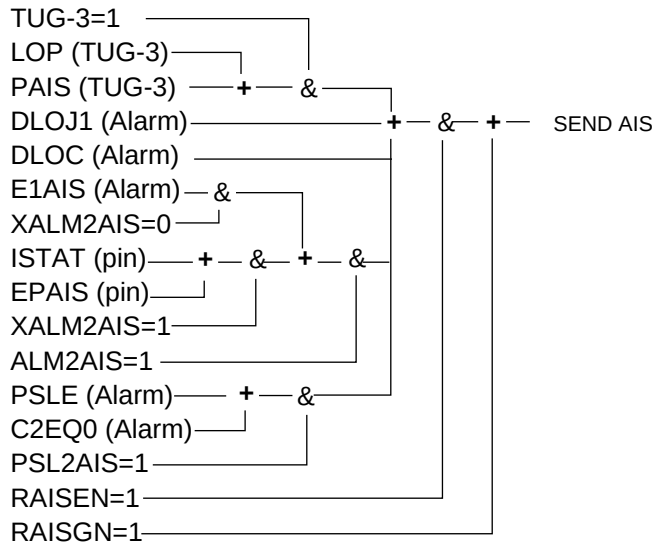
Address	Bit	Symbol	Description
C4	4	FEBEEN	**FEBE Enable:** A 1 enables the local B3 count or remote B3 count to be inserted as the FEBE count. A 0 written into this position permits the microprocessor to control the FEBE count. The logic diagram for sending FEBE for all conditions is given below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 
	3	XALM2AIS	**External Alarm AIS Pin Enable:** A 1enables the external alarm pins (ISTAT and PAIS) to function instead of detecting AIS in the E1 byte. A 0 disables the external alarm pins and enables the detection of E1AIS from the drop bus.
	2	TEST	**TranSwitch Test Mode:** A 0 is normally written into this bit position.
	1	TLOC2AIS	**Transmit Loss Of Clock (TLCK) AIS Enable:** A 1 enables the Mapper to automatically send DS3AIS or E3AIS when a transmit line clock failure is detected. The logic diagram for transmitting a line AIS is given below. The + symbol represents an or function, while & represents an and function. Control bit states are given by the = sign. 
	0	TLOS2AIS	**Transmit Loss Of Signal (TPOS/TNEG) AIS Enable:** A 1 enables the Mapper to automatically send DS3 or E3 AIS when a transmit line signal failure is detected.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="5">C5</td><td>7</td><td>COR</td><td>Clear On Read: A 0 enables all performance counters to become non-saturating with roll over capability. The contents of the counter is not affected by a read cycle. A 1 causes the performance counters to become saturating counters, with clear on read.</td></tr>
<tr><td>6</td><td>XVCXO</td><td>External VCXO Enabled: Writing a 1 into this location selects an external VCXO for the desynchronizer.</td></tr>
<tr><td>5</td><td>DROPT</td><td>Drop Bus Timing: Drop timing can only be selected when the L3M lead XCLKE is low. A 1 selects drop bus timing for the add bus. A 0 selects timing signals from the add bus.</td></tr>
<tr><td>4</td><td>POH2RAM</td><td>Path Overhead Bytes to RAM: Works in conjunction with the EXn control bits. The following table summarizes the action taken by this bit and an EXn bit.:

<table>
<tr><th>EXn (e.g., EXF2)</th><th>POH2RAM</th><th>Action</th></tr>
<tr><td>0</td><td>X</td><td>POH value written to RAM location by the microprocessor is transmitted.</td></tr>
<tr><td>1</td><td>0</td><td>POH interface byte transmitted, RAM location holds microprocessor written value.</td></tr>
<tr><td>1</td><td>1</td><td>POH interface byte transmitted and written to RAM location.</td></tr>
</table>
</td></tr>
<tr><td>3</td><td>RAISGN</td><td>Generate Receive Line AIS: A 1 written into this position generates a DS3/E3 AIS towards the line (RPOS, RNEG) independent of the state of the receive AIS enable bit (RAISEN).</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="3">C5</td><td>2</td><td>RAISEN</td><td>Receive AIS Enable: A 1 enables receive AIS to be generated when the following alarms/conditions occur:
- Loss of drop bus clock (DLOC)
- Loss of drop bus C1J1 (DLOJ1)
- E1 AIS (E1AIS) and XALM2AIS are 0, and ALM2AIS is a 1
- ISTAT or EPAIS and XALM2AIS are 1, and ALM2AIS is a 1
- Loss of pointer (LOP) (TUG-3)
- Path AIS (PAIS) (TUG-3)
- PSLERR or C2EQ0 occurs, and Path Signal Label Error Enable AIS control bit (PSL2AIS) is a 1

The logic diagram for generating receive line AIS is given below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign.

 
</td></tr>
<tr><td>1</td><td>WGDEC</td><td>Test Equipment BPV Selection: A 1 enables the decoder to detect coding violations as found in certain test equipment (e.g., Wandel & Goltermann™). A 0 enables the decoder to detect coding violations as found in other types of test equipment (e.g., Tberd™). The following table summarizes the two decoding procedures of coding violations:

<table>
<tr><th>BPV B3ZS</th><th>BPV HDB3</th><th>One Type of Test Equipment</th><th>Another Type of Test Equipment</th></tr>
<tr><td>++ or --</td><td>++ or - -</td><td>000 (preceding bit changed)</td><td>11</td></tr>
<tr><td>0BV or 000V</td><td>0BV or 000V</td><td>0000</td><td>1010 or 0001</td></tr>
<tr><td>BB0V after odd</td><td>BB00V after odd</td><td>1000</td><td>1101</td></tr>
<tr><td>BB0V after even</td><td>BB00V after even</td><td>1000</td><td>1001</td></tr>
</table></td></tr>
<tr><td>0</td><td>PSL2AIS</td><td>Path Signal Label Error Enable AIS: A 1 enables the Mapper to automatically send DS3 or E3 AIS towards the receive line, and path FERF when a PSLERR or C2EQ0 alarm occurs. (See RAMFERF and RAISEN for diagrams.)</td></tr>
</table>

Address	Bit	Symbol	Description
C6	7	FASTPTR	**Fast Pointer Enabled:** A 1 allows the Mapper to track pointer movements every frame instead of every other frame for TUG-3 operation.
	6	TOHOUT	**Transport Overhead Bytes Out:** A 1 enables the Mapper to generate the A1, A2, C1, and the H1H2 bytes, in the external timing mode (STS-1 mode) only. The H1 and H2 bytes are transmitted with a fixed pointer value 6800 hex.
	5	H4CTR	**H4 Counter Enable:** Normally written with a 0. A 1 enables the H4 byte to be transmitted with a count generated by an internal 8-bit frame counter.
	4	PAT23	**2^{23}-1 Test Pattern Enable:** A 0 selects the test pattern generator and analyzer to be 2^{15}-1. A 1 selects the pattern generator and analyzer to be 2^{23}-1.
	3	ENANA	**Enable Analyzer:** A 1 enables the 2^{15}-1or 2^{23}-1 analyzer. PRBS errors are counted in a 16-bit counter in locations AE and AF.
	2	TXANA	**Transmit Analyzer Enable:** A 1 enables the analyzer to sample the transmit NRZ line (DS3/E3) signal after the Decoder. A 0 causes the analyzer to sample the receive NRZ line data prior to the coder function. A 1 must be written into **ENANA** for this bit to function. (See Figure 29.)
	1	TPRBS	**Transmit Test Pattern Generator Enable:** A 1 enables the transmit test pattern generator and disables the NRZ decoder output.
	0	RPRBS	**Receive Test Pattern Generator Enable:** A 1 enables the receive test pattern generator and disables the NRZ coder input.

Address	Bit	Symbol	Description
C7	7	TESTB3	**Test B3 Byte:** A 1 transmits a B3 value written by the microprocessor in location 40 hex. A 0 enables the test byte to become a test mask. When configured as a test mask, a 1 in one or more bit positions causes those bits in the transmitted B3 byte to be inverted.
	6	FIXPTR	**TUG-3 Fixed Pointer Generation:** A 1 forces a fixed pointer of 0 to be generated in the transmitted TUG-3 regardless of any pointer movements (J1 in DC1J1) that may occur on the Drop side when the Drop timing mode is selected, or if a pointer movement (J1 in AC1J1) takes place when Add bus timing is selected.
	5	CCITT	**C2 Signal Label Mismatch, and Unequipped Detection Algorithm:** A 0 conditions the C2 signal label mismatch and unequipped state detection for 5 or more in a 50 ms period for an alarm, and for recovery. A 1 conditions the C2 signal label mismatch and unequipped state detection for 5 consecutive for an alarm, and for recovery.
	4	TEST	**TranSwitch Test Mode:** This bit position must be written with a 0.
	3	TEST	**TranSwitch Test Mode:** This bit position must be written with a 0.
	2	TXRST	**Transmit Reset:** A 1 written into this position resets the transmit section (Line to SONET/SDH) of the Mapper. This includes the transmit FIFOs and internal counters. The L3M transmitter shall remain reset until the processor writes a 0 into this location.
	1	RXRST	**Reset L3M:** A 1 written into this position resets the receive section (SONET/SDH to Line) of the Mapper. This includes the receive FIFOs and internal counters. The L3M receiver shall remain reset until the processor writes a 0 into this location.
	0	RSETC	**Reset Performance Counters:** A 1 written into this position resets all performance counters to 0. This bit is self clearing, and does not require the processor to write a 0 into this location.
C8	7-0	C2 Comp	**Path Signal Label Compare:** The bits in this location are written to by the microprocessor, and are compared against the C2 byte received for a signal label mismatch condition.
C9	7-0	TEST	**TranSwitch Test Mode:** This byte must be written with a 0.

Status Bits

Status bits report the condition of alarms. Unlatched bit positions (even addresses) provide access to transient alarm conditions. Latched bit positions (odd addresses) stay high until they are cleared by a read cycle.

Address	Bit	Symbol	Description
B0 & B1	7	DLOC	**Drop Bus Loss Of Clock Alarm:** An loss of clock alarm occurs when the input Drop clock is stuck high or low for 1000 ± 500 nanoseconds. Recovery occurs on the first clock transition.
	6	DLOJ1	**Drop Bus Loss of J1:** A 1 indicates that the J1 pulse is not present in the drop bus C1J1 signal or that eight new consecutive J1 locations have been detected.
	5	BUSERR	**Bus Parity Error:** A 1 indicates a parity error has been detected when the parity bit is compared against the parity calculation using the data, SPE and internal C1J1 signals. Other than providing this alarm, no other action is taken.
	4	E1AIS	**E1 Byte AIS Detected:** A 1 indicates that AIS has been detected in the E1 byte. Majority logic (5 out of 8 1s) is used for detection. The following alarms in the SOT-3/SOT-1 generate an E1 byte having an AIS indication: loss of frame, loss of signal, loss of pointer, and line AIS detected.
	3	LOP	**Loss Of Pointer Alarm:** Valid for TUG-3 pointer processing only. A loss of pointer alarm occurs when a New Data Flag (NDF) is detected, or an invalid pointer is detected for eight consecutive frames. Recovery occurs when a valid pointer is received for three consecutive frames.
	2	PAIS	**Path AIS Alarm:** Valid for TUG-3 pointer processing only. A Path Alarm Indication Signal (AIS) is detected when all ones are detected in the 16 bit pointer word (H1 and H2) for three consecutive frames. Recovery occurs when a valid NDF, or valid pointer is detected for three consecutive frames.
	1	PSLERR	**Path Signal Label Error:** A 1 indicates that the comparison between the received C2 byte and the microprocessor written C2 byte or an internal hardware value of 01 hex did not match.
	0	C2EQ0	**Received C2 value equal to 0:** A 1 indicates that the received C2 value was equal to 0

Address	Bit	Symbol	Description
B2 & B3	7	RDI	**Receive RDI (Yellow) Alarm:** A 1 indicates that bit 5 in G1 has been detected as a one for 10 consecutive frames. Recovery occurs when a 0 has been detected for 10 consecutive frames.
	6	L3LOS	**Mapper Transmit Loss Of Signal:** For an E3 signal, a loss of signal alarm occurs when the input NRZ data, or the positive/negative rail is stuck low for 256 bit times. Recovery occurs when there are at least 32 transitions (NRZ, or positive/negative rail) in a count of 256 clock cycles. For a DS3 signal, a loss of signal alarm occurs when the input NRZ data, or the positive/negative rail is stuck low for 200 bit times. Recovery occurs on the first transition (NRZ, or positive/negative rail).
	5	L3LOC	**Mapper Transmit Loss of Clock:** A 1 indicates the incoming line clock (TCLK) signal has been detected stuck high or low for 1000 ± 500 nanoseconds. Recovery occurs on the first transition.
	4	TOVFL	**Transmit FIFO Overflow/Underflow:** A 1 indicates that the transmit FIFO has either underflowed or overflowed. When this happens, the FIFO automatically resets to a preset position.
	3	L3AIS	**Mapper E3 Transmit AIS Detected:** For an E3 signal, AIS is detected when four or less zeros are detected in 1536 bits, twice in a row. Recovery occurs when there are five or more zeros detected in 1536 bits two consecutive times.
	2	RAMLOC	**Loss Of Microprocessor RAM Clock:** A 1 indicates that the RAM clock (RAMCI) has been detected stuck high or low for 1000 ± 500 nanoseconds. Recovery occurs on the first transition.
	1	ALOC	**Add Bus Loss Of Clock:** A loss of clock alarm occurs when the input add clock (ACLK) is stuck high or low for 1000 ± 500 nanoseconds. Recovery occurs on the first clock transition. When the add bus clock is an output, the external byte clock (XCLK1) is monitored for loss of clock, and is reported as this alarm.
	0	ALOJ1	**Add Bus Loss of J1:** A 1 indicates that the J1 pulse is not present in the add bus C1J1 signal.

Address	Bit	Symbol	Description
B4 & B5	7	SINT (B4 only)	**Software Interrupt:** A software interrupt indication occurs when one or more bit locations in the interrupt mask locations is written with a 1, and the corresponding alarm is detected. The SINT state is exited when the alarm causing the interrupt clears or its corresponding bit in the interrupt mask is cleared.
	6	FEBE9	**FEBE Count of 9 Indication:** An STS FEBE9 indication occurs when the code 1001 (count of 9) in bits 1-4 in the received G1 byte is detected for five consecutive frames. The alarm is terminated when any code other than the 1001 is detected in bits 1-4 for five consecutive frames.
	5	NEW	**New Alarm:** An indication that a new J1 location, other than those resulting from INC or DEC, has been detected.
	4	TUG3NEW	**TUG-3 New Alarm:** A TUG-3 new indication occurs when three consecutive new pointers, or an NDF and a match of the SS bits and the pointer offset value is in range has been detected.
	3	ROVFL	**Receive FIFO Overflow/Underflow:** A 1 indicates an underflow or overflow condition in the receive direction (SONET/SDH to line). When this happens, the FIFO will automatically reset to a preset position.
	2	XSTAI	**SONET Network Alarm Indication:** A 1 indicates that the input on the lead labeled STAI is high.
	1	XISTAT	**External STS-1 Alarm:** A 1 indicates that the input on the lead labeled ISTAT is a high. A 1 is equal to an external alarm condition (e.g., LOP).
	0	XPAIS	**External Path AIS:** A 1 indicates that the input on the lead labeled PAIS is a high. A 1 is equal to an external alarm condition (e.g., PAIS).
B6 & B7	6	LOVFL	**Leak FIFO Overflow/Underflow Alarm:** A 1 indicates that the leak FIFO has underflowed or overflowed. When this occurs, the FIFO will automatically reset to a preset position.
	5	RFRST	**Receive FIFO Reset Indication:** A 1 indicates that the receive FIFO has been reset. This may occur because of a FIFO overflow/underflow alarm, or the receive section has been reset by writing a 1 to control bit RXRST.
	4	TFRST	**Transmit FIFO Reset Indication:** A 1 indicates that the transmit FIFO has been reset. This may occur because of a FIFO overflow/underflow alarm, or the transmit section has been reset by writing a 1 to control bit TXRST.
	3	VCXOLOC	**Loss of VCXO Clock:** A 1 indicates that the internal VCXO clock, or the external clock has been detected stuck high or low for 1000 $\pm$ 500 nanoseconds. Recovery occurs on the first transition.
	2	TPLOC	**Loss of Transmit PLL Clock:** A 1 indicates that the internal PLL clock has been detected stuck high or low for 1000 $\pm$ 500 nanoseconds. Recovery occurs on the first transition.
	1	RPLOC	**Loss of Receive PLL Clock:** A 1 indicates that the internal PLL clock has been detected stuck high or low for 1000 $\pm$ 500 nanoseconds. Recovery occurs on the first transition.
	0	OOL	**Analyzer Out of Lock:** A 1 indicates that the analyzer, when enabled, is out of lock.

Interrupt Mask Bits

A 1 written to any of the bits in the interrupt mask (except HINT), and the occurrence of the corresponding alarm, causes a software interrupt (SINT) to occur. If the hardware interrupt bit (HINT) is also written with a 1, then a hardware interrupt also occurs.

Address	Bit	Symbol	Description
BA	7	DLOC	Drop Bus Loss Of Clock
	6	DLOJ1	Drop Bus Loss of J1
	5	BUSERR	Received Parity Error
	4	E1AIS	Drop E1 Byte AIS detected
	3	LOP	Loss Of Pointer (TUG-3 operation)
	2	PAIS	Path AIS (TUG-3 operation)
	1	PSLERR	Path Signal Label Error
	0	C2EQ0	C2 Equal to 0 alarm
BB	7	RDI	Receive RDI (yellow) detected. Bit 5 in G1
	6	L3LOS	Transmit Line Loss Of Signal
	5	L3LOC	Transmit Line Loss Of Clock
	4	TOVFL	Transmit FIFO Error (underflowed or overflowed)
	3	L3AIS	E3 Transmit Line AIS Detected
	2	UPLOC	Microprocessor Loss Of Clock (RAMC lead)
	1	ALOC	Add Bus Loss Of Clock
	0	ALOJ1	Add Bus Loss of J1
BC	7	HINT	Hardware Interrupt Enable
	6	FEBE9	Count of 9 in G1
	5	NEW	NDF and 3x new pointer events (TUG-3 operation)
	4	TUG3NEW	Three new pointer events
	3	ROVFL	Receive FIFO Overflow/Underflow
	2	XSTAI	SONET Network Alarm Indication
	1	XISTAT	External ISTAT signal detected as a 1 (if enabled)
	0	XPAIS	External PAIS signal detected as a 1 (if enabled)

Address	Bit	Symbol	Description
BD	6	LOVFL	Leak FIFO Overflow/Underflow
	5	RFRST	Receive FIFO Reset Indication
	4	TFRST	Transmit FIFO Reset Indication
	3	VCXOLOC	VCXO Loss Of Clock
	2	TPLOC	Transmit PLL loss of clock
	1	RPLOC	Receive PLL loss of clock
	0	OOL	Analyzer out of lock.

Transmit Path Overhead Bytes and O-bits

The Path Overhead bytes consists of the J1, B3, C2, G1, F2, H4, Z3, Z4, and the Z5 bytes. The POH bytes may be individually transmitted from the POH interface, or from RAM location written by the microprocessor. When POH2RAM is a 1, the POH interface byte selected for transmission shall be written into the common RAM location as transmitted. For example, if EXC2 is written with a 1, the received POH interface C2 byte is written into the assigned RAM location, in addition to being transmitted. If EXC2 is written with a 0, the transmitted byte is the value written into the RAM location by the microprocessor. When a 0 is written into the POH2RAM control bit, the L3M disables the capability of writing any of the selected POH interface bytes into their RAM locations. However, individual bytes may still be transmitted from either the POH interface or the microprocessor written RAM location. This feature permits you to switch back and forth between a selected POH interface byte or a RAM location for transmission, without having to reinitialize the RAM location. The following table is a summary of this operation:

POH2RAM	EXnn	Action
1	1	POH interface byte written into RAM, and also transmitted.
0	1	POH interface byte transmitted, but not written into RAM. Microprocessor writes RAM value as required.
X	0	POH RAM value transmitted.

The relationship between a transmitted Path Overhead byte and the corresponding RAM location is as follows:

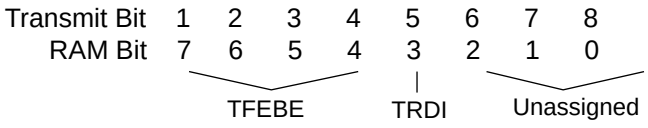
RAM Location

7	6	5	4	3	2	1	0

Transmitted POH Byte

1	2	3	4	5	6	7	8

The O-bits consists of two overhead communication bits per subframe, for nine subframes, in the DS3 format. The selection of the two bits per subframe either from the O-bit interface or from RAM operates in the same way as the Path Overhead bytes.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>00
to
3F</td><td>7-0</td><td>J1</td><td>Path Trace: The bytes written into this location provide a repetitive 64 byte fixed length message for transmission. The bytes written into these positions are either from the microprocessor or from the external POH I/O.</td></tr>
<tr><td>40</td><td>7-0</td><td>B3
Error
Mask</td><td>B3 Error Mask: When control bit TESTB3 is a 0, the bit columns written with a one represent the columns in the B3 byte in which errors are generated. The B3 errors are sent until this position is rewritten with a 00H. When control bit TESTB3 is a 1, the value written into this location is the transmitted B3 byte.</td></tr>
<tr><td>41</td><td>7-0</td><td>C2</td><td>Path Signal Label (processor): The bits written into this position indicate the construction of the AUG-3, TUG-3, or SPE.</td></tr>
<tr><td>42</td><td>7-0</td><td>G1</td><td>Transmit Byte G1: This byte is used for sending the microprocessor controlled states for FEBE, RDI, and the unassigned bits, according to states given in the tables below:
FEBE<table><tr><th>EXG1</th><th>FEBEEN</th><th>Action</th></tr><tr><td>0</td><td>0</td><td>Send microprocessor written value</td></tr><tr><td>0</td><td>1</td><td>Internal or mate (ring mode) value sent</td></tr><tr><td>1</td><td>X</td><td>Sent external POH value</td></tr></table>RDI<table><tr><th>EXG1</th><th>RAMRDI</th><th>Action</th></tr><tr><td>0</td><td>0</td><td>Internal or mate (ring mode) value sent</td></tr><tr><td>0</td><td>1</td><td>Send microprocessor written value</td></tr><tr><td>1</td><td>X</td><td>Sent external POH value</td></tr></table>Unassigned Bits<table><tr><th>EXG1</th><th>Action</th></tr><tr><td>0</td><td>Send microprocessor written value</td></tr><tr><td>1</td><td>Sent external POH value</td></tr></table> 
</td></tr>
<tr><td>43</td><td>7-0</td><td>F2</td><td>User Channel: This location provides microprocessor or I/O written information between elements.</td></tr>
<tr><td>44</td><td>7-0</td><td>H4</td><td>H4 Channel: This byte is not used in this mapping, and should be written with 0s by the microprocessor or I/O.</td></tr>
</table>

Address	Bit	Symbol	Description
45 46 47	7-0	Z3 Z4 Z5	**Path Growth:** These bytes are reserved for future growth.
48	7-0		Not used.
49	7-2		Not used.
	1 0	TO2 TO1	**Transmit "O" Bits:** These two bits correspond to the two "O" bits found in each of the nine subframes in the DS3 format. The O-bits are read once per frame and inserted into each of the subframes.

Receive Path Overhead Bytes, H1/H2 bytes and O-bits

The received bytes are written into the locations given below, and are also provided at the receive Path Overhead byte interface.

The relationship between a received Path Overhead byte and the corresponding RAM location is the following:

RAM Location:

7	6	5	4	3	2	1	0

Received POH Byte:

1	2	3	4	5	6	7	8

Address	Bit	Symbol	Description
50 to 8F	7-0	J1	**Path Trace:** The received J1 bytes are written in the 64 byte segment in a rotating fashion. There is no specific starting point.
90	7-0	B3	**Path B3:** The value in this location is the received B3 parity byte.
91	7-0	C2	**Path Signal Label:** The bits indicate the construction of the AU-3, TUG-3, or SPE (e.g. unequipped).
92	7-0	G1	**Receive Byte G1:** This location provides the receive status of the FEBE bits, Path RDI, and unassigned bits in the G1 byte. Receive Bit 1 2 3 4 5 6 7 8 RAM Bit 7 6 5 4 3 2 1 0 FEBE RDI Unassigned
93	7-0	F2	**User Channel:** This location provides user information between elements.
94	7-0	H4	**H4 Byte:** This byte is not specified for use in this application. It is provided for future use as required.

Address	Bit	Symbol	Description
95 96 97	7-0	Z3 Z4 Z5	**Path Growth:** These bytes are used for future growth.
98 99	7-0	H1 H2	**Received H1 and H2 Pointer:** The contents of the H1 and H2 pointer for a TUG-3 are provided in the following bit order for a microprocessor read cycle. H1 H2 Bit 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 N N N N S S I D I D I D I D I D
9A	1 0	RO2 RO1	**Receive "O" Bits:** The received states of the two Overhead Communication channel bits found in the DS3 format. The two bits are updated once a frame from one of the subframes in the frame.

Performance Counters

All 16-bit performance counters have a special 16-bit read operation which allows uninterrupted access, without the danger of one byte changing while the other byte is read. To perform a 16-bit read, the low order byte is read first. This causes the internal count to be transferred to a common high order byte at location 0xFF. The high order byte should be read next. If another performance counter low order byte is read, the contents of the higher order byte will reflect the performance counter just read. Counts that occur during the read cycle are held with the counter to be updated afterwards. All the performance counters can also be configured to be either saturating or non-saturating. When a 1 is written to control bit **COR** (clear on read), the performance counters are configured to be saturating, with the counters stopping at their maximum count. An 8-bit or 16-bit counter is reset on a microprocessor read cycle. When a 0 is written to control bit **COR**, the performance counters are configured to be non-saturating, and roll over to zero after the maximum count in the counter is reached. All the performance counters can be reset simultaneously by writing a 1 to control bit **RSETC**. This bit is self clearing, and does not require writing a 0 into this location.

All drop bus related performance counters are inhibited (i.e., will not increment) when one or more of the following alarms occurs:

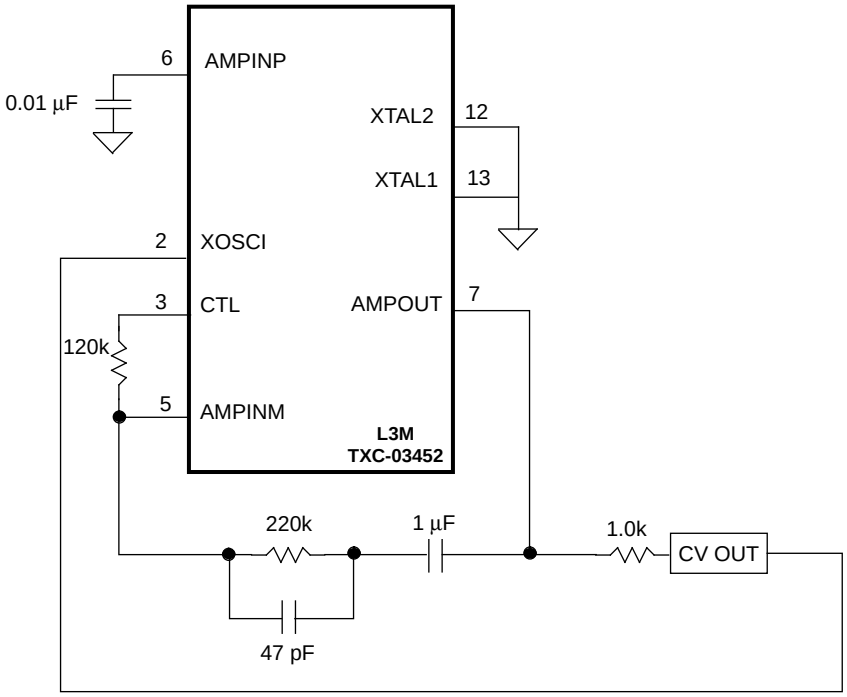
- Loss of drop bus clock (DLOC)
- Loss of drop bus J1 (DLOJ1)
- AIS detected in the E1 byte (when XALM2AIS = 0)
- When either ISTAT or PAIS lead is high (when XALM2AIS = 1)
- Loss of pointer (TUG-3)
- Path AIS (TUG-3)

The performance counters can also be written by the microprocessor. However, when writing to a 16-bit counter (at location n) it is recommended that the low byte be written first. The high order byte can be written by addressing location n + 1. Since the writes occur in separate cycles, care must be taken to prevent the low byte from carrying-out to the high byte before the high byte is initialized. Writing a low byte equal to 00 hex will provide the maximum time for the microprocessor to update the high byte.

Address	Bit	Symbol	Description
A0	7-0	Rcv Frame Cnt	**Receive SONET Frame Count:** Counts the number of receive SONET frames.
A2	7-0	FIFO Leak Rate	**FIFO Leak Rate Register:** The number written into this location represents the number of frames between leaked bits, modulo 32. Therefore, a value of one means that there are 32 frames between bit leaks. In addition, a value of zero may be used as a test case and causes bits to be leaked every other frame, when necessary.
A3	7-0	INC Count	**Positive Justification Counter:** Counts the number of positive (increment) pointer movements in the AUG/VC-4/STS-3/STS-1 based on J1 movements.
A4	7-0	DEC Count	**Negative Justification Counter:** Counts the number of negative (decrement) pointer movements in the AUG/VC-4/STS-3/STS-1 based on J1 movements.
A5	7-0	New Count	**New Data Flag (NDF) Counter:** Counts the number of J1 movements for the AUG/VC-4/STS-3/STS-1.
A6	7-0	TUG-3 INC Count	**TUG-3 Positive Justification Counter:** Counts the number of positive (increment) pointer movements in the TUG-3, based on interpretation of H1 and H2.
A7	7-0	TUG-3 DEC Count	**TUG-3 Negative Justification Counter:** Counts the number of negative (decrement) pointer movements in the TUG-3, based on interpretation of H1 and H2.
A8	7-0	TUG-3 New Count	**TUG-3 New Data Flag (NDF) Counter:** Counts the number of New Data Flags (NDFs) or new pointers in the TUG-3 pointer (H1).
A9	7-0	B3 Block Count	**B3 Blocks (in error) Counter:** Counts the number of B3 blocks which are received in error.
AA AB	7-0	FEBE Count	**Far End Block Error Counter:** Counts the FEBE error count indication received in bits 1 through 4 of G1. Location AA is the low order byte, while location AB is the high order byte of the 16-bit counter.
AC AD	7-0	B3 Counter	**B3 Error Counter:** Counts the number of B3 errors that occur between the incoming value and calculated value. Location AC is the low order byte, while location AD is the high order byte of the 16-bit counter.
AE AF	7-0	Coding Errors	**HDB3/B3ZS Coding Error Counter:** Counts the number of internal coding violation errors detected, or external coding violations present on the TNEG lead when the input line signal is NRZ. Location AE is the low order byte while location AF is the high order byte of the 16-bit counter. When control bit ENANA is written with a 1, PRBS errors are counted when the internal analyzer is in lock (no OOL alarm).
FF	7-0	Count	**Common High Order Byte:** This location contains the high order byte associated with the low order byte of the 16-bit counter that was most recently read.

VCXO

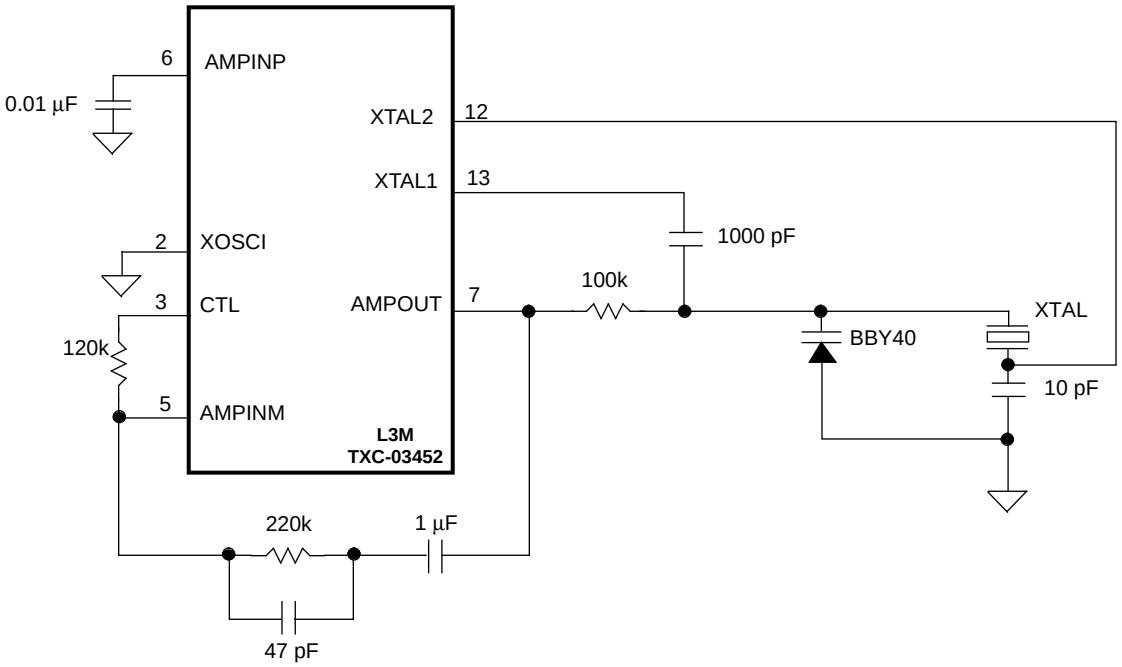
External VCXO operation is enabled by writing a 1 to control bit 6 (XVCXO) in location C5 hex. The schematic for the external VCXO components and connection to the L3M is shown in Figure 27 below. The two crystals pins (XTAL2 and XTAL1) are grounded.



Note: All resistors are 5%, 1/4 watt.

Figure 27. L3M External VCXO Connections

Internal VCXO operation is enabled by writing a 0 to control bit 6 (XVCXO) in location C5 hex. The schematic for the internal VCXO components and connections to the L3M is shown in Figure 28 below. Pin 2 (XOSCI) on the L3M is grounded.



Note: All resistors are 5%, 1/4 watt.

Figure 28. L3M VCXO Connections

TESTING

Loopbacks

Three loopback capabilities are provided: facility, line, and SONET. Writing a 1 to control bit FLBK enables facility loopback. Facility loopback and line loopback operations are shown in Figure 29. When facility loopback is enabled, the internal transmit NRZ signal becomes the internal receive NRZ signal. Either interface may be used, Rail or NRZ.

Line loopback is enabled by writing a 1 to control bit L3LBK. The receive output becomes the transmit line input. The receive output may be Rail or NRZ.

Writing a 1 to control bit SLBK enables a SONET loopback. SONET loopback disables the STM-1/STS-3/STS-1 signal input on the drop bus, and enables the add signals to become the drop bus signals. The add signals are provided at the add bus.

Test Generators and Analyzers

Two pseudo-random test generators are provided. Each generator can provide a 2^{15}-1 or 2^{23}-1 pseudo-random pattern. The test sequence of 2^{23}-1 is selected when a 1 is written into control bit PAT23.

The transmit test generator is enabled by writing a 1 to control bit TPRBS. When enabled, the transmit test generator transmits the pseudo-random pattern in place of transmit NRZ data.

The receive test generator is enabled by writing a 1 to control bit RPRBS. When enabled, the receive test generator inserts the pseudo-random test pattern in place of the received desynchronized NRZ data.

The test analyzer is enabled by writing a 1 to control bit ENANA. The test sequence of 2^{23}-1 is selected when a 1 is written into control bit PAT23. Receive NRZ data is analyzed when a 0 is written to control bit TXANA. When a 1 is written to control bit TXANA, the transmit NRZ data path is monitored. The selection of the test analyzer disables the decoder CV output to the 16-bit counter. The 16-bit counter now counts received errors from the test analyzer, when the analyzer is in lock.

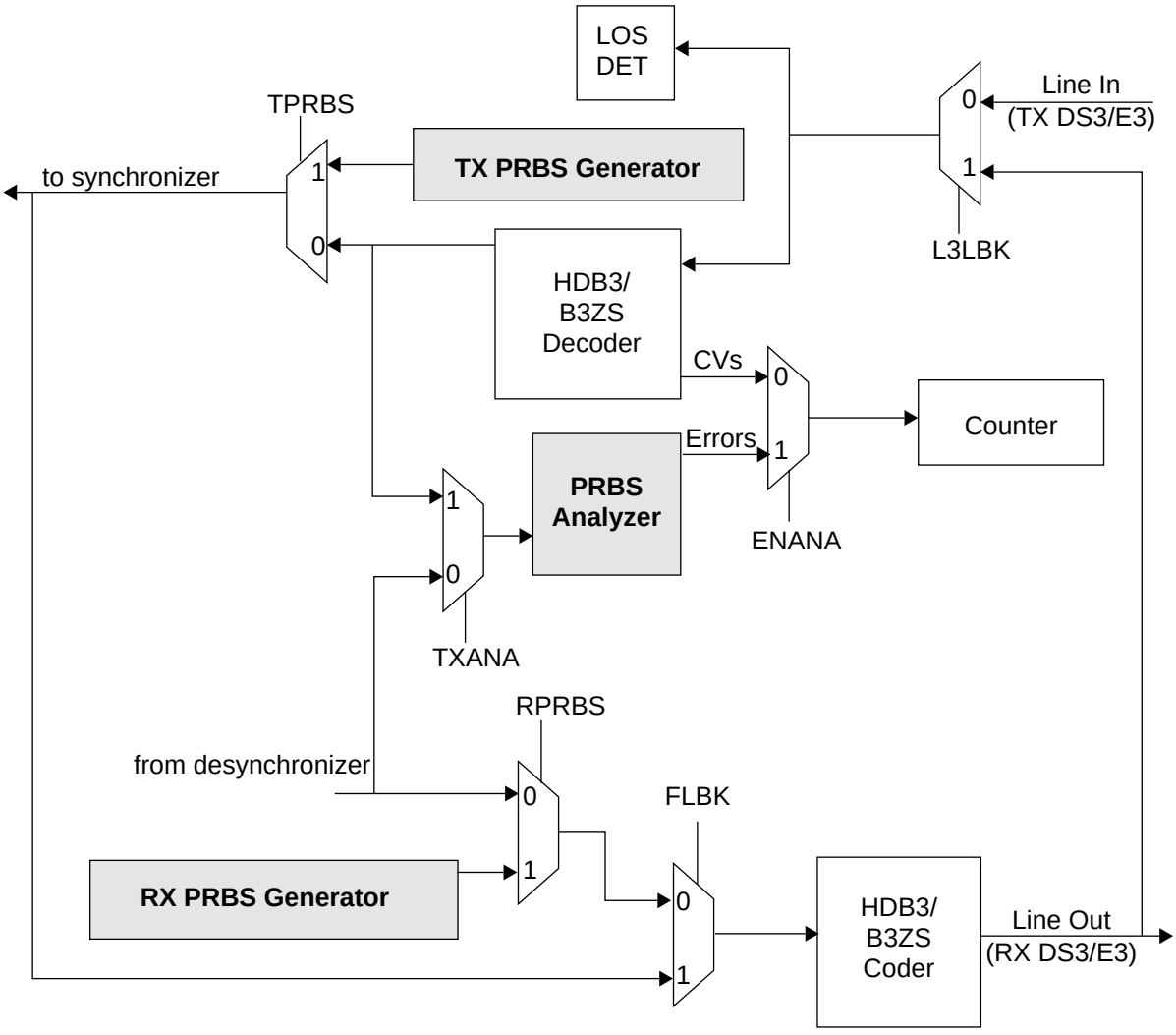


Figure 29. Loopbacks, Test Generator & Analyzers

PACKAGE INFORMATION

The L3M device is packaged in a 144-pin plastic quad flat pack suitable for socket or surface mounting. All dimensions shown are in millimeters and are nominal unless otherwise noted.

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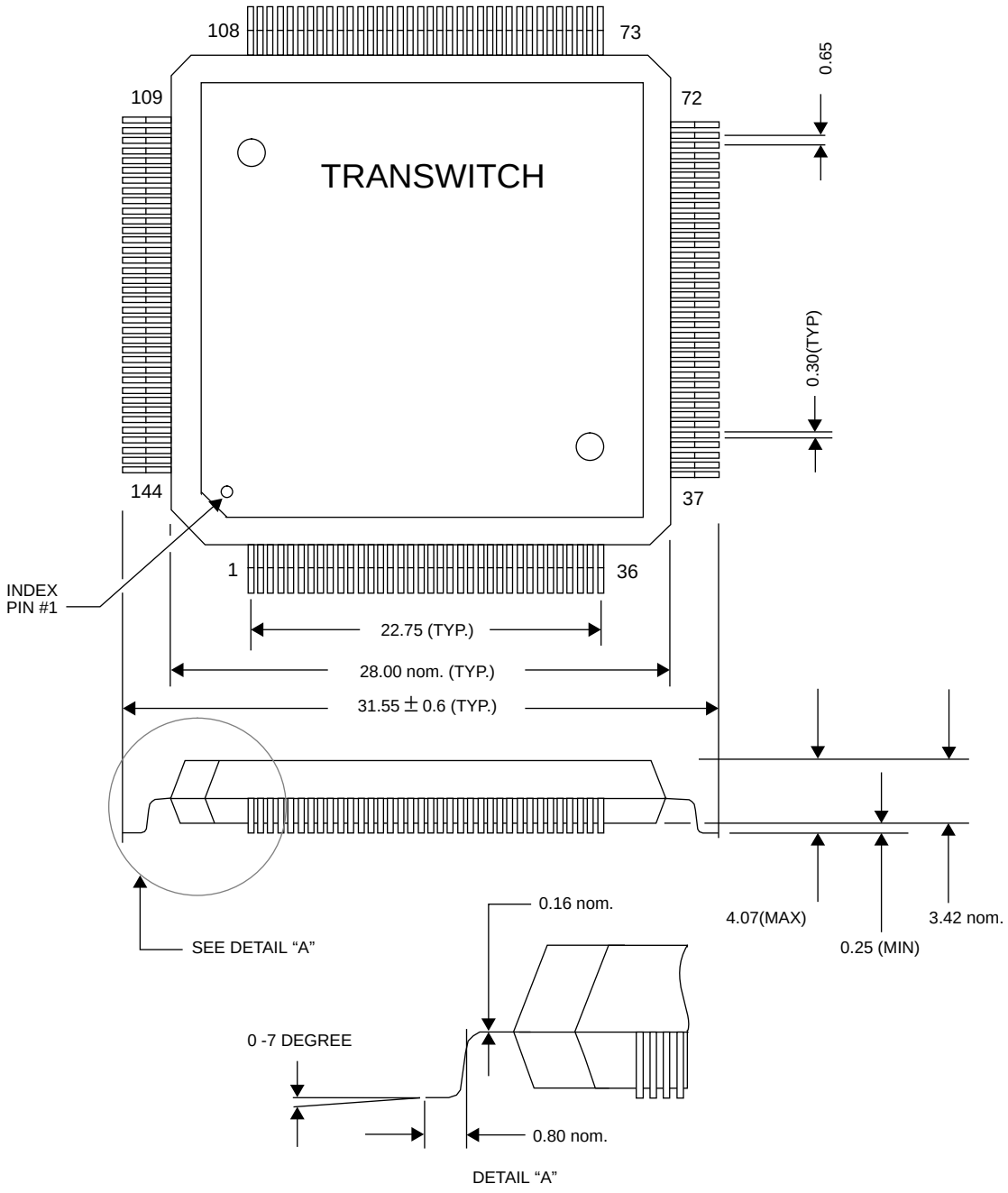


Figure 30. L3M 144-Pin Plastic Quad Flat Pack

ORDERING INFORMATION

Part Number:	TXC-03452-AIPQ	Plastic 144-Pin Quad Flat Pack

RELATED PRODUCTS

TXC-02301, SYN155 VLSI Device (155-Mbit/s Synchronizer, Data Output). Transmits and receives at STS-3/STM-1 rates. Provides the complete STS-3/STM-1 frame synchronization function. Connects directly to optical fiber interface components.

TXC-02302, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). This device is similar to the SYN155. It has both clock and data outputs on the line side.

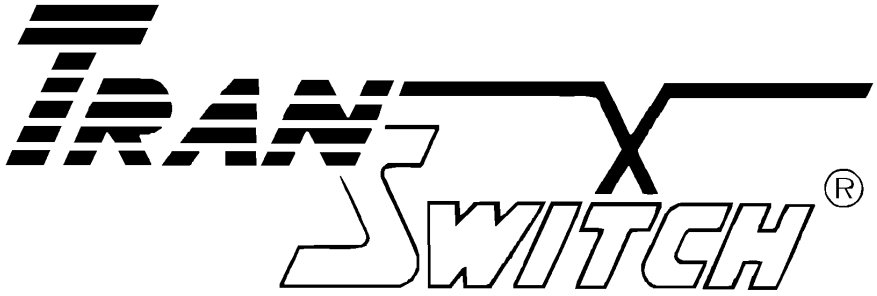
TXC-03001, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). This device performs section, line and path overhead processing for STS-1 SONET signals. Has programmable STS-1 or STS-N modes.

TXC-03003, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This device performs section, line and path overhead processing for STM-1/STS-3/STS-3c signals. Compliant with ANSI and CCITT standards.

LIST OF DATA SHEET CHANGES

The Edition 2 of the Data sheet is the first released edition of this Data Sheet. The draft Edition 1 (not released) was used for internal TranSwitch purposes.

Starting with the next edition of this Data Sheet, this section will list the changes made to the Data Sheet.



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