E123MUX Device
E1/E2/E3 MUX/DEMUX
TXC-03361

DATA SHEET

FEATURES

- E1 (2048 kbit/s) multiplexer/demultiplexer for ITU-T Recommendations:
  G.742 (8448 kbit/s E2 frame format)
  G.751 (34368 kbit/s E3 frame format)
- Multiplexer/demultiplexer converts:
  16 E1s to/from 1 E3 (E13 skip mux), or
  16 E1s to/from 4 E2s, or
  4 E2s to/from 1 E3 (E12/E23 split mux)
- Counters for bipolar violations, frame errors and loss of frame conditions
- E1 digital phase-locked loop circuits with bypass option
- Test features:
  PRBS generator and analyzer for E1 channels
  Local/Remote Loopbacks for E1, E2 or E3 channels
  Corrupt frame generation for E2 and E3 frames
- E2 and E3 bit error rate indications
- E1 and E3 line side interfaces are selectable as positive and negative rail or NRZ with external loss of signal indication on negative input pin.
- Microprocessor input/output bus provides multiplexed, Intel or Motorola interfaces
- Test access port for boundary scan
- Single +5 volt, ±5 % power supply
- 208-pin plastic quad flat package

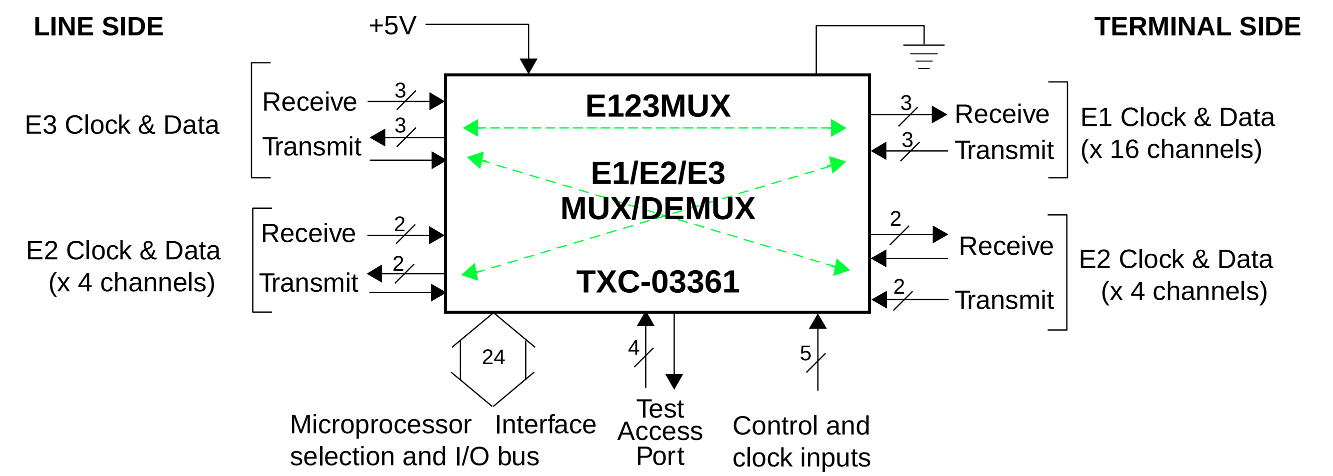
DESCRIPTION

The E123MUX is a CMOS VLSI device that provides the E13 functions needed to multiplex and demultiplex 16 independent E1 signals to and from an E3 signal that conforms to the ITU-T G.751 Recommendation. The E1 and E3 signal interfaces can be either dual unipolar (rail) or NRZ. Digital phase-locked loop circuits are provided for the received E1 signals, but they may be bypassed.

The E123MUX can also be configured to operate as an E12 or E23 multiplexer and demultiplexer. Sixteen E1 signals can be multiplexed and demultiplexed to and from four E2 signals that conform to the ITU-T G.742 Recommendation. Alternatively, four E2 signals can multiplexed and demultiplexed to and from one E3 signal. The E2 signal interfaces are NRZ only. The E123MUX uses memory locations for setting control bits and reporting status information. The status bits have maskable interrupt control bits.

APPLICATIONS

- Single-board E13 multiplexer
- Compact add/drop multiplexer
- DCS and EDSX systems
- CSU/DSU equipment



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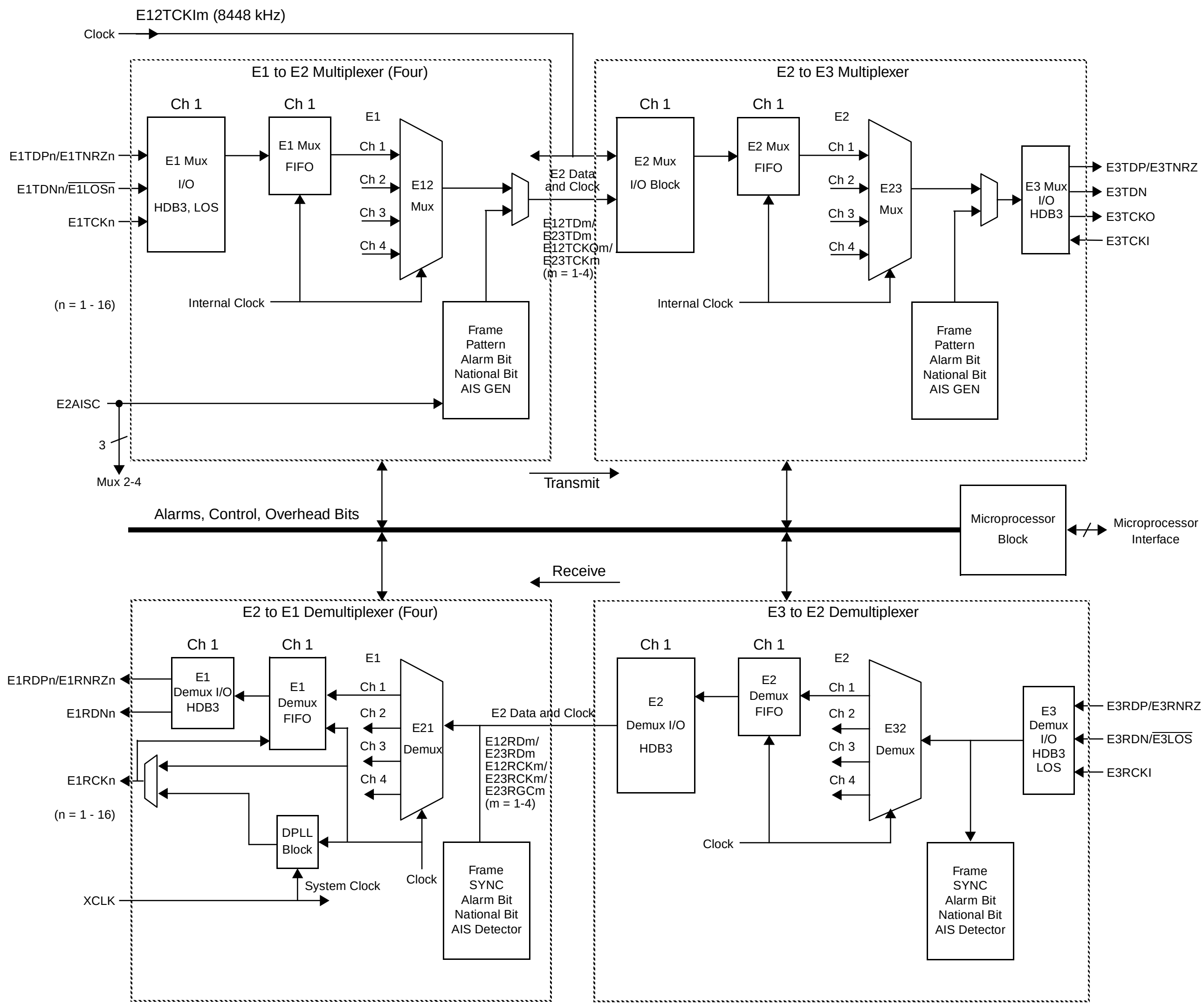
BLOCK DIAGRAM



Note: Test Access Port block and Microprocessor Interface lead details are not shown. Please refer to Pin Descriptions section.

Figure 1. E123MUX TXC-03361 Block Diagram

BLOCK DIAGRAM DESCRIPTION

Figure 1 shows a simplified block diagram of the E123MUX and its signal leads. In the transmit direction (multiplexer direction), the E123MUX multiplexes 16 independent asynchronous E1 signals operating at 2048 kbit/s into four separate E2 signals operating at 8448 kbit/s. The E1 transmit signal inputs can be in either the dual rail unipolar HDB3 format (E1TDPn and E1TDNn) or in the NRZ format (E1TNRZn). The rail/NRZ interface selection is common to both the multiplexer and demultiplexer sections of the chip. The clock edge for clocking in the data is programmable for either clock (E1TCKn) edge. When the rail interface is selected, the E1 rail signal interface is monitored for loss of signal using the detect and recovery requirements specified in ITU-T Recommendation G.775. Loss of signal status information is provided along with a maskable interrupt. In addition, bipolar violations (BPVs) are counted in 16-bit counters provided for each of the E1 channels. When the NRZ interface is selected for an E1 channel, an external loss of signal indication from the external line interface unit can also be provided as an input to the E123MUX on the lead designated as E1TDNn/$\overline{\text{E1LOSn}}$, to provide status information and a maskable interrupt for the microprocessor.

Four E1 framed or unframed asynchronous channels operating at 2048 kbit/s are multiplexed into one E2 signal, using the frame format specified in ITU-T recommendation G.742. The G.742 format consists of the 848 bits, starting with bit 1 in the frame alignment. The frame alignment pattern is defined as 1111010000. Bit 11 is defined as a remote alarm, and bit 12 is defined as a spare bit. The remaining bits carry tributary bits and justification control bits.

The four E12 multiplexers are numbered 1 through 4. Microprocessor access is provided in the transmit direction in each of the four E1 frame formats for controlling the states of the remote alarm indication bit (bit 11) and the spare bit (bit 12). Continuous framing errors may also be inserted into each of four frame formats.

The output of the four E12 multiplexers is connected internally to the E23 multiplexer section when the device is configured for E13 operation. The E2 multiplexed data and clock for the four E12 channels is not provided as an interface in this mode. However, an external 8448 kHz clock is required to be connected to the E12TCKIm input for clocking data out from the E12 multiplexer. The E23 section multiplexes each of the four E2 frames into a single E3 signal using the format specified in ITU-T recommendation G.751. The G.751 format consists of the 1536 bits, starting with bit 1 in the frame alignment. The frame alignment pattern is defined as 1111010000. Bit 11 is defined as a remote alarm, and bit 12 is defined as a spare bit. The remaining bits carry tributary bits and justification control bits. A 34368 kHz input clock (E3TCKI) is used to derive the output E3 clock (E3TCKO), which is used to clock out the E3 data. Microprocessor access is provided for controlling the states of the remote alarm indication bit (bit 11) and the spare bit (bit 12) in the E3 frame format. Continuous framing errors may also be inserted into the frame format. The output of the E23 multiplexer can be configured to be either a dual unipolar HDB3 signal or an NRZ signal. The control bit for selecting the HDB3 or NRZ format is common to the demultiplexer (receive direction). Data (E3TDP/E3TNRZ and E3TDN) is clocked out of the E123MUX using the E3 clock (E3TCKO) signal, which is derived from the E3 input clock (E3TCKI). A control bit is provided for clocking out the data on either clock edge.

In the receive direction (demultiplexed direction) from the E3 line, HDB3 or NRZ data (E3RDP/E3RNRZ and E3RDN/$\overline{\text{E3LOS}}$) is clocked into the E123MUX using the E3 clock (E3RCKI) signal. The clock edge employed can be programmed using the microprocessor. The E23 demultiplexer monitors the incoming signal for loss of signal using the requirements specified in ITU-T recommendation G.775. Bipolar violations are counted in a 16-bit counter. In addition, the E123MUX detects frame alignment using the requirements specified in the G.751 recommendation, and monitors the line signal for AIS. Besides providing status bits for LOS, AIS, and LOF, both framing errors and loss of frame events are counted in 8-bit counters. The status bits have maskable interrupt control bits for enabling and disabling the interrupt for the microprocessor. The remote alarm bit (bit 11), and the national bit (bit 12) in the frame format are monitored for status. A threshold detector is provided for a bit error rate (BER) measurement. The E3 signal is demultiplexed into four E2 signals, which pass through 32-bit FIFOs at the output.

When the device is configured as an E13 multiplexer/demultiplexer, the four E2 signals are connected internally to the four E12 demultiplexers. However, the four E23RGCm Clock outputs must be physically connected to E23RCKm clock inputs for proper operation in E13 mode. The E2 signals are available for monitoring using the data lead E23RDm and gapped clock lead.

Each of the four E2 signals is monitored for frame alignment and AIS, which are provided with status bits and maskable interrupt control bits. The states of the remote alarm bit (bit 11) and national bit (bit 12) in each of the four E2 frames are provided as status bits with associated maskable interrupts. A threshold detector is provided for a bit error rate (BER) measurement. Each of the E12s demultiplexes the E2 frame into four E1 signals. The data is written into 32-bit FIFOs using the internal gapped clock. Each E1 channel has an internal digital phase-locked loop circuit (DPLL). The receive gapped clock is connected to the digital phase-locked loop circuit as the reference frequency, along with the 34368 kHz external system clock (XCLK). The output of the DPLL is used to clock the data from the E1 receive FIFO, and is also provided as an output (E1RCKn). The E1 DPLLs require approximately 1 second of settling time after they are enabled to ensure proper operation of E1 FIFOs. Under microprocessor control, either clock edge may be used to clock out the data (E1RDPn/ E1RNRZn and E1RDNn).

The E123MUX can also be configured into hybrid configurations. That is, the device can be configured to provide four E12 multiplexers and demultiplexers (16 E1 channels to/from four E2 channels), and one E23 multiplexer and demultiplexer (four E2 channels to/from one E3 channel). In this configuration, the format of the data from the four multiplexers and demultiplexers at the E2 level is NRZ only. In the multiplex direction, the data (E12TDm) from the four sections is clocked out by the E2 clocks (E12TCKOm). The NRZ data input (E23TDn) to the E23 multiplexer is clocked in by the E2 clocks (E23TCKm). The clock edges used for clocking in and out data from the E23 section are programmable.

In the demultiplex direction, four E23 gapped output clocks are provided on leads E23RGCm. E2 data (E23RDm) is clocked out of the internal FIFO by the receive input clock (E23RCKm). It is assumed that external DPLLs will be used in this configuration to provide a symmetrical clock, and that the outputs of the DPLLs are connected to the E23RCKm leads for E2 operation. The receive data input to the four E12 demultiplexers consists of data (E12RDm) and clock (E12RCKm).

If an E23 demultiplexer is connected to the E12 demultiplexer to provide E3 to E1 demultiplexing, the E23 receive gapped clock lead (E23RGCm) is connected to the E23 receive input clock (E23RCKm) and the E12 receive input clock (E12RCKm). The E23 data leads (E23RDm) are connected to the E12 receive data leads (E12RDm). The clock edges used for clocking data into and out of the E12 sections are programmable.

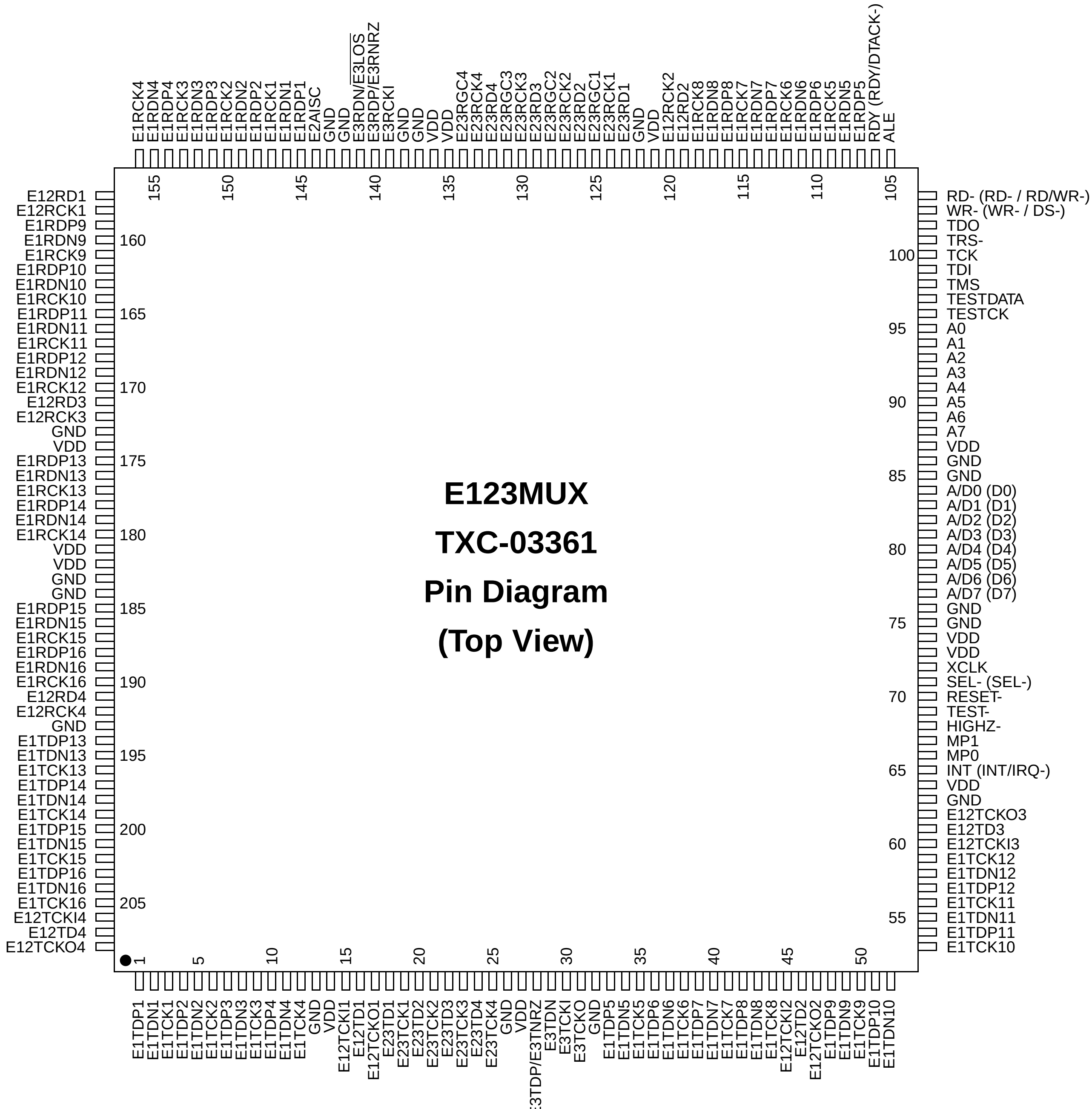
The E123MUX provides a number of testing features, including an E1 PRBS generator and analyzer. The PRBS sequence is a 2^{15}-1 polynomial, and the sequence corresponds to the sequence specified in the ITU-T O-151 recommendation. The E1 transmit channel to be used for inserting the PRBS pattern is programmable. The E1 receive channel to be analyzed is also programmable, and is independent of the channel selected in the transmit direction. Only one channel at a time is programmable for PRBS testing in each direction.

The E123MUX also supports individual E1 remote loopbacks, E2 local and remote loopbacks, and E3 local and remote loopbacks. Remote loopback enables the receive clock and data leads to be looped back as transmit clock and data in the upstream direction.

For device testing, both boundary scan and an option to force all bidirectional outputs to a high impedance state for board testing are provided.

The microprocessor interface supports a multiplexed 8-bit address/data bus, an Intel-compatible split bus or a Motorola-compatible split bus. The split bus has 8 address bits and 8 data bits. Interrupt capability is also provided, with the ability to mask an active alarm status from causing an interrupt.

PIN DIAGRAM



Notes:

1. An X(Y/Z) format is used for symbol names of microprocessor interface signal pins to identify pin functions in the Multiplexed Address/Data [X] and (Intel [Y] / Motorola [Z]) modes of operation, where these functions are different.
2. Active low (inverted) signals are indicated by '-' at end of symbol (e.g., RESET- is equivalent to $\overline{\text{RESET}}$).
3. Some pin symbols have been abbreviated due to space limitations (see Pin Descriptions section for complete symbols).

Figure 2. E123MUX TXC-03361 Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY AND GROUND

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	14, 27, 64, 73, 74, 87, 121, 135, 136, 174, 181, 182	P		**V_{DD}:** +5 volt supply voltage, ± 5%.
GND	13, 26, 32, 63, 75, 76, 85, 86, 122, 137, 138, 142, 143, 173, 183, 184, 193	P		**Ground:** 0 volts reference

*Note: I = Input; O = Output; P = Power; T = Tri-state; D = Open Drain Tri-state

E1 RECEIVE AND TRANSMIT INTERFACES

Symbol	Pin No.	I/O/P	Type *	Name/Function
E1RDPn/ E1RNRZn (n = 1 - 16) n=4 --> n=8 --> n=12 --> n=16 -->	145 148 151 154 107 110 113 116 159 162 165 168 175 178 185 188	O	CMOS 2 mA	**Receive Positive Rail/NRZ Output, E1 Channels 1 - 16:** These pins are used for output of the receive positive rail HDB3 signal, or the receive NRZ signal, for E1 channels 1 through 16. Dual rail unipolar or NRZ mode may be selected for each channel independently, by setting 16 control bits. Pin 145 represents the output signal for E1 channel 1, while pin 188 represents channel 16. The positive rail or NRZ signals for all 16 ports are clocked out of the E123MUX on rising edges of the receive clocks E1RCKn when control bit RE1CS is a 1, and on falling edges of the clocks when the control bit is set to 0.
E1RDNn (n = 1 - 16) n=4 --> n=8 --> n=12 --> n=16 -->	146 149 152 155 108 111 114 117 160 163 166 169 176 179 186 189	O	CMOS 2 mA	**Receive Negative Rail Output, E1 Channels 1 - 16:** These pins are used for the receive negative rail HDB3 signal outputs for E1 channels 1 through 16. Pin 146 represents the negative rail signal for E1 channel 1, while pin 189 represents channel 16. The negative rail signals for all 16 ports are clocked out of the E123MUX on rising edges of the receive clocks E1RCKn when control bit RE1CS is a 1, and on falling edges of the clocks when this control bit is set to 0. This pin is disabled when the NRZ mode is selected for a channel.

*See Input, Output and I/O Parameters section below for Type definitions.

Symbol	Pin No.	I/O/P	Type	Name/Function
E1RCKn (n = 1 - 16) n=4 --> n=8 --> n=12 --> n=16 -->	147 150 153 156 109 112 115 118 161 164 167 170 177 180 187 190	O	CMOS 2 mA	**Receive Output Clock, E1 Channels 1 - 16:** These pins provide receive output clocks for E1 channels 1 through 16. These clocks are derived from internal DPLLs using the system clock (XCLK) and the internal E1 receive gapped clock. When control bit BPPLLm is a 1 (m = 1 to 4, for n = 1-4, 5-8, 9-12 and 13-16), the DPLL is bypassed and the output is the receive gapped clock. Pin 147 represents channel 1, while pin 190 represents channel 16.
E1TDPn/ E1TNRZn (n = 1 - 16) n=4 --> n=8 --> n=12 --> n=16 -->	1 4 7 10 33 36 39 42 48 51 54 57 194 197 200 203	I	TTL	**Transmit Positive Rail/NRZ Input, E1 Channels 1 - 16:** These pins are used for the transmit positive rail HDB3 signal inputs, or the transmit NRZ signal inputs, for E1 channels 1 through 16. Dual rail unipolar or NRZ mode may be selected for each channel independently by setting 16 control bits. Pin 1 represents the input signal for E1 channel 1, while pin 203 represents channel 16. The positive rail or NRZ signal input for channel n is clocked into the E123MUX on rising edges of the transmit clock E1TCKn when control bit TE1CS is a 0, and on falling edges of this clock when this control bit is set to 1.
E1TDNn/ $\overline{\text{E1LOSn}}$ (n = 1 - 16) n=4 --> n=8 --> n=12 --> n=16 -->	2 5 8 11 34 37 40 43 49 52 55 58 195 198 201 204	I	TTL	**Transmit Negative Rail Input or Loss of Signal Input, E1 Channels 1 - 16:** In the dual rail unipolar operating mode, these pins are used for the transmit negative rail HDB3 signal inputs for E1 channels 1 through 16. Pin 2 represents the input negative rail signal for E1 channel 1, while pin 204 represents channel 16. The negative rail signal for channel n is clocked into the E123MUX on rising edges of the transmit clock E1TCKn when control bit TE1CS is a 0, and on falling edges of this clock when this control bit is set to 1. When the NRZ operating mode is selected for a channel, this pin may be used as the input for an external E1 loss of signal (LOS) indication from an external line interface unit. $\overline{\text{E1LOSn}}$ is active low. Any of these pins that are not used for LOS inputs must be held high.

Symbol	Pin No.	I/O/P	Type	Name/Function
E1TCKn (n = 1 - 16) n=4 --> n=8 --> n=12 --> n=16 -->	3 6 9 12 35 38 41 44 50 53 56 59 196 199 202 205	I	CMOS	**Transmit Input Clock, E1 Channels 1 - 16:** These pins provide the transmit input clocks for E1 channels 1 through 16. Pin 3 represents channel 1, while pin 205 represents channel 16. The clock frequency must be 2048 kHz ± 50 ppm and the duty cycle must be (50 ± 10) %.

E2 RECEIVE AND TRANSMIT INTERFACES (E12 MULTIPLEXERS/DEMULTIPLEXERS 1-4)

Symbol	Pin No.	I/O/P	Type	Name/Function
E12RDm (m = 1 - 4)	157 119 171 191	I	TTL	**Receive E12 Data:** These four pins are used for the receive E2 NRZ data input signals when the E123MUX is configured as a separate E12 multiplexer/demultiplexer. Pin 157 corresponds to the E12 multiplexer/demultiplexer number 1, which is associated with E1 channels 1 - 4. In the E13 mode of operation these pins are connected internally to the corresponding E23RDm output pins.
E12RCKm (m = 1 - 4)	158 120 172 192	I	CMOS	**Receive E12 Clock:** These four pins are used to clock in the receive E2 NRZ data signals. Pin 158 corresponds to the E12 multiplexer/demultiplexer number 1. Receive data is clocked into the E123MUX on rising edges of this clock. In the E13 mode of operation these pins are connected internally to the corresponding E23RGCm output pins.
E12TDm (m = 1 - 4)	16 46 61 207	O	CMOS 2 mA	**Transmit E12 Data:** These four pins are used to output the transmit E2 NRZ data signal when the E123MUX is configured as a separate E12 multiplexer/demultiplexer. Pin 16 corresponds to the E12 multiplexer number 1, which is associated with E1 channels 1 - 4. In the E13 mode of operation these pins are connected internally to the corresponding E23TDm pins.
E12TCKIm (m = 1 - 4)	15 45 60 206	I	CMOS	**Transmit E12 Clock Input:** These four pins are used to provide input clocks for clocking out the transmit E2 NRZ data output signals E12TDm and clock signal E12TCKOm. Pin 15 corresponds to the E12 multiplexer/demultiplexer number 1. Please note that an 8448 kHz clock with a ± 30 ppm tolerance and a duty cycle of (50 ± 10) % must be connected to these pins for proper E12 to E23 operation.

Symbol	Pin No.	I/O/P	Type	Name/Function
E12TCKOm (m = 1 - 4)	17 47 62 208	O	CMOS 2 mA	**Transmit E12 Clock Output:** These four pins are used to provide output clocks for clocking out the transmit E2 NRZ data output signals (E12TDm). Pin 17 corresponds to the E12 multiplexer/demultiplexer number 1. Transmit data is clocked out of the E12 on rising edges of this clock in E13 mode. In E12 skip mux mode this is programmable by control bit T12CSm. In the E13 mode of operation the E12TCKOm signals are connected internally to the corresponding E23TCKm signals.

E2 RECEIVE AND TRANSMIT INTERFACES (E23 MULTIPLEXER/DEMULTIPLEXER)

Symbol	Pin No.	I/O/P	Type	Name/Function
E23RDm (m = 1 - 4)	123 126 129 132	O	CMOS 2 mA	**Receive E23 Data:** These four pins are used to output the receive E2 NRZ data signals when the E123MUX is configured as a separate E23 multiplexer/demultiplexer. Pin 123 corresponds to the E23 demultiplexer E2 output channel number 1.
E23RGCm (m = 1 - 4)	125 128 131 134	O	CMOS 2 mA	**Receive Gapped E23 Clock:** These four pins provide the receive gapped clock outputs for the E23 demultiplexer when the E123MUX is configured for E23 operation. These clocks are the write clocks of an internal FIFO. These clocks may be connected to an external digital PLL if the E123MUX is used in hybrid configurations (E12 and E23 sections). The dejittered clock from the digital PLL is connected to the E23RCKm input clocks. This clock is derived from the received E3 34368 kHz clock. Pin 125 represents the output gapped clock for E2 channel 1. Please note that, for E13 operation, the E23RGCm output receive gapped clock leads must be connected to the corresponding E23RCKm input clock leads.
E23RCKm (m = 1 - 4)	124 127 130 133	I	CMOS	**Receive Input Clock:** These four pins provide the input clocks for clocking out the receive data from the E23 demultiplexer when the E123MUX is configured for E23 operation. The receive data is clocked out of an internal FIFO. For hybrid configurations these clocks may be connected to digital PLLs. The NRZ signal for channel m is clocked out of the E23 on rising edges of the E23RCKm clocks when control bit R23CSm is a 1, and on falling edges of this clock when the control bit is set to 0. Pin 124 represents the input clock for E2 channel 1. Please note that, for E13 operation, the E23RCKm input clock leads must be connected to the corresponding E23RGCm output receive gapped clock leads.

Symbol	Pin No.	I/O/P	Type	Name/Function
E23TDm (m = 1 - 4)	18 20 22 24	I	TTL	**Transmit E2 Data:** These four pins are used for the transmit E2 NRZ data input signals when the E123MUX is configured as an E23 multiplexer/demultiplexer. Pin 18 corresponds to the E23 multiplexer/demultiplexer E2 input channel number 1. When in E13 skip mux mode these input pins are ignored by the internal logic. For E13 operation these unused pins should be attached to a common pull-up resistor.
E23TCKm (m = 1 - 4)	19 21 23 25	I	CMOS	**Transmit E2 Clock:** These four pins are used to provide input clocks for clocking in the transmit E2 NRZ data input signals when the E123MUX is configured for E23 operation. Pin 19 represents the input clock for E23 multiplexer/ demultiplexer E2 input channel number 1. Transmit data is clocked into the E123MUX on rising edges of this clock when control bit T23CSm is a 0, and on falling edges of this clock when the control bit is set to 1 for each E23 multiplexer. When in E13 Mode, these input pins are ignored and the clocking is done by internal logic. For E13 Mode, these pins should be attached to a common pull-up resistor. When in E23 Mode, the input clock frequency must be 8448 kHz with ± 30 ppm accuracy and a duty cycle of (50 ± 10) %.

E3 RECEIVE AND TRANSMIT INTERFACES

Symbol	Pin No.	I/O/P	Type	Name/Function
E3RDP/ E3RNRZ	140	I	TTL	**Receive E3 Positive Rail/NRZ Input:** This pin is used for the receive E3 positive rail HDB3 signal input, or the receive E3 NRZ signal input.
E3RDN/ $\overline{\text{E3LOS}}$	141	I	TTL	**Receive E3 Negative Rail Input/E3 LOS Input:** In dual rail unipolar mode, this pin is used for the receive E3 negative rail HDB3 signal input. When the NRZ operating mode is selected, this pin may be used as the input for an active low external E3 loss of signal (LOS) indication from an external line interface unit. If this pin is not used for LOS it must be tied high.
E3RCKI	139	I	CMOS	**Receive E3 Clock In:** The E3 positive and negative rail signals or the E3 NRZ signal are clocked into the E123MUX on rising edges of this clock input signal when control bit RE3CS is a 0, and on falling edges when this control bit is a 1.
E3TDP/ E3TNRZ	28	O	CMOS 2 mA	**Transmit E3 Positive Rail/NRZ Output:** This pin is used for the transmit E3 positive rail HDB3 signal output, or the transmit NRZ signal output.
E3TDN	29	O	CMOS 2 mA	**Transmit E3 Negative Rail Output:** This pin is used for the transmit E3 negative rail HDB3 signal output. This lead is disabled when the NRZ mode is selected.

Symbol	Pin No.	I/O/P	Type	Name/Function
E3TCKO	31	O	CMOS 2 mA	**Transmit E3 Clock Output:** The E3 positive and negative rail signals or the E3 NRZ signal are clocked out of the E123MUX on rising edges of this clock when control bit TE3CS is a 1, and on falling edges when this control bit is a 0. E3TCKO is derived from E3TCKI.
E3TCKI	30	I	CMOS	**Transmit E3 Clock Input:** This input clock frequency must be 34368 kHz ± 20 ppm and the duty cycle must be (50 ± 5) %.

EXTERNAL CLOCK INPUTS

Symbol	Pin No.	I/O/P	Type	Name/Function
XCLK	72	I	CMOS	**External Clock:** A 34368 kHz clock with ± 20 ppm accuracy and a duty cycle of (50 ± 5) % must be connected to this pin. It is used by the E123MUX as a reference for the internal E1 digital PLLs.
E2AISC	144	I	CMOS	**E2 AIS External Clock:** An 8448 kHz clock with ± 30 ppm accuracy and a duty cycle of (50 ± 10) % must be connected to this pin. It is used by the E123MUX for E2 AIS generation during fault conditions. This clock may also be connected to the Transmit E12 Clock Input pins (E12TCKIm). Note: This clock is required for the proper operation of the microprocessor interface.

CONTROL LEADS

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{HIGHZ}}$	68	I	TTL	**High Impedance Enable:** A low forces all E123MUX output and bidirectional leads (except TDO) to a high impedance state for board level testing. For normal operation this pin must be held high.
$\overline{\text{TEST}}$	69	I	TTL	**TranSwitch Test Mode:** For normal operation this pin must be held high.
$\overline{\text{RESET}}$	70	I	TTL	**Reset:** An active low on this lead resets the internal state machines, counters and control registers to their default states. The reset signal should be held low for a minimum of 150 nanoseconds. It should be applied after power becomes stable.

TEST ACCESS PORT FOR BOUNDARY SCAN

Symbol	Pin No.	I/O/P	Type	Name/Function
TCK	100	I	TTL	**Test Clock:** This is the input clock for boundary scan testing. The TDI and TMS states are clocked into the E123MUX on rising edges of this clock.
TDI	99	I	TTLp	**Test Data Input:** Serial data input for boundary scan test messages. This lead has an internal pull-up resistor.
TDO	102	O(T)	CMOS 4 mA	**Test Boundary Data Output:** Serial data output whose information is clocked out on falling edges of TCK.
TMS	98	I	TTLp	**Test Boundary Mode Select:** This input signal is used to control test operations. This lead has an internal pull-up resistor.
$\overline{\text{TRS}}$	101	I	TTLp	**Test Boundary Scan Reset:** This pin must be either held low or asserted low, then high (pulsed low) for a minimum of 500 ns to asynchronously reset the Test Access Port (TAP) controller. Failure to perform this reset may cause the TAP controller to take over control of the output pins. See Test Access Port Section for details. This lead has an internal pull-up resistor.

TEST PINS

Symbol	Pin No.	I/O/P	Type	Name/Function
TESTCK	96	O	CMOS 2 mA	**Test Scan Clock:** Provided for TranSwitch testing purposes only.
TESTDATA	97	O	CMOS 2 mA	**Test Scan Data:** Provided for TranSwitch testing purposes only.

MICROPROCESSOR SELECTION

Symbol	Pin No.	I/O/P	Type	Name/Function
MP0 MP1	66 67	I	TTL	**Microprocessor Selection Control Bits:** The type of microprocessor interface bus is selected according to the states given in the table below: MP0 / MP1 / Selection Low / Low / Motorola-compatible bus I/O Low / High / Reserved. Do not use. High / Low / Intel-compatible bus I/O High / High / Multiplexed bus I/O

MICROPROCESSOR INTERFACE - MULTIPLEXED BUS

Symbol	Pin No.	I/O/P	Type	Name/Function
A/D(7-0)	77 - 84	I/O	TTL 4 mA	**Address/Data Bus:** Address input leads and bidirectional data leads used for selecting the address and transferring data between the E123MUX and the microprocessor. High is logic one. A/D0 (pin 84) is the least significant bit.
ALE	105	I	TTL	**Address Latch Enable:** An active high signal generated by the microprocessor. It is used for holding an address stable during a read/write cycle when in multiplexed microprocessor mode. This pin should be held high in Motorola/ Intel modes.
$\overline{\text{SEL}}$	71	I	TTL	**Select:** A low enables data transfers between the microprocessor and the E123MUX during a read/write cycle.
$\overline{\text{RD}}$	104	I	TTL	**Read:** An active low signal generated by the microprocessor for reading the E123MUX memory map locations.
$\overline{\text{WR}}$	103	I	TTL	**Write:** An active low signal generated by the microprocessor for writing to the E123MUX memory map locations.
RDY	106	O(T)	CMOS 4 mA	**Ready**: A high is an acknowledgment from the addressed memory location that the transfer can be completed. A low indicates that the transfer cannot be completed and that microprocessor wait states must be generated. This lead is tri-stated when not driven high or low.
INT	65	O(D)	CMOS 2 mA	**Interrupt:** A high on this output pin signals an interrupt request to the microprocessor when an alarm occurs while the interrupt mask bit for that alarm is disabled (set to 0). This pin is open drain and requires a 4.7 kilohm pull-up resistor for proper operation.

MICROPROCESSOR INTERFACE - SPLIT BUS

Symbol	Pin No.	I/O/P	Type	Name/Function
A(7-0)	88 - 95	I	TTL	**Address Bus (Intel/Motorola Interfaces):** These are address line inputs that are used for accessing a memory location for a read/write cycle. High is logic one. A0 (pin 95) is the least significant bit.
D(7-0)	77 - 84	I/O	TTL 4 mA	**Data Bus (Intel/Motorola Interfaces):** These are bidirectional data lines used for transferring data between the memory and the microprocessor. High is logic one. D0 (pin 84) is the least significant bit.
$\overline{\text{SEL}}$	71	I	TTL	**Select (Intel/Motorola Interfaces):** A low enables data transfers between the microprocessor and the E123MUX during a read/write cycle.
$\overline{\text{RD}}$ / RD/$\overline{\text{WR}}$	104	I	TTL	**Read (Intel Interface) or Read/Write (Motorola):** Intel Interface - An active low signal generated by the microprocessor for reading the E123MUX memory map locations. Motorola Interface - An active high signal is generated by the microprocessor for reading the E123MUX memory map locations. An active low signal is used to write to E123MUX memory map locations.
$\overline{\text{WR}}$/$\overline{\text{DS}}$	103	I	TTL	**Write (Intel Interface) or Data Select (Motorola):** Intel Interface - An active low signal generated by the microprocessor for writing to the E123MUX memory map locations. Motorola Interface - An active low signal generated by the microprocessor to select the data to be read or written. Connect to the $\overline{\text{DS}}$ signal at the microprocessor.
RDY/ $\overline{\text{DTACK}}$	106	O(T)	CMOS 4 mA	**Ready (Intel Interface) or Data Transfer Acknowledge (Motorola Interface):** Intel Interface - A high is an acknowledgment from the addressed memory map location that the transfer can be completed. A low indicates that the E123MUX cannot complete the transfer cycle and that microprocessor wait states must be generated. Motorola Interface - During a read bus cycle, a low signal indicates that the information on the data bus is valid. During a write bus cycle, a low signal acknowledges the acceptance of data. This lead is tri-stated when it is not driven high or low.
INT/$\overline{\text{IRQ}}$	65	O(D)	CMOS 2 mA	**Interrupt (Intel Interface) or Interrupt Request (Motorola Interface):** Intel Interface - A high on this output pin signals an interrupt to the microprocessor when an alarm occurs while the interrupt mask bit for that alarm is disabled (set to 0). Motorola Interface - A low on this output pin signals an interrupt request to the microprocessor when an alarm occurs while the interrupt mask bit for that alarm is disabled (set to 0). This pin is open drain tri-state and requires a 4.7 kilohm pull-up resistor for proper operation in both Intel and Motorola Modes.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+7.0	V	Note 1
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	Note 1
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient operating temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Component Temperature x Time	TI		270 x 5	^oC x s	Note 1
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD		±2000	V	per MIL-STD-833D Method 3015.7

Notes:
1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		26.0		$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}			285	mA	
P_{DD}			1500	mW	Inputs switching

INPUT, OUTPUT AND I/O PARAMETERS

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			0.8	V	$4.75 \le V_{DD} \le 5.25$
Input leakage current			10	µA	V_{DD} =5.25
Input capacitance		5.0		pF	

Input Parameters For TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			0.8	V	$4.75 \le V_{DD} \le 5.25$
Input leakage current		0.10	0.24	mA	V_{DD} =5.25; Input = 0 volts
Input capacitance		5.5		pF	

Note: Input has a 47 kilohm (nominal) internal pull-up resistor.

Input Parameters For CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			1.65	V	$4.75 \le V_{DD} \le 5.25$
Input leakage current			10	µA	V_{DD} =5.25
Input capacitance		5.0		pF	

Output Parameters For CMOS 2 mA (Open Drain)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 2.0
I_{OL}			2.0	mA	

Note: Open Drain requires use of an external 4.7 kilohm pull-up resistor for proper operation.

Output Parameters For CMOS 2 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 2.0
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF
Leakage Tri-state			+/-10	µA	0 to 5.25 V input

Output Parameters For CMOS 4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.8			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.5	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
I_{OZ} (HIGHZ output current)			±10.0	µA	

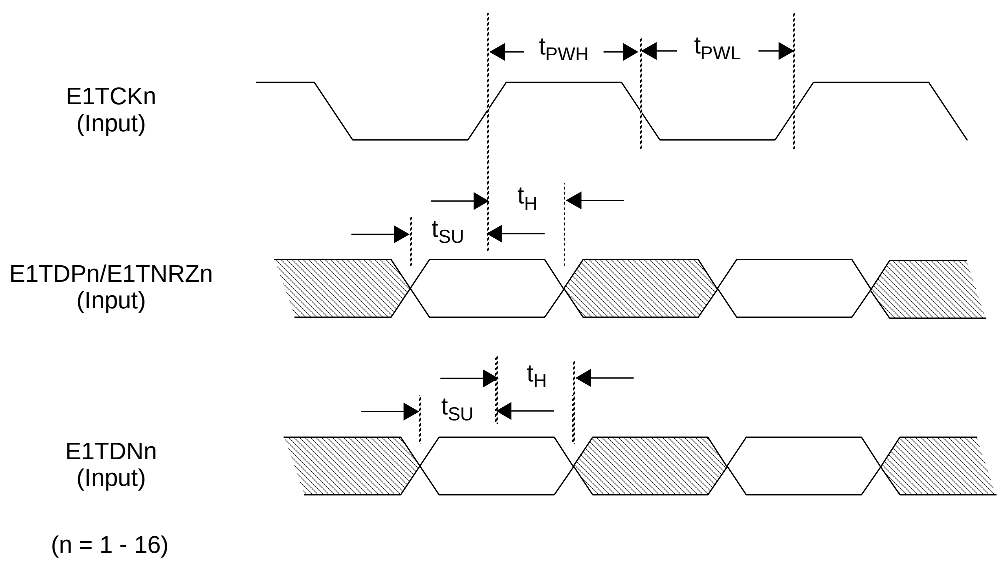
Input/Output Parameters For TTL 4 mA (slew rate controlled)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			0.8	V	$4.75 \le V_{DD} \le 5.25$
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		7.0		pF	
V_{OH}	2.4			V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 25 pF
t_{FALL}			5	ns	C_{LOAD} = 25 pF

TIMING CHARACTERISTICS

Detailed timing diagrams for the E123MUX are illustrated in Figures 3 through 19, with values of the timing intervals tabulated below each diagram. All output times are measured with a maximum 25 pF load capacitance. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals.

Figure 3. E1 Transmit Input Interface Timing

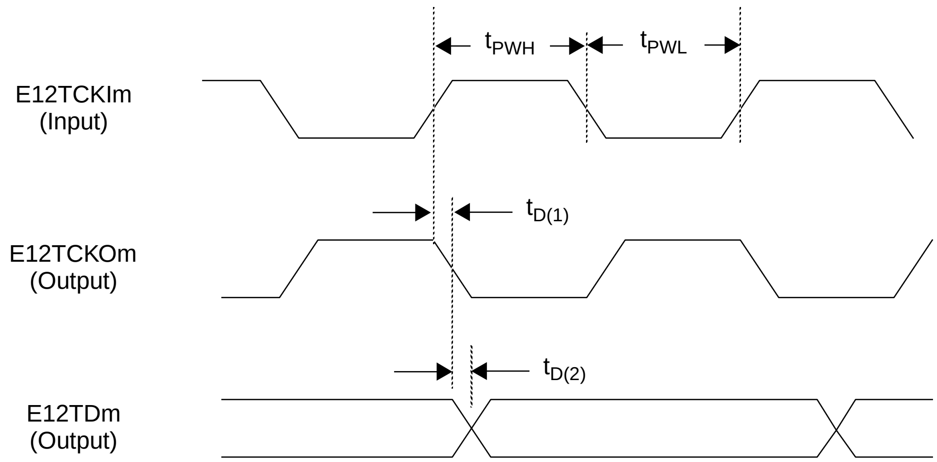


Note: Shown for control bit TE1CS equal to 0 (Bit 6 in address 04H)

Parameter	Symbol	Min	Typ	Max	Unit
E1TCKn clock frequency		2048 ± 50 ppm (Note 1)			kHz
E1TCKn high time	t_{PWH}	40	50	60	%
E1TCKn low time	t_{PWL}	40	50	60	%
E1TDPn/E1TNRZn and E1TDNn set-up time before E1TCKn↑	t_{SU}	10			ns
E1TDPn/E1TNRZn and E1TDNn hold time after E1TCKn↑	t_H	10			ns

Note 1: Meets the G.823 E1 jitter tolerance curve.

Figure 4. E12 Transmit Output Interface Timing

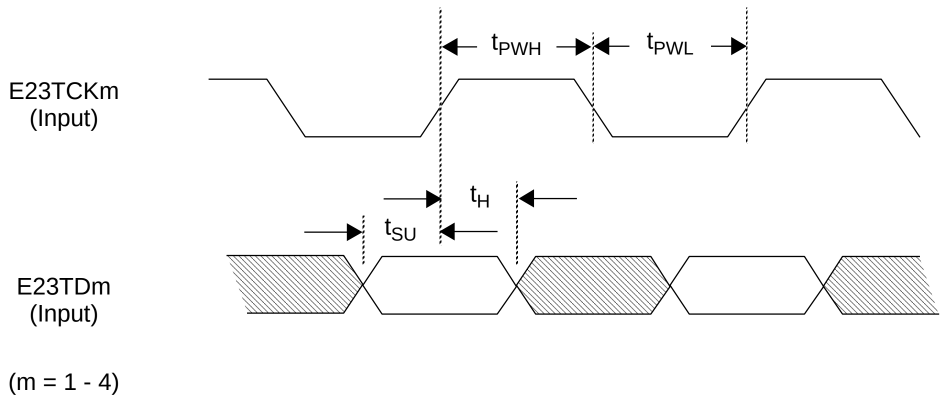


(m = 1 - 4)

Note: Shown for control bit T12CSm Parameter equal to 0 (bit 5 in addresses 2AH, 3AH, 4AH, and 5AH, for m = 1-4) and configuration bit E13M equal to 0 (bit 7 address B9H).

Parameter	Symbol	Min	Typ	Max	Unit
E12TCKIm clock frequency			8448 ± 30 ppm		kHz
E12TCKIm high time	t_{PWH}	40	50	60	%
E12TCKIm low time	t_{PWL}	40	50	60	%
E12TCKOm↓ output delay after E12TCKIm↑	$t_{D(1)}$	5.0		93	ns
E12TDm (NRZ Data) output delay after E12TCKOm↓	$t_{D(2)}$	5.0		10	ns

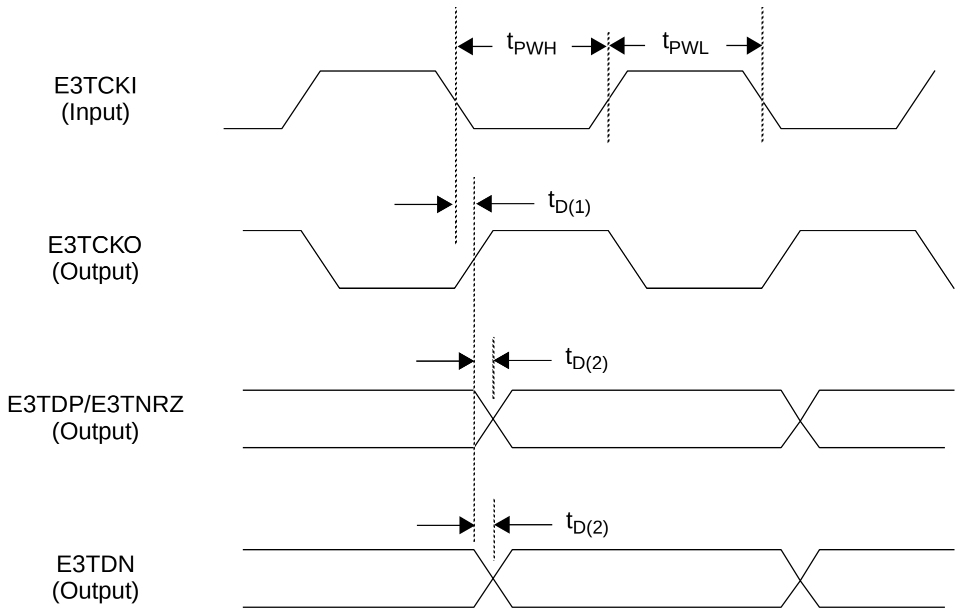
Figure 5. E23 Transmit Input Interface Timing



Note: Shown for control bit T23CSm equal to 0 (bits 7, 5, 3, 1 in address B7H, for m = 4-1)

Parameter	Symbol	Min	Typ	Max	Unit
E23TCKm clock frequency		8448 ± 30 ppm			kHz
E23TCKm high time	t_{PWH}	40	50	60	%
E23TCKm low time	t_{PWL}	40	50	60	%
E23TDm set-up time before E23TCKm↑	t_{SU}	10			ns
E23TDm hold time after E23TCKm↑	t_H	10			ns

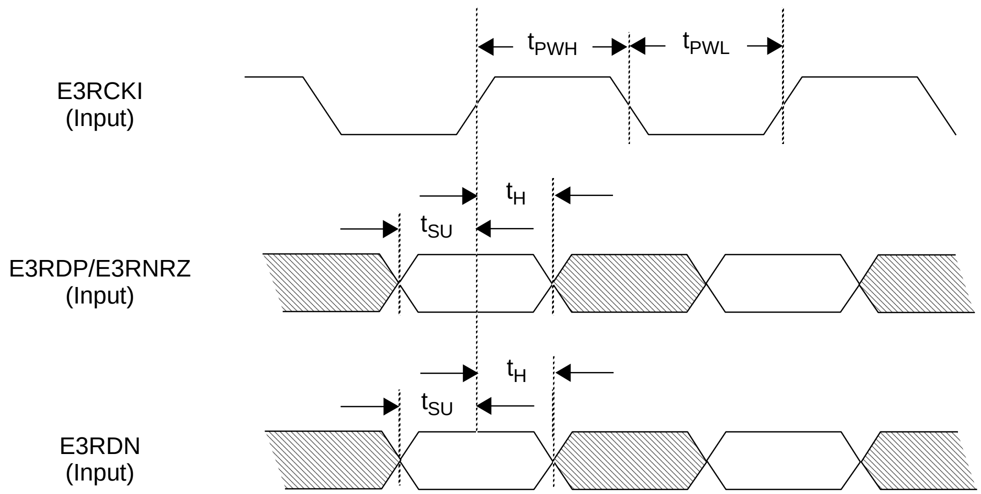
Figure 6. E3 Transmit Output Interface Timing



Note: Shown for control bit TE3CS equal to 1 (Bit 0 in address B0H)

Parameter	Symbol	Min	Typ	Max	Unit
E3TCKI clock frequency		34368 ± 20 ppm			kHz
E3TCKI high time	t_{PWH}	45	50	55	%
E3TCKI low time	t_{PWL}	45	50	55	%
E3TCKO↑ output delay after E3TCKI↓	$t_{D(1)}$	3.0		14	ns
E3TDP/E3TNRZ and E3TDN output delay after E3TCKO↑	$t_{D(2)}$	3.0		8.0	ns

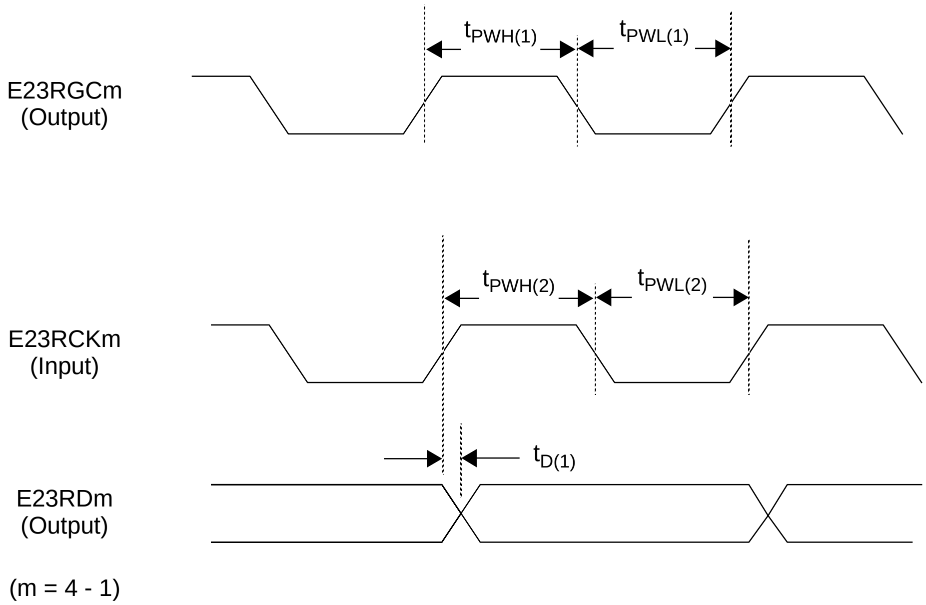
Figure 7. E3 Receive Input Interface Timing



Note: Shown for control bit RE3CS equal to 0 (Bit 1 in address B0H)

Parameter	Symbol	Min	Typ	Max	Unit
E3RCKI clock frequency		34368 ± 20 ppm			kHz
E3RCKI high time	t_{PWH}	45	50	55	%
E3RCKI low time	t_{PWL}	45	50	55	%
E3RDP/E3RNRZ and E3RDN set-up time before E3RCKI↑	t_{SU}	7.0			ns
E3RDP/E3RNRZ and E3RDN hold time after E3RCKI↑	t_H	5.0			ns

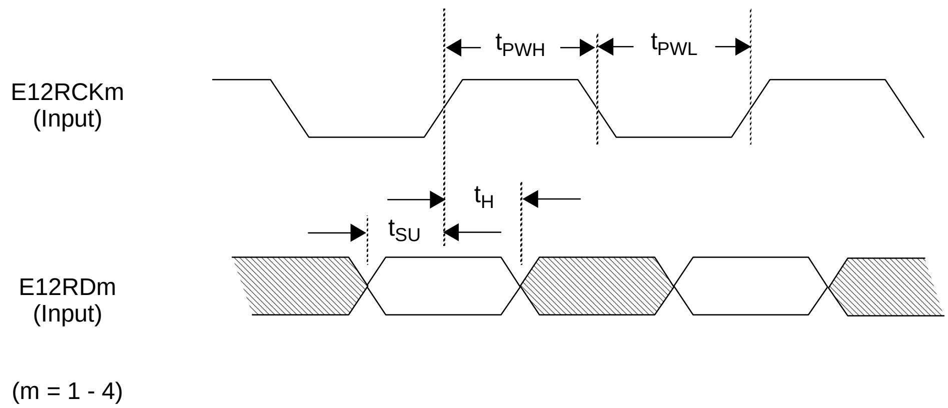
Figure 8. E23 Receive Output Interface Timing



Note: Shown for control bit R23CSm equal to 1 (bits 6, 4, 2, 0 in address B7H, for m = 4 - 1)

Parameter	Symbol	Min	Typ	Max	Unit
E23RGCm receive gapped clock frequency			8448 ± 30 ppm		kHz
E23RGCm receive gapped clock high time	$t_{PWH(1)}$	40	50	60	%
E23RGCm receive gapped clock low time	$t_{PWL(1)}$	40	50	60	%
E23RCKm clock frequency			8448 ± 30 ppm		kHz
E23RCKm high time	$t_{PWH(2)}$	40	50	60	%
E23RCKm low time	$t_{PWL(2)}$	40	50	60	%
E23RDm output delay after E23RCKm ↑	$t_{D(1)}$	10			ns

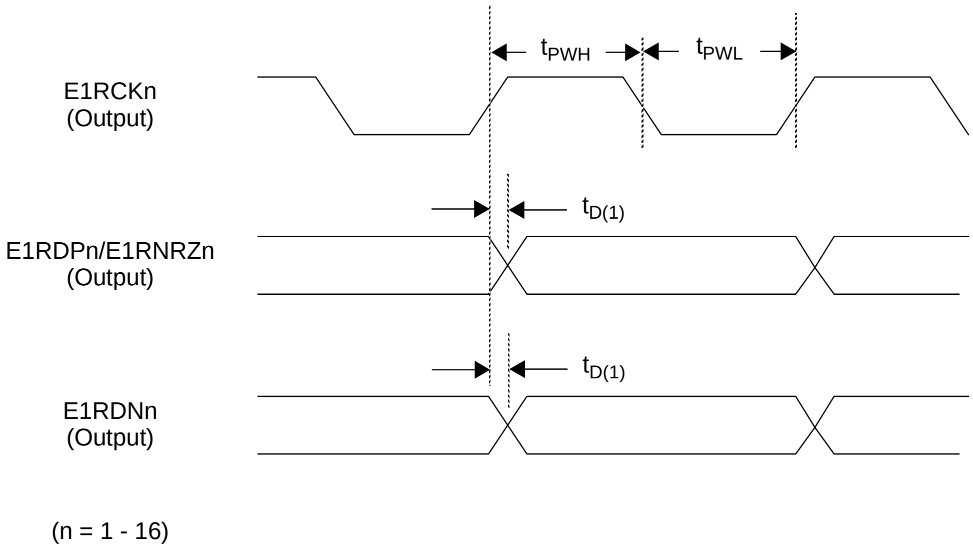
Figure 9. E12 Receive Input Interface Timing



Note: Shown for control bit R12CSm equal to 0 (bit 6 in addresses 2AH, 3AH, 4AH, and 5AH, for m = 1-4)

Parameter	Symbol	Min	Typ	Max	Unit
E12RCKm clock frequency			8448 ± 30 ppm		kHz
E12RCKm high time	t_{PWH}	40	50	60	%
E12RCKm low time	t_{PWL}	40	50	60	%
E12RDm (NRZ) set-up time before E12RCKm ↑	t_{SU}	10			ns
E12RDm hold time after E12RCKm ↑	t_H	10			ns

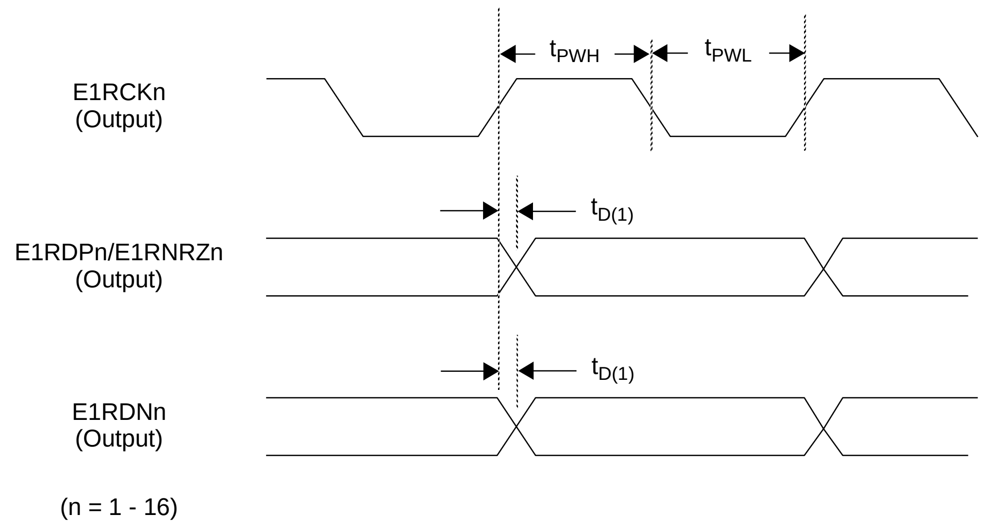
Figure 10. E1 Receive Output Interface Timing - PLL Enabled



Note: Shown for control bit BPPLLm equal to 0 (bit 7 in addresses 61H, 71H, 81H, and 91H, for m = 1-4) and control bit RE1CS equal to 1 (Bit 5 in address 04H). For m = 1, 2, 3, 4 the values of n are 4-1, 8-5, 12-9, 16-13.

Parameter	Symbol	Min	Typ	Max	Unit
E1RCKn clock frequency		2048 ± 50 ppm			kHz
E1RCKn high time	t_{PWH}	40	50	60	%
E1RCKn low time	t_{PWL}	40	50	60	%
E1RDPn/E1RNRZn and E1RDNn output delay after E1RCKn↑	$t_{D(1)}$			10	ns

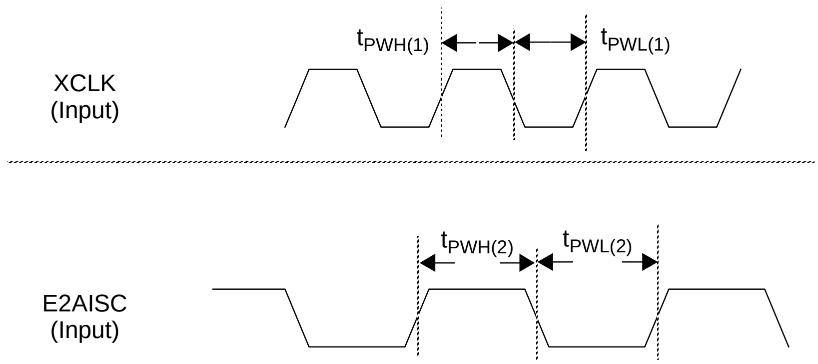
Figure 11. E1 Receive Output Interface Timing - PLL Bypassed



Note: Shown for control bit BPPLLm equal to 1 (bit 7 in addresses 61H, 71H, 81H, and 91H, for m = 1-4) and control bit RE1CS equal to 1 (Bit 5 in address 04H). For m = 1, 2, 3, 4 the values of n are 4-1, 8-5, 12-9, 16-13.

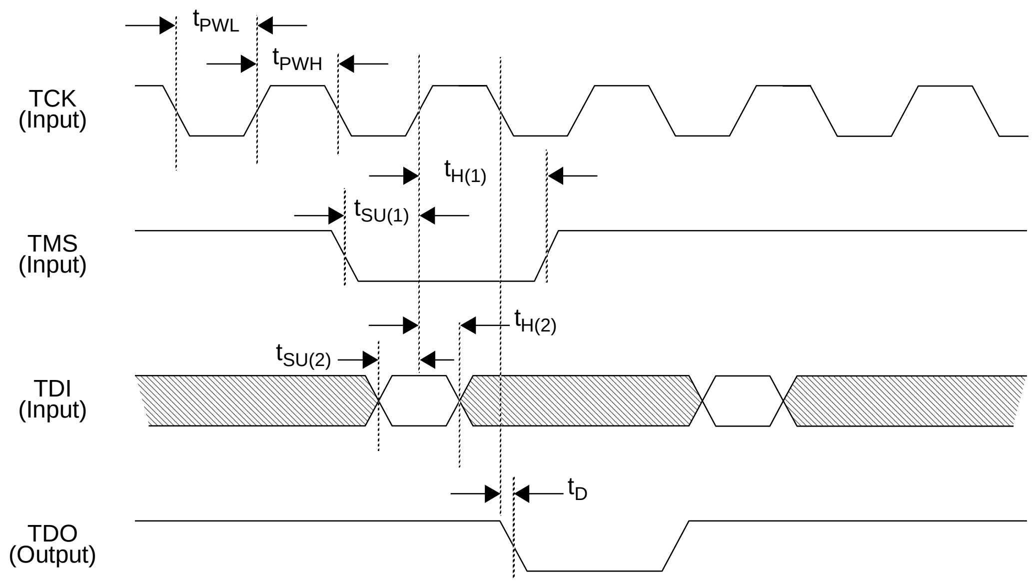
Parameter	Symbol	Min	Typ	Max	Unit
E1RCKn clock frequency			2048 ± 50 ppm		kHz
E1RCKn high time	t_{PWH}	40	50	60	%
E1RCKn low time	t_{PWL}	40	50	60	%
E1RDPn / E1RNRZn and E1RDNn output delay after E1RCKn↑	$t_{D(1)}$			10	ns

Figure 12. External Clocks Interface Timing



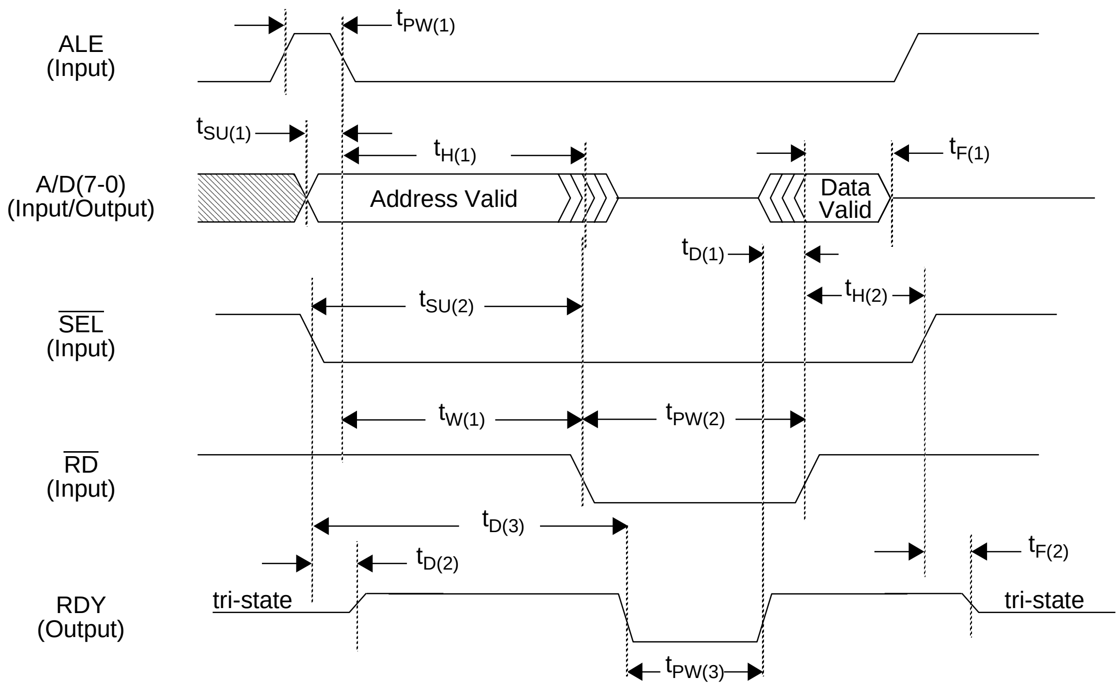
Parameter	Symbol	Min	Typ	Max	Unit
XCLK clock frequency			34368 ± 20 ppm		kHz
XCLK clock high time	$t_{PWH(1)}$	45	50	55	%
XCLK clock low time	$t_{PWL(1)}$	45	50	55	%
E2AISC clock frequency			8448 ± 30 ppm		kHz
E2AISC clock high time	$t_{PWH(2)}$	40	50	60	%
E2AISC clock low time	$t_{PWL(2)}$	40	50	60	%

Figure 13. Boundary Scan Timing



Parameter	Symbol	Min	Typ	Max	Unit
TCK clock high time	t_{PWH}	50			ns
TCK clock low time	t_{PWL}	50			ns
TMS set-up time before TCK↑	$t_{SU(1)}$	12			ns
TMS hold time after TCK↑	$t_{H(1)}$	12			ns
TDI set-up time before TCK↑	$t_{SU(2)}$	12			ns
TDI hold time after TCK↑	$t_{H(2)}$	12			ns
TDO delay after TCK↓	t_D	0.0		15	ns

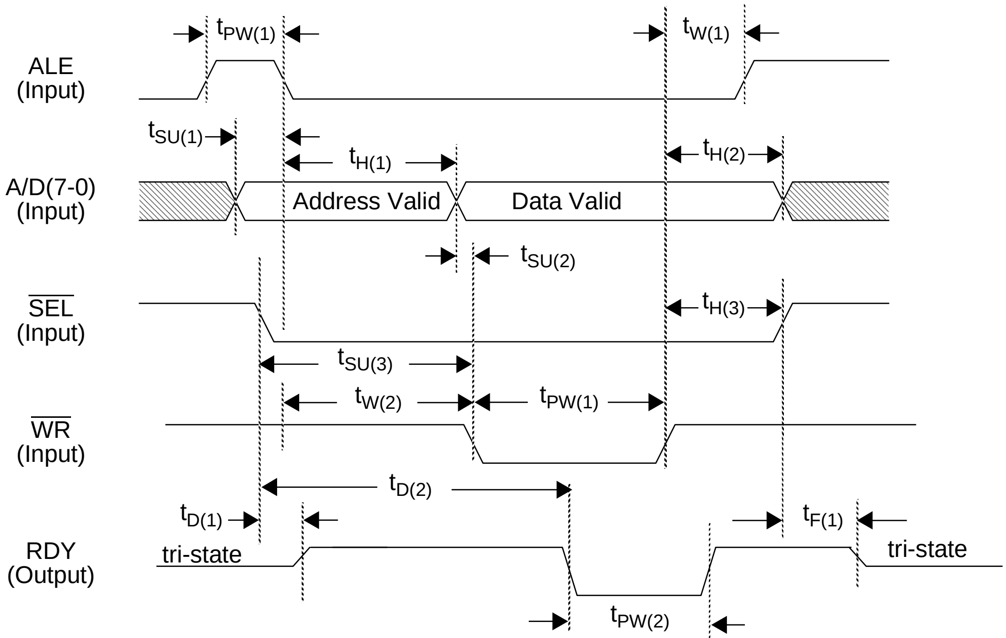
Figure 14. Multiplex Mode - Microprocessor Read Cycle Timing



Note: The signal E2AISC is required for proper operation of the microprocessor interface.

Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	4.0			ns
A/D(7-0) address set-up time before ALE↓	$t_{SU(1)}$	0.0			ns
A/D(7-0) address hold time after ALE↓	$t_{H(1)}$	12			ns
A/D(7-0) data output delay to tri-state after $\overline{\text{RD}}$↑	$t_{F(1)}$			7.0	ns
A/D(7-0) data available output delay after RDY↑	$t_{D(1)}$			0.0	ns
$\overline{\text{RD}}$ pulse width	$t_{PW(2)}$	425			ns
$\overline{\text{SEL}}$↓ set-up time to $\overline{\text{RD}}$↓	$t_{SU(2)}$	0.0			ns
$\overline{\text{SEL}}$ hold time after $\overline{\text{RD}}$↑	$t_{H(2)}$	0.0			ns
$\overline{\text{RD}}$ wait after ALE↓	$t_{W(1)}$	0.0			ns
RDY↑ delay after $\overline{\text{SEL}}$↓	$t_{D(2)}$			8.0	ns
RDY↓ delay after $\overline{\text{SEL}}$↓	$t_{D(3)}$			10	ns
RDY float time after $\overline{\text{SEL}}$↑	$t_{F(2)}$			5.0	ns
RDY pulse width	$t_{PW(3)}$	295	355	420	ns

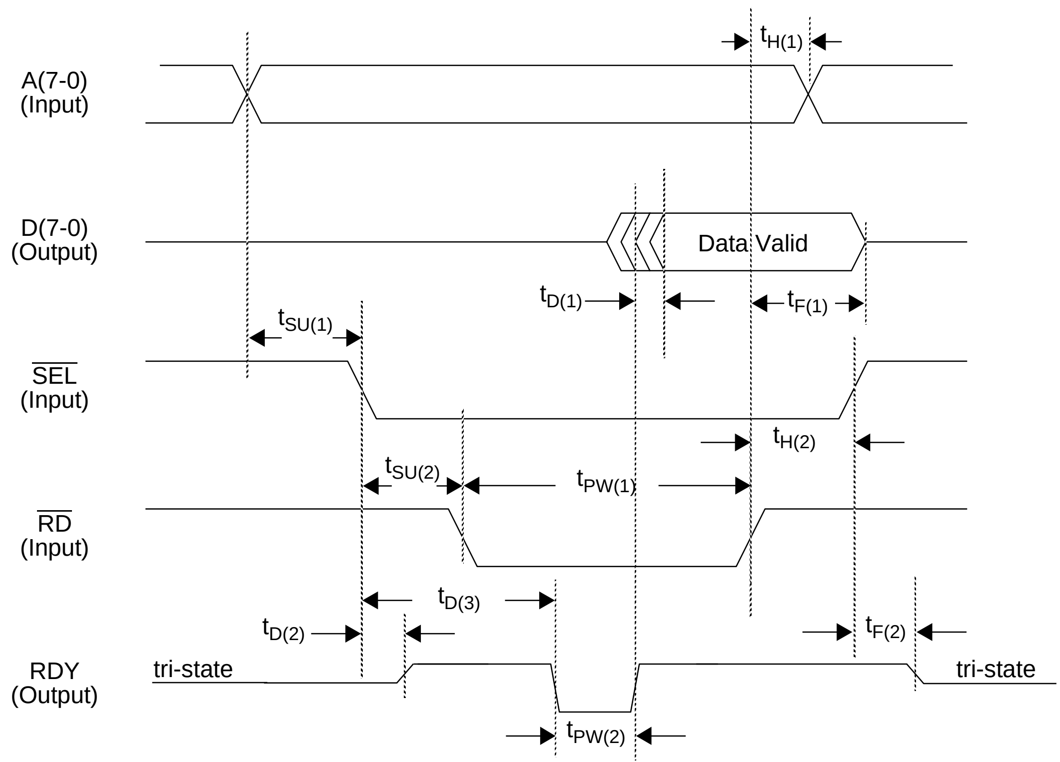
Figure 15. Multiplex Mode - Microprocessor Write Cycle Timing



Note: The signal E2AISC is required for proper operation of the microprocessor interface.

Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	4.0			ns
ALE wait after $\overline{\text{WR}}\uparrow$	$t_{W(1)}$	0.0			ns
A/D(7-0) address set-up time before ALE$\downarrow$	$t_{SU(1)}$	0.0			ns
A/D(7-0) address hold time after ALE$\downarrow$	$t_{H(1)}$	12			ns
A/D(7-0) data input set-up time to $\overline{\text{WR}}\downarrow$	$t_{SU(2)}$	0.0			ns
A/D(7-0) data input hold time after $\overline{\text{WR}}\uparrow$	$t_{H(2)}$	0.0			ns
$\overline{\text{SEL}}\downarrow$ set-up time to $\overline{\text{WR}}\downarrow$	$t_{SU(3)}$	0.0			ns
$\overline{\text{SEL}}$ hold time after $\overline{\text{WR}}\uparrow$	$t_{H(3)}$	0.0			ns
$\overline{\text{WR}}$ wait after ALE$\downarrow$	$t_{W(2)}$	0.0			ns
$\overline{\text{WR}}$ pulse width	$t_{PW(1)}$	425			ns
RDY$\uparrow$ delay after $\overline{\text{SEL}}\downarrow$	$t_{D(1)}$			8.0	ns
RDY$\downarrow$ delay after $\overline{\text{SEL}}\downarrow$	$t_{D(2)}$			10	ns
RDY float time after $\overline{\text{SEL}}\uparrow$	$t_{F(1)}$			5.0	ns
RDY pulse width	$t_{PW(2)}$	295	355	420	ns

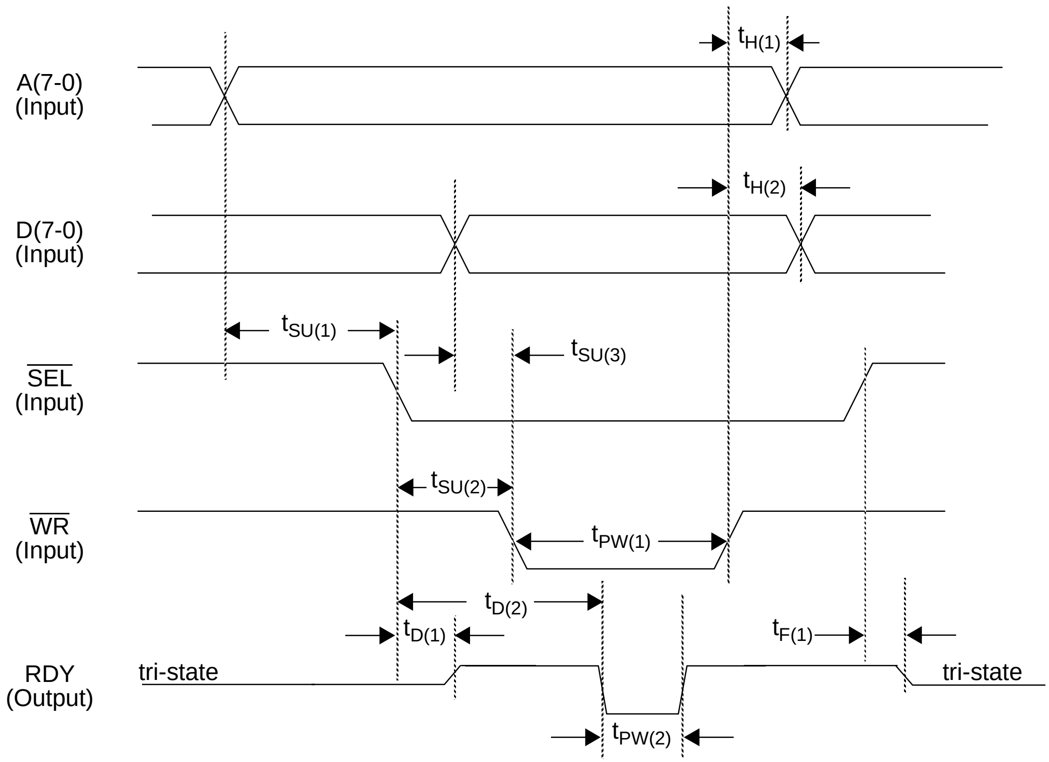
Figure 16. Intel Mode - Microprocessor Read Cycle Timing



Note: The signal E2AISC is required for proper operation of the microprocessor interface.

Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{RD}$↑	$t_{H(1)}$	0.0			ns
A(7-0) address set-up time before $\overline{SEL}$↓	$t_{SU(1)}$	0.0			ns
D(7-0) data output valid delay after RDY↑	$t_{D(1)}$			0.0	ns
D(7-0) data output float time after $\overline{RD}$↑	$t_{F(1)}$			7.0	ns
$\overline{SEL}$↓ set-up time to $\overline{RD}$↓	$t_{SU(2)}$	0.0			ns
$\overline{RD}$ pulse width	$t_{PW(1)}$	425			ns
$\overline{SEL}$↓ hold time after $\overline{RD}$↑	$t_{H(2)}$	0.0			ns
RDY↑ delay after $\overline{SEL}$↓	$t_{D(2)}$			8.0	ns
RDY↓ delay after $\overline{SEL}$↓	$t_{D(3)}$			10	ns
RDY float time after $\overline{SEL}$↑	$t_{F(2)}$			5.0	ns
RDY pulse width	$t_{PW(2)}$	295	355	420	ns

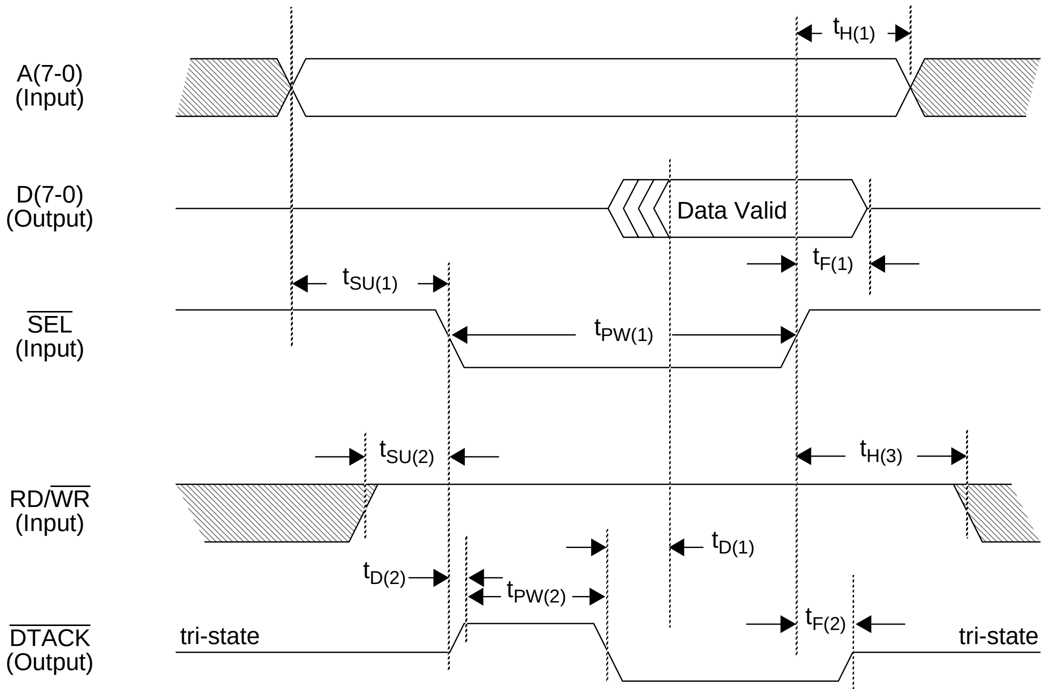
Figure 17. Intel Mode - Microprocessor Write Cycle Timing



Note: The signal E2AISC is required for proper operation of the microprocessor interface.

Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{WR}$↑	$t_{H(1)}$	0.0			ns
A(7-0) address set-up time before $\overline{SEL}$↓	$t_{SU(1)}$	0.0			ns
D(7-0) data input hold time after $\overline{WR}$↑	$t_{H(2)}$	0.0			ns
D(7-0) data input valid set-up time to $\overline{WR}$↓	$t_{SU(3)}$	0.0			ns
$\overline{SEL}$↓ set-up time to $\overline{WR}$↓	$t_{SU(2)}$	0.0			ns
$\overline{WR}$ pulse width	$t_{PW(1)}$	425			ns
RDY↑ delay after $\overline{SEL}$↓	$t_{D(1)}$			8.0	ns
RDY↓ delay after $\overline{SEL}$↓	$t_{D(2)}$			10	ns
RDY float time after $\overline{SEL}$↑	$t_{F(1)}$			5.0	ns
RDY pulse width	$t_{PW(2)}$	295	355	420	ns

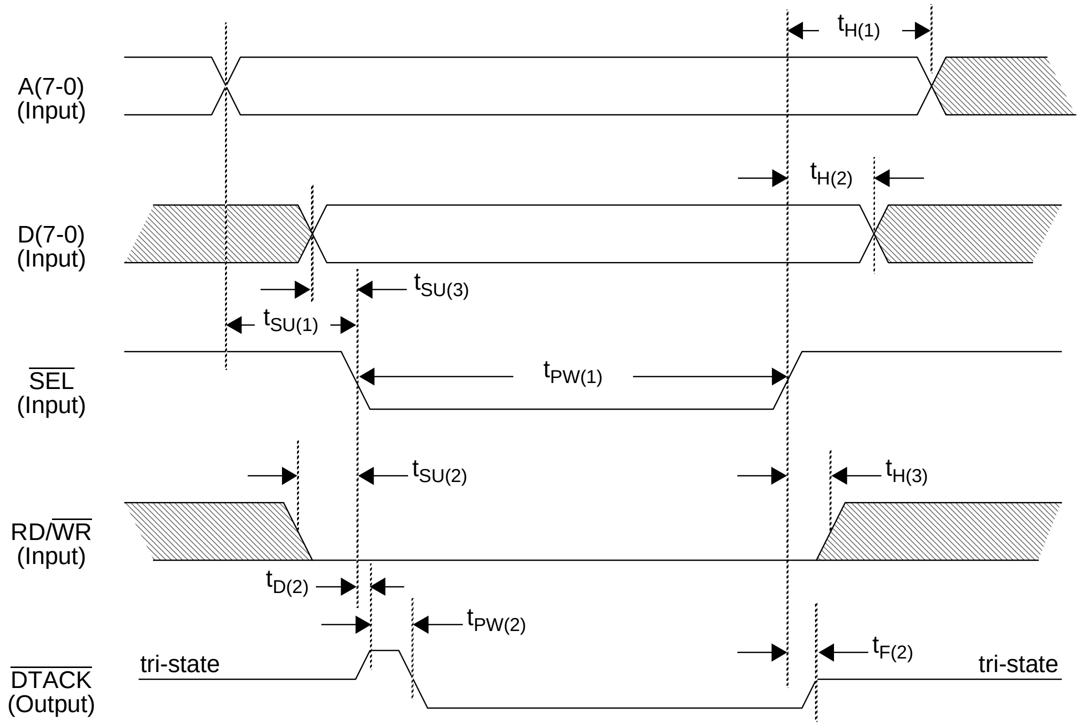
Figure 18. Motorola Mode - Microprocessor Read Cycle Timing



Note: The signal E2AISC is required for proper operation of the microprocessor interface.

Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{\text{SEL}}$↑	$t_{H(1)}$	0.0			ns
A(7-0) address valid set-up time before $\overline{\text{SEL}}$↓	$t_{SU(1)}$	0.0			ns
D(7-0) data output valid delay after $\overline{\text{DTACK}}$↓	$t_{D(1)}$			0.0	ns
D(7-0) data output float time after $\overline{\text{SEL}}$↑	$t_{F(1)}$			6.2	ns
$\overline{\text{SEL}}$ pulse width	$t_{PW(1)}$	427			ns
RD/$\overline{\text{WR}}$↑ set-up time before $\overline{\text{SEL}}$↓	$t_{SU(2)}$	0.0			ns
RD/$\overline{\text{WR}}$↑ hold time after $\overline{\text{SEL}}$↑	$t_{H(3)}$	0.0			ns
$\overline{\text{DTACK}}$↑ delay after $\overline{\text{SEL}}$↓	$t_{D(2)}$			8.0	ns
$\overline{\text{DTACK}}$ float time after $\overline{\text{SEL}}$↑	$t_{F(2)}$			5.0	ns
$\overline{\text{DTACK}}$ pulse width	$t_{PW(2)}$	300	360	425	ns

Figure 19. Motorola Mode - Microprocessor Write Cycle Timing



Note: The signal E2AISC is required for proper operation of the microprocessor interface.

Parameter	Symbol	Min	Typ	Max	Unit
A(7-0) address hold time after $\overline{\text{SEL}}$↑	$t_{H(1)}$	0.0			ns
A(7-0) address set-up time before $\overline{\text{SEL}}$↓	$t_{SU(1)}$	0.0			ns
D(7-0) data input hold time after $\overline{\text{SEL}}$↑	$t_{H(2)}$	0.0			ns
D(7-0) data input valid set-up before $\overline{\text{SEL}}$↓	$t_{SU(3)}$	0.0			ns
$\overline{\text{SEL}}$ pulse width	$t_{PW(1)}$	427			ns
RD/$\overline{\text{WR}}$↓ set-up time before $\overline{\text{SEL}}$↓	$t_{SU(2)}$	0.0			ns
RD/$\overline{\text{WR}}$↓ hold time after $\overline{\text{SEL}}$↑	$t_{H(3)}$	0.0			ns
$\overline{\text{DTACK}}$↑ delay after $\overline{\text{SEL}}$↓	$t_{D(2)}$			8.0	ns
$\overline{\text{DTACK}}$ float time after $\overline{\text{SEL}}$↑	$t_{F(2)}$			5.0	ns
$\overline{\text{DTACK}}$ pulse width	$t_{PW(2)}$	300	360	425	ns

OPERATION

TEST ACCESS PORT

Introduction

The five-pin Test Access Port (TAP) block provides external boundary scan functions to read and write the external I/O pins from the TAP for board and component test.

Boundary scan is a specialized scan architecture that provides observability and controllability for the interface pins of the device. As shown in Figure 20, one cell of a boundary scan register is assigned to each input or output pin to be observed or tested (bidirectional pins may have two cells). Some pins may not be observable or controllable. The boundary scan capability is based on a Test Access Port (TAP) controller, instruction and bypass registers, and a boundary scan register bordering the input and output pins. The boundary scan test bus interface consists of four input signals (Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{TRS}$)) and a Test Data Output (TDO) output signal. Boundary scan signal timing is shown in Figure 13. The TDI, TMS and $\overline{TRS}$ pins have internal pull-up resistors.

The TAP controller receives external control information via a Test Clock (TCK) signal and a Test Mode Select (TMS) signal, and sends control signals to the internal scan paths. The serial scan path architecture consists of an instruction register, a boundary scan register, a bypass register and a device identification register. These four serial registers are connected in parallel between the Test Data Input (TDI) and Test Data Output (TDO) signals, as shown in Figure 20.

The boundary scan function can be reset and disabled by holding pin $\overline{TRS}$ low. Specific control of the $\overline{TRS}$ pin is required to ensure that the boundary scan logic does not interfere with normal device operation. This pin must be either held low, or asserted low, then high (pulsed low) for a minimum of 500 ns to asynchronously reset the TAP controller. If boundary scan testing is to be performed and the $\overline{TRS}$ pin is held low, a pull-down resistor value must be chosen allowing the tester the ability to drive this pin high. When boundary scan testing is not being performed the boundary scan register is transparent, allowing the input and output signals to pass to and from the E123MUX device's internal logic. During boundary scan testing, the boundary scan register may disable the normal flow of input and output signals to allow the device to be controlled and observed via scan operations.

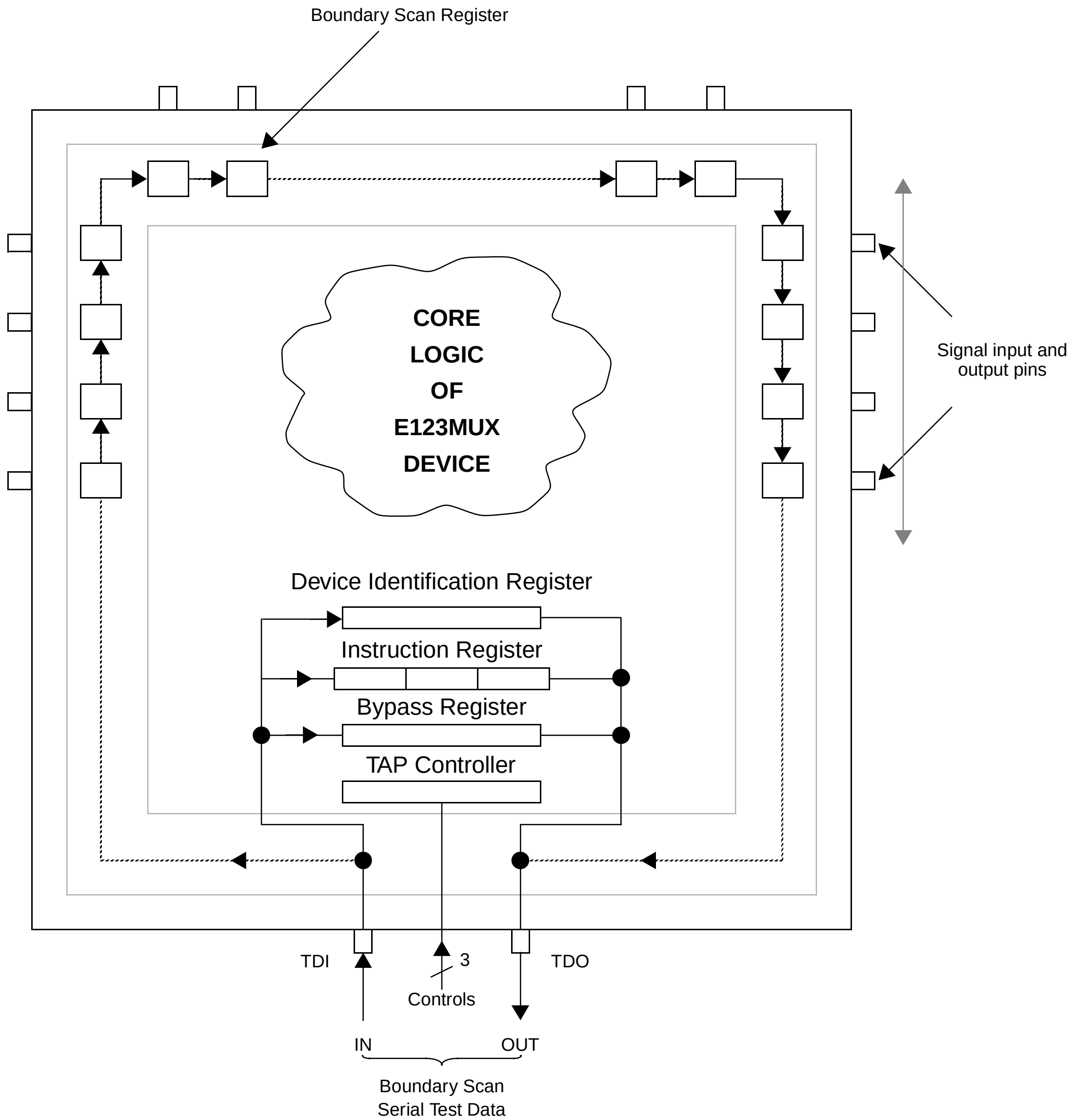
Boundary Scan Operation

The maximum frequency the E123MUX device will support for boundary scan is 10 MHz. The timing diagrams for the boundary scan interface pins are shown in Figure 13.

The E123MUX device performs the following four boundary scan test instructions:

> The EXTEST test instruction (000) provides the ability to test the connectivity of the E123MUX device to external circuitry.
>
> The SAMPLE test instruction (010) provides the ability to examine the boundary scan register contents without interfering with device operation.
>
> The IDCODE test instruction (001) allows the loading of the internal Device Identification Register, and the shifting of its contents without interfering with normal device operation.
>
> The BYPASS test instruction (111) provides the ability to bypass the E123MUX boundary scan and instruction registers.

Figure 20. Boundary Scan Schematic



Boundary Scan Chain

A boundary scan description language (BSDL) source file will be available via the Products page of the TranSwitch World Wide Web site (www.transwitch.com), which contains implementation details.

INITIALIZATION SEQUENCE

Please refer to the Memory Map and Memory Map Descriptions sections for information on all memory registers. All the memory register bit locations that are assigned for control purposes power up to the states indicated in the control bit descriptions. They go to the same states when a low is applied to the $\overline{\text{RESET}}$ pin (pin 70).

Unused registers must not be written to unless otherwise noted, since they may have been assigned functions for manufacturing test purposes.

The table in the next section shows the power-up states of the E123MUX memory registers and the following Sample Configurations section provides examples of how to configure those registers to set up the device as an E13 Skip Mux or as an E12/E23 Split Mux.

Power-Up Default Register Values.

The table below shows the default states of the memory registers following power-up or hardware reset. Addresses 00-03 contain fixed values. Please note that the bits in the shaded cells are not used, while X indicates an indeterminate bit that may be 0 or 1.

Address (Hex)	Bit Position							
	7	6	5	4	3	2	1	0
00	Manufacturer ID, LS 7 bits (1101011)							1
01	Part Number, LS Nibble (0001)				Manufacturer ID, MS Nibble (0000)			
02	Part Number, Middle Nibbles (11010010)							
03	Version (0000), may vary				Part Number, MS Nibble (0000)			
04	0	0	0	0	0	0	0	0
05	0	0	0	0	0	0	0	0
06	0	0	0	0	0	0	0	0
07	0	0	0	0	0	0	0	0
0A	0	0	0	0	0	0	0	0
0B	0	0	0	0	0	0	0	0
0C	0	0	0	0	0	0	0	0
0D	0	0	0	0	0	0	0	0
0E	0	0	0	0	0	0	0	0
0F	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0
11	0	1	1	0	0	0	1	1
12	1	1	0	1	1	1	1	1
20	X	X	X	X	0	0	0	0
21	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0
23	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0

Address (Hex)	Bit Position							
	7	6	5	4	3	2	1	0
25	0	0	0	0	0	0	0	0
26	0	0	0	0	0	0	0	0
27	0	0	0	0	0	0	0	0
28	0	0	0	0	0	0	0	0
29	0	0	0	0	0	0	0	0
2A	0	0	0	0	0	0	0	0
2B	X	X	X	X	0	0	0	0
30	X	X	X	X	0	0	0	0
31	0	0	0	0	0	0	0	0
32	0	0	0	0	0	0	0	0
33	0	0	0	0	0	0	0	0
34	0	0	0	0	0	0	0	0
35	0	0	0	0	0	0	0	0
36	0	0	0	0	0	0	0	0
37	0	0	0	0	0	0	0	0
38	0	0	0	0	0	0	0	0
39	0	0	0	0	0	0	0	0
3A	0	0	0	0	0	0	0	0
3B	X	X	X	X	0	0	0	0
40	X	X	X	X	0	0	0	0
41	0	0	0	0	0	0	0	0
42	0	0	0	0	0	0	0	0
43	0	0	0	0	0	0	0	0
44	0	0	0	0	0	0	0	0
45	0	0	0	0	0	0	0	0
46	0	0	0	0	0	0	0	0
47	0	0	0	0	0	0	0	0
48	0	0	0	0	0	0	0	0
49	0	0	0	0	0	0	0	0
4A	0	0	0	0	0	0	0	0
4B	X	X	X	X	0	0	0	0
50	X	X	X	X	0	0	0	0
51	0	0	0	0	0	0	0	0
52	0	0	0	0	0	0	0	0
53	0	0	0	0	0	0	0	0

Address (Hex)	Bit Position							
	7	6	5	4	3	2	1	0
54	0	0	0	0	0	0	0	0
55	0	0	0	0	0	0	0	0
56	0	0	0	0	0	0	0	0
57	0	0	0	0	0	0	0	0
58	0	0	0	0	0	0	0	0
59	0	0	0	0	0	0	0	0
5A	0	0	0	0	0	0	0	0
5B	X	X	X	X	0	0	0	0
60	0	0	0	0	1	1	1	1
61	1	0	0	0	0	0	0	0
63	0	0	0	0	0	0	0	0
64	0	0	0	0	0	0	0	0
65	X	X	0	0	0	0	0	X
66	0	0	0	0	0	0	0	0
67	X	X	0	0	0	0	0	X
6B	0	0	0	0	0	0	0	0
6C	0	0	0	0	0	0	0	0
6D	0	0	0	0	0	0	0	0
70	0	0	0	0	1	1	1	1
71	1	0	0	0	0	0	0	0
73	0	0	0	0	0	0	0	0
74	0	0	0	0	0	0	0	0
75	X	X	0	0	0	0	0	X
76	0	0	0	0	0	0	0	0
77	X	X	0	0	0	0	0	X
7B	0	0	0	0	0	0	0	0
7C	0	0	0	0	0	0	0	0
7D	0	0	0	0	0	0	0	0
80	0	0	0	0	1	1	1	1
81	1	0	0	0	0	0	0	0
83	0	0	0	0	0	0	0	0
84	0	0	0	0	0	0	0	0
85	X	X	0	0	0	0	0	X
86	0	0	0	0	0	0	0	0
87	X	X	0	0	0	0	0	X

Address (Hex)	Bit Position							
	7	6	5	4	3	2	1	0
8B	0	0	0	0	0	0	0	0
8C	0	0	0	0	0	0	0	0
8D	0	0	0	0	0	0	0	0
90	0	0	0	0	1	1	1	1
91	1	0	0	0	0	0	0	0
93	0	0	0	0	0	0	0	0
94	0	0	0	0	0	0	0	0
95	X	X	0	0	0	0	0	X
96	0	0	0	0	0	0	0	0
97	X	X	0	0	0	0	0	X
9B	0	0	0	0	0	0	0	0
9C	0	0	0	0	0	0	0	0
9D	0	0	0	0	0	0	0	0
A1	0	0	0	0	0	0	0	0
A2	0	0	0	0	0	0	0	0
A3	0	0	0	0	0	0	0	0
A4	0	0	0	0	0	0	0	0
A5	X	X	0	0	0	0	0	X
A6	0	0	0	0	0	0	0	0
A7	X	X	0	0	0	0	0	X
A8	0	0	0	0	1	1	1	1
AA	0	0	0	0	0	0	0	0
AB	0	0	0	0	0	0	0	0
AC	0	0	0	0	0	0	0	0
B0	0	0	0	0	0	0	0	0
B1	0	0	0	0	0	0	0	0
B6	X	X	X	X	0	0	0	0
B7	0	0	0	0	0	0	0	0
B9	0	0	0	0	0	0	0	0

Note: The shaded boxes represent undefined bit locations and X = indeterminate value.

SAMPLE CONFIGURATIONS

E13 Skip Mux Configuration:

The following table shows the basic register configuration required to set up the E123MUX device as an E1 to E3 Skip Mux following a hardware reset ($\overline{RESET}$, pin 70). All Register Address and Data values are shown in hexadecimal.

All E1 I/Os and the E3 I/O will be set up as NRZ Interfaces. All E1, E2, and E3 AIS are set to off. All E1 channels are active. All E1 DPLLs are on. There are no loopbacks.

Additional registers can be configured according to user needs.

Register Address (H)	Register Name	Data (H)	Functional Description
04	E1 Control	20	Each E1RCKn clocks out data on its positive edge (RE1CS=1)
0A	E1 Control	FF	E1 NRZ On, E1 #1 thru E1 #8 (CnNRZ=1)
0B	E1 Control	FF	E1 NRZ On, E1 #9 thru E1 #16 (CnNRZ=1)
0C	E1 Loopback	00	No E1 Loopback, E1 #1 thru E1 #8 (CHnLB=0)
0D	E1 Loopback	00	No E1 Loopback, E1 #9 thru E1 #16 (CHnLB=0)
0E	E12 Loopback	00	No E12 loopbacks, E12 #1 thru E12 #4 (E12LLm, E12RLm=0)
0F	E23 Loopback	00	No E23 Loopbacks, E23 #1 thru E23 #4 (E23RLm=0)
10	E3 Loopback	00	No E3 loopbacks (E3RLB, E3LLB=0)
60	E1 Control	00	E1 AIS Off, E1 #1 thru E1 #4 (CnAIS=0)
61	E1 Control	00	E1 DPLLs On, E1 #1 thru E1 #4 (BPPLL1=0)
70	E1 Control	00	E1 AIS Off, E1 #5 thru E1 #8 (CnAIS=0)
71	E1 Control	00	E1 DPLLs On, E1 #5 thru E1 #8 (BPPLL2=0)
80	E1 Control	00	E1 AIS Off, E1 #9 thru E1 #12 (CnAIS=0)
81	E1 Control	00	E1 DPLLs On, E1 #9 thru E1 #12 (BPPLL3=0)
90	E1 Control	00	E1 AIS Off, E1 #13 thru E1 #16 (CnAIS=0)
91	E1 Control	00	E1 DPLLs On, E1 #13 thru E1 #16 (BPPLL4=0)
A8	E23 Control	00	E23 AIS Off, E23 #1 thru E23 #4 (E23AISm=0)
B0	E3 Control	22	E3 NRZ On, E3RCKI negative edge clocking (E3NRZ, RE3CS=1)
B6	FIFO Centering Control	0F	Sets all E12, E23 FIFOs to robust centering mode
B9	Configuration	80	Selects E13 Mux mode (E13M=1)

E12/E23 Split Mux Configuration:

The following table shows the basic register configuration required to set up the E123MUX device as an E1/E2 or E2/E3 Split Mux following a hardware reset ($\overline{RESET}$, pin 70). All Register Address and Data values are shown in hexadecimal.

All E1 I/Os will be set up as dual unipolar interfaces. The E3 I/O will be set up as an NRZ interface. All E1, E12, E23, and E3 AIS are set to off. All E1 channels are active. All E1 DPLLs are on. There are no loopbacks.

Additional registers can be configured according to user needs.

Register Address (H)	Register Name	Data (H)	Functional Description
04	E1 Control	20	Each E1RCKn clocks out data on its positive edge (RE1CS=1)
0A	E1 Control	00	E1 NRZ Off, E1 #1 thru E1 #8 (CnNRZ=0)
0B	E1 Control	00	E1 NRZ Off, E1 #9 thru E1#16 (CnNRZ=0)
0C	E1 Loopback	00	No E1 Loopback, E1 #1 thru E1 #8 (CHnLB=0)
0D	E1 Loopback	00	No E1 Loopback, E1 #9 thru E1 #16 (CHnLB=0)
0E	E12 Loopback	00	No E12 loopbacks, E12 #1 thru E12 #4 (E12LLm, E12RLm=0)
0F	E23 Loopback	00	No E23 Loopbacks, E23 #1 thru E23 #4 (E23RLm=0)
10	E3 Loopback	00	No E3 loopbacks (E3RLB, E3LLB=0)
2A	E12 Control	60	Clock in E2 receive data on E12RCKm negative edge, and clock at E2 transmit data on E12TCKOm positive edge, for m = 1 - 4 (R12CSm, T12CSm=1)
3A	E12 Control	60	
4A	E12 Control	60	
5A	E12 Control	60	
60	E1 Control	00	E1 AIS Off, E1 #1 thru E1 #4 (CnAIS=0)
61	E1 Control	00	E1 DPLLs On, E1 #1 thru E1 #4 (BPPLL1=0)
70	E1 Control	00	E1 AIS Off, E1 #5 thru E1 #8 (CnAIS=0)
71	E1 Control	00	E1 DPLLs On, E1 #5 thru E1 #8 (BPPLL2=0)
80	E1 Control	00	E1 AIS Off, E1 #9 thru E1 #12 (CnAIS=0)
81	E1 Control	00	E1 DPLLs On, E1 #9 thru E1 #12 (BPPLL3=0)
90	E1 Control	00	E1 AIS Off, E1 #13 thru E1 #16 (CnAIS=0)
91	E1 Control	00	E1 DPLLs On, E1 #13 thru E1 #16 (BPPLL4=0)
A8	E23 Control	00	E23 AIS Off, E23 #1 thru E23 #4 (E23AISm=0)
B0	E3 Control	22	E3 NRZ On, E3RCKI negative edge clocking (E3NRZ, RE3CS=1)
B6	FIFO Centering Control	0F	Sets all E12/E23 FIFOs to robust centering mode
B7	E23 Control	00	E23TCKm positive edge clocking, E23RCKm negative edge clocking, for E23 #m, m= 4 -1 (T23CSm, R23CSm=0)
B9	Configuration	00	Selects E12/E23 Split Mux mode (E13M=0)

ALARM AND INTERRUPT INDICATIONS

Unlatched alarm indication bits are provided in read only registers of the memory map to indicate the current status of an alarm, with 1 indicating alarm presence and 0 indicating alarm absence. Latched alarm indication bits are provided in read only (latched) registers. Each is automatically set to 1 when the corresponding unlatched alarm indication bit changes from 0 to 1, and it then remains at 1 until it is reset to 0 by having a 1 written to it from the microprocessor. Once it is reset, it remains at 0 until the next 0 to 1 transition of the corresponding unlatched alarm indication bit sets it to 1.

Interrupt indication bits are provided in bits 6-0 of the read/write register at address 07H. Each is automatically set to 1 when any one or more of the associated unlatched alarm indication bits changes from 0 to 1 or from 1 to 0, provided that the corresponding alarm interrupt mask bit provided in a read/write register has been set to 0 (a 1 masks the alarm from causing an interrupt). The interrupt indication bit remains at 1 until it is reset to 0 by having a 1 written to it. The software interrupt indication bit INT at bit 7 of address 07H is automatically set to 1 when any one or more of bits 6-0 is set to 1, and it remains at 1 until a 1 is written to reset it to 0. The hardware interrupt, INT or INT/$\overline{\text{IRQ}}$ at pin 65, is active while bit INT is 1 and inactive while it is 0.

Since the interrupt indication bit also provides an interrupt after an alarm is terminated, it is necessary for the interrupt servicing routine of the microprocessor to discriminate the interrupts that do correspond to new alarms. If the microprocessor resets both the interrupt indication bit and its associated, active, latched alarm indication bit(s) immediately after analyzing an interrupt, then a check on the status of the corresponding unmasked latched alarm indication bits for a new interrupt will reveal when it has been caused by an unlatched alarm indication bit changing from 1 to 0 at the termination of an alarm condition, since none of these latched bits will then be found to be in the 1 state.

THROUGHPUT DELAYS

The throughput delays of the E123MUX device operating in the E123 mode (E13 Skip Mux) are as shown in the table below:

Path	Delay
E1 to E2	14 E1 Clock Cycles
E2 to E3	14 E2 Clock Cycles
E3 to E2	32 E2 Clock Cycles
E2 to E1	32 E1 Clock Cycles

MEMORY MAP

The E123MUX memory map consists of register bit positions and counters which may be accessed by the microprocessor. The memory map segment consists of 256 address locations. Address locations in the range 00H - FFH that are unlisted must not be accessed by the microprocessor. Individual bit positions within register locations that are shown as Not Used (N.U.) will contain unspecified values (X) when read, unless a 0 or 1 value is indicated in the Power-Up Default Register Values section or in the tables below as the fixed (R) or power-up (R/W) state, or the address can be written by the microprocessor, in which case unused bit positions must always be set to 0 when the register is written. The memory map contains the device ID, configuration register, various functional control and alarm registers, bit error threshold registers, a functional scan register, interrupt status registers and mask bits, and several counters for error condition occurrences.

DEVICE IDENTIFIER

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	R	Manufacturer ID LS 7 bits (1101011)							1
01	R	Part Number LS Nibble (0001)				Manufacturer ID MS 4 bits (0000)			
02	R	Part Number Middle Nibbles (11010010)							
03	R	Version (0000), may vary				Part Number MS Nibble (0000)			

CONFIGURATION REGISTER

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B9	R/W	E13M	Not Used (0000000)						

E1 CONTROL AND ALARM REGISTERS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04	R/W	EPRBS	TE1CS	RE1CS	PRBSEN	TSEL3	TSEL2	TSEL1	TSEL0
05	R/W	Not Used (000)			ANLEN	RSEL3	RSEL2	RSEL1	RSEL0
60	R/W	Not Used (0000)				C4AIS	C3AIS	C2AIS	C1AIS
61	R/W	BPPLL1	Not Used (000)			C4LOL	C3LOL	C2LOL	C1LOL
70	R/W	Not Used (0000)				C8AIS	C7AIS	C6AIS	C5AIS
71	R/W	BPPLL2	Not Used (000)			C8LOL	C7LOL	C6LOL	C5LOL
80	R/W	Not Used (0000)				C12AIS	C11AIS	C10AIS	C9AIS
81	R/W	BPPLL3	Not Used (000)			C12LOL	C11LOL	C10LOL	C9LOL
90	R/W	Not Used (0000)				C16AIS	C15AIS	C14AIS	C13AIS
91	R/W	BPPLL4	Not Used (000)			C16LOL	C15LOL	C14LOL	C13LOL
0A	R/W	C8NRZ	C7NRZ	C6NRZ	C5NRZ	C4NRZ	C3NRZ	C2NRZ	C1NRZ
0B	R/W	C16NRZ	C15NRZ	C14NRZ	C13NRZ	C12NRZ	C11NRZ	C10NRZ	C9NRZ

* R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write

E12 CONTROL REGISTERS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2A	R/W	E12FE1	R12CS1	T12CS1	E12AIS1	E12RA1	E12SB1	Not used (00)	
3A	R/W	E12FE2	R12CS2	T12CS2	E12AIS2	E12RA2	E12SB2	Not used (00)	
4A	R/W	E12FE3	R12CS3	T12CS3	E12AIS3	E12RA3	E12SB3	Not used (00)	
5A	R/W	E12FE4	R12CS4	T12CS4	E12AIS4	E12RA4	E12SB4	Not used (00)	

E23 CONTROL REGISTERS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A8	R/W	Not Used (0000)				E23AIS4	E23AIS3	E23AIS2	E23AIS1
B7	R/W	T23CS4	R23CS4	T23CS3	R23CS3	T23CS2	R23CS2	T23CS1	R23CS1

E3 CONTROL REGISTER

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B0	R/W	E3FE	Not Used (0)	E3NRZ	E3AIS	E3RA	E3SB	RE3CS	TE3CS

E12, E23 FIFO CENTERING CONTROL REGISTER

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B6	R/W	Not Used (0000)				E23MCTR	E12MCTR	E23DCTR	E12DCTR

LOOPBACK CONTROL REGISTERS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0C	R/W	CH8LB	CH7LB	CH6LB	CH5LB	CH4LB	CH3LB	CH2LB	CH1LB
0D	R/W	CH16LB	CH15LB	CH14LB	CH13LB	CH12LB	CH11LB	CH10LB	CH9LB
0E	R/W	E12LL4	E12LL3	E12LL2	E12LL1	E12RL4	E12RL3	E12RL2	E12RL1
0F	R/W	Not Used (0000)				E23RL4	E23RL3	E23RL2	E23RL1
10	R/W	Not Used (000000)						E3RLB	E3LLB

* R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write

E2 AND E3 BIT ERROR THRESHOLD REGISTERS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
11	R/W	Set E2 BER Threshold							
12	R/W	Set E3 BER Threshold							

FUNCTIONAL TEST REGISTER

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B1	R/W	TranSwitch Test Register (do not access)							
BA	R/W	TranSwitch Test Register (do not access)							

INTERRUPT INDICATION REGISTER

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07	R/W	INT	E3	E2CH4	E2CH3	E2CH2	E2CH1	E1LOS 9-16	E1LOS 1-8

INTERRUPT MASK BITS REGISTERS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
21	R/W	Not Used (0000)				C4LSM	C3LSM	C2LSM	C1LSM
31	R/W	Not Used (0000)				C8LSM	C7LSM	C6LSM	C5LSM
41	R/W	Not Used (0000)				C12LSM	C11LSM	C10LSM	C9LSM
51	R/W	Not Used (0000)				C16LSM	C15LSM	C14LSM	C13LSM
66	R/W	Not Used (00)		E2SM1	E2RM1	E2BM1	E2LFM1	E2AM1	N.U. (0)
76	R/W	Not Used (00)		E2SM2	E2RM2	E2BM2	E2LFM2	E2AM2	N.U. (0)
86	R/W	Not Used (00)		E2SM3	E2RM3	E2BM3	E2LFM3	E2AM3	N.U. (0)
96	R/W	Not Used (00)		E2SM4	E2RM4	E2BM4	E2LFM4	E2AM4	N.U. (0)
A6	R/W	Not Used (00)		E3SPBM	E3REMM	E3BERM	E3LOFM	E3AISM	E3LOSM

* R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write

ALARM REGISTERS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20	R	Not Used (XXXX)				C4LOS	C3LOS	C2LOS	C1LOS
2B	R(L)	Not Used (XXXX)				C4LOS	C3LOS	C2LOS	C1LOS
30	R	Not Used (XXXX)				C8LOS	C7LOS	C6LOS	C5LOS
3B	R(L)	Not Used (XXXX)				C8LOS	C7LOS	C6LOS	C5LOS
40	R	Not Used (XXXX)				C12LOS	C11LOS	C10LOS	C9LOS
4B	R(L)	Not Used (XXXX)				C12LOS	C11LOS	C10LOS	C9LOS
50	R	Not Used (XXXX)				C16LOS	C15LOS	C14LOS	C13LOS
5B	R(L)	Not Used (XXXX)				C16LOS	C15LOS	C14LOS	C13LOS
65	R	Not Used (XX)		E2SPB1	E2RA1	E2BER1	E2LOF1	E2AIS1	N.U. (X)
67	R(L)	Not Used (XX)		E2SPB1	E2RA1	E2BER1	E2LOF1	E2AIS1	N.U. (X)
75	R	Not Used (XX)		E2SPB2	E2RA2	E2BER2	E2LOF2	E2AIS2	N.U. (X)
77	R(L)	Not Used (XX)		E2SPB2	E2RA2	E2BER2	E2LOF2	E2AIS2	N.U. (X)
85	R	Not Used (XX)		E2SPB3	E2RA3	E2BER3	E2LOF3	E2AIS3	N.U. (X)
87	R(L)	Not Used (XX)		E2SPB3	E2RA3	E2BER3	E2LOF3	E2AIS3	N.U. (X)
95	R	Not Used (XX)		E2SPB4	E2RA4	E2BER4	E2LOF4	E2AIS4	N.U. (X)
97	R(L)	Not Used (XX)		E2SPB4	E2RA4	E2BER4	E2LOF4	E2AIS4	N.U. (X)
A5	R	Not Used (XX)		E3SPB	E3RA	E3BER	E3LOF	E3AIS	E3LOS
A7	R(L)	Not Used (XX)		E3SPB	E3RA	E3BER	E3LOF	E3AIS	E3LOS

* R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write

COUNTERS

The low order byte in a 16-bit counter should be read first, followed by the high order byte.

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06	R	PRBS Error 8-bit Counter							
22-23	R	Channel 1 BPV 16-bit Counter (23H High Order Byte)							
24-25	R	Channel 2 BPV 16-bit Counter (25H High Order Byte)							
26-27	R	Channel 3 BPV 16-bit Counter (27H High Order Byte)							
28-29	R	Channel 4 BPV 16-bit Counter (29H High Order Byte)							
32-33	R	Channel 5 BPV 16-bit Counter (33H High Order Byte)							
34-35	R	Channel 6 BPV 16-bit Counter (35H High Order Byte)							
36-37	R	Channel 7 BPV 16-bit Counter (37H High Order Byte)							
38-39	R	Channel 8 BPV 16-bit Counter (39H High Order Byte)							
42-43	R	Channel 9 BPV 16-bit Counter (43H High Order Byte)							
44-45	R	Channel 10 BPV 16-bit Counter (45H High Order Byte)							
46-47	R	Channel 11 BPV 16-bit Counter (47H High Order Byte)							
48-49	R	Channel 12 BPV 16-bit Counter (49H High Order Byte)							
52-53	R	Channel 13 BPV 16-bit Counter (53H High Order Byte)							
54-55	R	Channel 14 BPV 16-bit Counter (55H High Order Byte)							
56-57	R	Channel 15 BPV 16-bit Counter (57H High Order Byte)							
58-59	R	Channel 16 BPV 16-bit Counter (59H High Order Byte)							
63	R	E12 Frame Error 8-bit Counter for Demux No. 1							
64	R	E12 Loss Of Frame Error 8-bit Counter No. 1							
6B-6C	R	E12 16-bit Frame Counter for Demux No. 1 (6C High Order Byte) - for BER Measurement							
6D	R	E12 8-bit Errored Frame Counter for Demux No. 1 - for BER Measurement							
73	R	E12 Frame Error 8-bit Counter for Demux No. 2							
74	R	E12 Loss Of Frame Error 8-bit Counter No. 2							
7B-7C	R	E12 16-bit Frame Counter for Demux No. 2 (7C High Order Byte) - for BER Measurement							
7D	R	E12 8-bit Errored Frame Counter for Demux No. 2 - for BER Measurement							
83	R	E12 Frame Error 8-bit Counter for Demux No. 3							
84	R	E12 Loss Of Frame Error 8-bit Counter No. 3							
8B-8C	R	E12 16-bit Frame Counter for Demux No. 3 (8C High Order Byte) - for BER Measurement							
8D	R	E12 8-bit Errored Frame Counter for Demux No. 3 - for BER Measurement							
93	R	E12 Frame Error 8-bit Counter for Demux No. 4							

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
94	R	E12 Loss Of Frame Error 8-bit Counter No. 4							
9B-9C	R	E12 16-bit Frame Counter for Demux No. 4 (9C High Order Byte) - for BER Measurement							
9D	R	E12 8-bit Errored Frame Counter for Demux No. 4 - for BER Measurement							
A1-A2	R	E3 BPV 16-bit Counter (A2 High Order Byte)							
A3	R	E3 Receive Frame Error 8-bit Counter							
A4	R	E3 Receive Loss Of Frame 8-bit Counter							
AA-AB	R	E3 16-bit Frame Counter (AB High Order Byte)							
AC	R	E3 8-bit Errored Frame Counter							

* R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write

UNUSED REGISTERS

The following registers are not used, and they do not require an initialization value: 08H, 09H, 13H-1FH, 2CH-2FH, 3CH-3FH, 4CH-4FH, 5CH-5FH, 68H-6AH, 6EH, 6FH, 78H-7AH, 7EH, 7FH, 88H-8AH, 8EH, 8FH, 98H-9AH, 9EH, 9FH, A9H, ADH-AFH, B2H-B5H, B8H and BBH through FFH.

MEMORY MAP DESCRIPTIONS

All memory addresses in this document are shown in hexadecimal, even when the suffix “H” is omitted.

DEVICE IDENTIFIER

The 32-bit Device Identifier (ID) in read-only addresses 00H - 03H includes the Manufacturer Identity code which is assigned by the Solid State Products Council (JEDEC). It also includes a part number code, a version code (which is set to zero for the initial design but may vary if the device is revised) and a fixed bit. The serial format for this Device ID is 00D210D7H, as shown below, where the MSB is at the left. The Manufacturer Identity for all TranSwitch chips is 107 decimal (06BH). The part number code for the E123MUX is 03361 (0D21H).

31 - 28	27 - 12	11 - 1	0
Address 03H, bits 7-4	Address 03H, bit 3 to Address 01H, bit 4	Address 01H, bit 3 to Address 00H, bit 1	Address 00H, bit 0
Version (4 bits, 0000, may vary)	Part Number (16 bits, 0D21H)	Manufacturer Identity (11 bits, 06BH)	Fixed Bit (1 bit, 1)
		◄ 12-bit value is 0D7H ►	

CONFIGURATION REGISTER

Address	Bit	Symbol	Description
B9	7	E13M	**E13 Multiplexer/Demultiplexer Enable:** A 1 enables the device to be configured as an E13 multiplexer/demultiplexer (16 E1 channels multiplexed to/from one E3 channel). A 0 enables the device to function as four E12 multiplexer/demultiplexers (16 E1 channels multiplexed to/from four E2 channels), and as an E23 multiplexer/demultiplexer (four E2 channels multiplexed to/from one E3 channel). This bit is set to 0 upon power-up.
	6-0	Not Used	**Not Used:** These bits power up in the zero state.

E1 CONTROL AND ALARM REGISTERS

Address	Bit	Symbol	Description
04	7	EPRBS	**Transmit Errored PRBS Pattern:** A single bit error in the PRBS pattern is transmitted continuously when this bit is written with a 1 and control bit PBRSEN (bit 4 in this register) is set to 1. When this bit is set to 0 with PBRSEN set to 1, an error-free PBRS pattern is transmitted. This bit is set to 0 upon power-up.
	6	TE1CS	**Transmit E1 Clock Sense:** A global control bit for all transmit E1 channels. A 0 enables the dual unipolar positive and negative rail signals or the NRZ signal to be clocked into the E123MUX on rising edges of the transmit clock (E1TCKn), while a 1 enables falling edges of the clock to be used for clocking in data. This bit is set to 0 upon power up.

Address	Bit	Symbol	Description
04 (cont.)	5	RE1CS	**Receive E1 Clock Sense:** A global control bit for all receive E1 channels. A 1 enables the unipolar positive and negative rail signals or the NRZ signal to be clocked out of the E123MUX on rising edges of the receive clock (E1RCKn), while a 0 enables falling edges of the clock to be used for clocking out data. This bit is set to 0 upon power-up.
	4	PRBSEN	**PRBS Generator Enable:** A 1 enables the E1 2^{15} -1 generator for the transmit E1 channel that is selected by control bits TSEL3-TSEL0. Transmit data for the selected channel is disabled when this bit is written with a 1. The PRBS generator is disabled when this bit is written with a 0. This bit is set to 0 upon power-up.
	3-0	TSEL3-TSEL0	**Transmit E1 Channel Selection for PRBS Pattern:** The transmit E1 channel selection control bits are enabled when control bit PRBSEN in this register is written with a 1. The E1 channel selected for PRBS pattern application is determined by these four bits, according to the following table: TSEL3 TSEL2 TSEL1 TSEL0 Channel Selected 0 0 0 0 Channel 1 (power-up state) 0 0 0 1 Channel 2 - - - - and so on, through channels 3-14 1 1 1 0 Channel 15 1 1 1 1 Channel 16
05	7-5	Not Used	**Not Used:** These bits power up in the zero state.
	4	ANLEN	**PRBS Analyzer Enable:** A 1 enables the E1 2^{15} -1 analyzer for the receive E1 channel that is selected by control bits RSEL3-RSEL0. Receive data (i.e., the PRBS pattern) is provided as a dual unipolar or NRZ signal. The PRBS analyzer is disabled when this bit is written with a 0. This bit is set to 0 upon power-up.
	3-0	RSEL3-RSEL0	**Receive E1 Channel Selection for PRBS Pattern:** The receive channel selection control bits are enabled when control bit ANLEN in this register is written with a 1. The E1 channel selected for PRBS pattern analysis is determined by these four bits, according to the following table: RSEL3 RSEL2 RSEL1 RSEL0 Channel Selected 0 0 0 0 Channel 1 (power-up state) 0 0 0 1 Channel 2 - - - - and so on, through channels 3-14 1 1 1 0 Channel 15 1 1 1 1 Channel 16
60	7-4	Not Used	**Not Used:** These bits power up in the zero state.
	3-0	CnAIS (n = 4-1)	**E1 Channels 4 - 1 Receive AIS Enable:** A 1 inserts AIS for receive E1 channel number n. Bit 3 represents channel 4. An AIS is defined as all ones in the asynchronous E1 data bit stream. These bits are set to 1 upon power-up.

Address	Bit	Symbol	Description
61	7	BPPLL1	**Bypass Internal DPLL for E1 Channels 4 - 1:** A 1 disables the internal receive DPLLs for channels 4 to 1. When disabled, a receive gapped clock (E1RCKn) is provided as an output clock for clocking out the receive data for channel n. A 0 enables the internal DPLLs for channels 4 - 1. For this mode of operation, the E1RCKn output clock for channels 4 - 1 is symmetrical. This bit is set to 1 upon power-up. Note: The E1 DPLLs require about 1 second of settling time after being enabled to ensure proper operation.
	6-4	Not Used	**Not Used:** These bits power up in the zero state.
	3-0	CnLOL (n = 4-1)	**Loss of Lock for E1 DPLL for Channels 4 - 1:** Enabled when control bit BPPLL1 is a 0. A 1 indicates that the DPLL for E1 channel n has exceeded the alarm range of the DPLL and that it is no longer in lock. Bit 3 represents channel 4.
70	7-4	Not Used	**Not Used:** These bits power up in the zero state.
	3-0	CnAIS (n = 8-5)	**E1 Channels 8 - 5 Receive AIS Enable:** A 1 inserts AIS for receive E1 channel number n. Bit 3 represents channel 8. An AIS is defined as all ones in the asynchronous E1 data bit stream. These bits are set to 1 upon power-up.
71	7	BPPLL2	**Bypass Internal DPLL for E1 Channels 8 - 5:** A 1 disables the internal receive DPLLs for channels 8 to 5. When disabled, a receive gapped clock (E1RCKn) is provided as an output clock for clocking out the receive data for channel n. A 0 enables the internal DPLLs for channels 8 - 5. For this mode of operation, the E1RCKn output clock for channels 8 - 5 is symmetrical. This bit is set to 1 upon power-up. Note: The E1 DPLLs require about 1 second of settling time after being enabled to ensure proper operation.
	6-4	Not Used	**Not Used:** These bits power up in the zero state.
	3-0	CnLOL (n = 8-5)	**Loss of Lock for E1 DPLL for Channels 8 - 5:** Enabled when control bit BPPLL2 is a 0. A 1 indicates that the DPLL for E1 channel n has exceeded the alarm range of the DPLL and that it is no longer in lock. Bit 3 represents channel 8.
80	7-4	Not Used	**Not Used:** These bits power up in the zero state.
	3-0	CnAIS (n = 12-9)	**E1 Channels 12 - 9 Receive AIS Enable:** A 1 inserts AIS for receive E1 channel number n. Bit 3 represents channel 12. An AIS is defined as all ones in the asynchronous E1 data bit stream. These bits are set to 1 upon power-up.

Address	Bit	Symbol	Description
81	7	BPPLL3	**Bypass Internal DPLL for E1 Channels 12 - 9:** A 1 disables the internal receive DPLLs for channels 12 to 9. When disabled, a receive gapped clock (E1RCKn) is provided as an output clock for clocking out the receive data for channel n. A 0 enables the internal DPLLs for channels 12 - 9. For this mode of operation, the E1RCKn output clock for channels 12 - 9 is symmetrical. This bit is set to 1 upon power-up. Note: The E1 DPLLs require about 1 second of settling time after being enabled to ensure proper operation.
	6-4	Not Used	**Not Used:** These bits power up in the zero state.
	3-0	CnLOL (n = 12-9)	**Loss of Lock for E1 DPLL for Channels 12 - 9:** Enabled when control bit BPPLL3 is a 0. A 1 indicates that the DPLL for E1 channel n has exceeded the alarm range of the DPLL and that it is no longer in lock. Bit 3 represents channel 12.
90	7-4	Not Used	**Not Used:** These bits power up in the zero state.
	3-0	CnAIS (n = 16-13)	**E1 Channels 16 - 13 Receive AIS Enable:** A 1 inserts AIS for receive E1 channel number n. Bit 3 represents channel 16. An AIS is defined as all ones in the asynchronous E1 data bit stream. These bits are set to 1 upon power-up.
91	7	BPPLL4	**Bypass Internal DPLL for E1 Channels 16 - 13:** A 1 disables the internal receive DPLLs for channels 16 to 13. When disabled, a receive gapped clock (E1RCKn) is provided as an output clock for clocking out the receive data for channel n. A 0 enables the internal DPLLs for channels 16 - 13. For this mode of operation, the E1RCKn output clock for channels 16 - 13 is symmetrical. This bit is set to 1 upon power-up. Note: The E1 DPLLs require about 1 second of settling time after being enabled to ensure proper operation.
	6-4	Not Used	**Not Used:** These bits power up in the zero state.
	3-0	CnLOL (n = 16-13)	**Loss of Lock for E1 DPLL For Channels 16 - 13:** Enabled when control bit BPPLL4 is a 0. A 1 indicates that the DPLL for E1 channel n has exceeded the alarm range of the DPLL and that it is no longer in lock. Bit 3 represents channel 16.
0A	7-0	CnNRZ (n = 8-1)	**E1 NRZ Interface for Channels 8 - 1 Enable:** A 1 written to a bit location in this register selects the corresponding E1 channel n (both receive and transmit interfaces) to be configured for NRZ receive and transmit interfaces. A 0 configures the E1 channel for unipolar (positive and negative rail) interfaces. Bit 7 represents E1 channel 8. This bit is set to 0 upon power-up.
0B	7-0	CnNRZ (n = 16-9)	**E1 NRZ Interface for Channels 16 - 9 Enable:** A 1 written to a bit location in this register selects the corresponding E1 channel n (both receive and transmit interfaces) to be configured for NRZ receive and transmit interfaces. A 0 configures the E1 channel for unipolar (positive and negative rail) interfaces. Bit 7 represents E1 channel 16. This bit is set to 0 upon power-up.

E12 CONTROL REGISTERS

Address	Bit	Symbol	Description
2A	7	E12FE1	**Insert E2 Framing Pattern Errors for E12 Multiplexer No. 1:** A 1 causes the insertion of one framing pattern error to be sent continuously in the E2 G.742 format for E12 multiplexer number 1 until this bit is set to 0. This corresponds to the E2 signal that is carrying E1 channels 1 through 4. This bit is set to 0 upon power-up.
	6	R12CS1	**Receive E12 Clock Sense Selection for Demultiplexer No. 1:** This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Receive E2 data for E12 demultiplexer number 1 is clocked in on rising edges of the clock (E12RCK1) when this bit is a 0, and on falling edges when this bit is a 1. This bit is set to 0 upon power-up.
	5	T12CS1	**Transmit E12 Clock Sense Selection for Multiplexer No. 1:** This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Transmit E2 data for E12 multiplexer number 1 is clocked out on rising edges of the clock (E12TCKO1) when this bit is a 1, and on falling edges when this bit is a 0. This bit is set to 0 upon power-up.
	4	E12AIS1	**E12 AIS Generation for E12 Multiplexer No. 1:** When set to 1, AIS is generated in the E2 G.742 format signal for E12 multiplexer number 1. AIS consists of all ones. This bit is set to 0 upon power-up.
	3	E12RA1	**E12 Remote Alarm Control for E12 Multiplexer No. 1:** When set to 1, the remote alarm bit (bit 11) in the E2 G.742 for E12 multiplexer number 1 is transmitted as a 1. When set to 0, the remote alarm bit is transmitted as a 0. This bit is set to 0 upon power-up.
	2	E12SB1	**E12 Spare Bit Control for E12 Multiplexer No. 1.** When set to 1, the spare bit (bit 12) in the E2 G.742 format for E12 multiplexer number 1 is transmitted as a 1. When set to 0, the spare bit is transmitted as a 0. This bit is set to 0 upon power-up.
	1-0	Not Used	**Not Used:** These bits power up in the zero state.

Address	Bit	Symbol	Description
3A	7	E12FE2	**Insert E2 Framing Pattern Errors for E12 Multiplexer No. 2:** A 1 causes the insertion of one framing pattern error to be sent continuously in the E2 G.742 format for E12 multiplexer number 2 until this bit is set to 0. This corresponds to the E2 signal that is carrying E1 channels 5 through 8. This bit is set to 0 upon power-up.
	6	R12CS2	**Receive E12 Clock Sense Selection for Demultiplexer No. 2:** This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Receive E2 data for E12 demultiplexer number 2 is clocked in on rising edges of the clock (E12RCK2) when this bit is a 0, and on falling edges when this bit is a 1. This bit is set to 0 upon power-up.
	5	T12CS2	**Transmit E12 Clock Sense Selection for Multiplexer No. 2:** This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Transmit E2 data for E12 multiplexer number 2 is clocked out on rising edges of the clock (E12TCKO2) when this bit is a 1, and on falling edges when this bit is a 0. This bit is set to 0 upon power-up.
	4	E12AIS2	**E12 AIS Generation for E12 Multiplexer No. 2:** When set to 1, AIS is generated in the E2 G.742 format signal for E12 multiplexer number 2. AIS consists of all ones. This bit is set to 0 upon power-up.
	3	E12RA2	**E12 Remote Alarm Control for E12 Multiplexer No. 2:** When set to 1, the remote alarm bit (bit 11) in the E2 G.742 for E12 multiplexer number 2 is transmitted as a 1. When set to 0, the remote alarm bit is transmitted as a 0. This bit is set to 0 upon power-up.
	2	E12SB2	**E12 Spare Bit Control for E12 Multiplexer No. 2.** When set to 1, the spare bit (bit 12) in the E2 G.742 format for E12 multiplexer number 2 is transmitted as a 1. When set to 0, the spare bit is transmitted as a 0. This bit is set to 0 upon power-up.
	1-0	Not Used	**Not Used:** These bits power up in the zero state.

Address	Bit	Symbol	Description
4A	7	E12FE3	**Insert E2 Framing Pattern Errors for E12 Multiplexer No. 3:** A 1 causes the insertion of one framing pattern error to be sent continuously in the E2 G.742 format for E12 multiplexer number 3 until this bit is set to 0. This corresponds to the E2 signal that is carrying E1 channels 9 through 12. This bit is set to 0 upon power-up.
	6	R12CS3	**Receive E12 Clock Sense Selection for Demultiplexer No. 3:** This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Receive E2 data for E12 demultiplexer number 3 is clocked in on rising edges of the clock (E12RCK3) when this bit is a 0, and on falling edges when this bit is a 1. This bit is set to 0 upon power-up.
	5	T12CS3	**Transmit E12 Clock Sense Selection for Multiplexer No. 3:** This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Transmit E2 data for E12 multiplexer number 3 is clocked out on rising edges of the clock (E12TCKO3) when this bit is a 1, and on falling edges when this bit is a 0. This bit is set to 0 upon power-up.
	4	E12AIS3	**E12 AIS Generation for E12 Multiplexer No. 3:** When set to 1, AIS is generated in the E2 G.742 format signal for E12 multiplexer number 3. AIS consists of all ones. This bit is set to 0 upon power-up.
	3	E12RA3	**E12 Remote Alarm Control for E12 Multiplexer No. 3:** When set to 1, the remote alarm bit (bit 11) in the E2 G.742 for E12 multiplexer number 3 is transmitted as a 1. When set to 0, the remote alarm bit is transmitted as a 0. This bit is set to 0 upon power-up.
	2	E12SB3	**E12 Spare Bit Control for E12 Multiplexer No. 3.** When set to 1, the spare bit (bit 12) in the E2 G.742 format for E12 multiplexer number 3 is transmitted as a 1. When set to 0, the spare bit is transmitted as a 0. This bit is set to 0 upon power-up.
	1-0	Not Used	**Not Used:** These bits power up in the zero state.

Address	Bit	Symbol	Description
5A	7	E12FE4	**Insert E2 Framing Pattern Errors for E12 Multiplexer No. 4:** A 1 causes the insertion of one framing pattern error to be sent continuously in the E2 G.742 format for E12 multiplexer number 4 until this bit is set to 0. This corresponds to the E2 signal that is carrying E1 channels 13 through 16. This bit is set to 0 upon power-up.
	6	R12CS4	**Receive E12 Clock Sense Selection for Demultiplexer No. 4:** This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Receive E2 data for E12 demultiplexer number 4 is clocked in on rising edges of the clock (E12RCK4) when this bit is a 0, and on falling edges when this bit is a 1. This bit is set to 0 upon power-up.
	5	T12CS4	**Transmit E12 Clock Sense Selection for Multiplexer No. 4:** This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Transmit E2 data for E12 multiplexer number 4 is clocked out on rising edges of the clock (E12TCKO4) when this bit is a 1, and on falling edges when this bit is a 0. This bit is set to 0 upon power-up.
	4	E12AIS4	**E12 AIS Generation for E12 Multiplexer No. 4:** When set to 1, AIS is generated in the E2 G.742 format signal for E12 multiplexer number 4. AIS consists of all ones. This bit is set to 0 upon power-up.
	3	E12RA4	**E12 Remote Alarm Control for E12 Multiplexer No. 4:** When set to 1, the remote alarm bit (bit 11) in the E2 G.742 for E12 multiplexer number 4 is transmitted as a 1. When set to 0, the remote alarm bit is transmitted as a 0. This bit is set to 0 upon power-up.
	2	E12SB4	**E12 Spare Bit Control for E12 Multiplexer No. 4.** When set to 1, the spare bit (bit 12) in the E2 G.742 format for E12 multiplexer number 4 is transmitted as a 1. When set to 0, the spare bit is transmitted as a 0. This bit is set to 0 upon power-up.
	1-0	Not Used	**Not Used:** These bits power up in the zero state.

E23 CONTROL REGISTERS

Address	Bit	Symbol	Description
A8	7-4	Not Used	**Not Used:** These bits power up in the zero state.
	3-0	E23AISm (m = 4-1)	**Receive E23 Insert AIS for Demultiplexers No. 4-1:** When any of these four bits is set to 1, E2 AIS is inserted into the corresponding E2 bit stream m. AIS is defined as all ones in the G.742 format. Bit 0 represents the insertion of E2 AIS into the receive E2 bit stream for demultiplexer number 1. The E23AISm bits are active in both the E13 skip mux mode and the E12/E23 split mux mode. These bits power up to 1 (AIS on).
B7	7	T23CS4	**Transmit E23 Clock Sense Selection for Multiplexer No. 4:** This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Transmit E2 data for multiplexer number 4 is clocked in on rising edges of the input clock (E23TCK4) when this bit is a 0, and on falling edges when this bit is a 1. This bit is set to 0 upon power-up.
	6	R23CS4	**Receive E23 Clock Sense Selection for Demultiplexer No. 4**: This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Receive E2 data from demultiplexer number 4 is clocked out on falling edges of the input clock (E23RCK4) when this bit is a 0, and on rising edges when this bit is a 1. This bit is set to 0 upon power-up.
	5	T23CS3	**Transmit E23 Clock Sense Selection for Multiplexer No. 3:** This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Transmit E2 data for multiplexer number 3 is clocked in on rising edges of the input clock (E23TCK3) when this bit is a 0, and on falling edges when this bit is a 1. This bit is set to 0 upon power-up.
	4	R23CS3	**Receive E23 Clock Sense Selection for Demultiplexer No. 3:** This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Receive E2 data from demultiplexer number 3 is clocked out on falling edges of the input clock (E23RCK3) when this bit is a 0, and on rising edges when this bit is a 1. This bit is set to 0 upon power-up.
	3	T23CS2	**Transmit E23 Clock Sense Selection for Multiplexer No. 2:** This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Transmit E2 data for multiplexer number 2 is clocked in on rising edges of the input clock (E23TCK2) when this bit is a 0, and on falling edges when this bit is a 1. This bit is set to 0 upon power-up.
	2	R23CS2	**Receive E23 Clock Sense Selection for Demultiplexer No. 2:** This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Receive E2 data from demultiplexer number 2 is clocked out on falling edges of the input clock (E23RCK2) when this bit is a 0, and on rising edges when this bit is a 1. This bit is set to 0 upon power-up.

Address	Bit	Symbol	Description
B7 (cont.)	1	T23CS1	**Transmit E23 Clock Sense Selection for Multiplexer No. 1:** This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Transmit E2 data for multiplexer number 1 is clocked in on rising edges of the input clock (E23TCK1) when this bit is a 0, and on falling edges when this bit is a 1. This bit is set to 0 upon power-up.
	0	R23CS1	**Receive E23 Clock Sense Selection for Demultiplexer No. 1:** This bit is enabled when a 0 is written to control bit E13M (bit 7 in address B9H). In this mode, the E123MUX is configured for E12 and E23 operation. Receive E2 data from demultiplexer number 1 is clocked out on falling edges of the input clock (E23RCK1) when this bit is a 0, and on rising edges when this bit is a 1. This bit is set to 0 upon power-up.

E3 CONTROL REGISTER

Address	Bit	Symbol	Description
B0	7	E3FE	**Insert E3 Framing Pattern Errors into E3 Frame:** A 1 causes the insertion of one framing pattern error into the transmitted E3 G.751 framing pattern. This bit is set to 0 upon power-up.
	6	Not Used	**Not Used:** This bit powers up in the zero state.
	5	E3NRZ	**E3 NRZ Interface Enable:** A 1 written into this bit location enables the E3 channel to be configured for NRZ receive and transmit interfaces. A 0 configures the E3 for unipolar (positive and negative rail) interfaces. This bit is set to 0 upon power-up.
	4	E3AIS	**E3 Transmit AIS Enable:** A 1 inserts AIS for the transmit E3 G.751 signal. An AIS is defined as all ones in the asynchronous data bit stream. This bit is set to 0 upon power-up.
	3	E3RA	**E3 Remote Alarm Control:** When set to 1, the remote alarm bit (bit 11) in the E3 G.751 signal is transmitted as a 1. When set to 0, the remote alarm bit is transmitted as a 0. This bit is set to 0 upon power-up.
	2	E3SB	**E3 Spare Bit Control:** When set to 1, the spare bit (bit 12) in the E3 G.751 signal is transmitted as a 1. When set to 0, the spare bit is transmitted as a 0. This bit is set to 0 upon power-up.
	1	RE3CS	**Receive E3 Clock Sense Selection:** Receive E3 data is clocked in on rising edges of the input clock (E3RCKI) when this bit is a 0, and on falling edges when this bit is a 1. This bit is set to 0 upon power-up.
	0	TE3CS	**Transmit E3 Clock Sense Selection:** Transmit E3 data is clocked out on falling edges of the input clock (E3TCKI) when this bit is a 0, and on rising edges when this bit is a 1. This bit is set to 0 upon power-up.

E12, E23 FIFO CENTERING CONTROL REGISTER

Address	Bit	Symbol	Description
B6	7-4	Not Used	**Not Used:** These bits power up in the zero state.
	3	E23MCTR	**E23MUX FIFO Centering Control Bit:** TranSwitch recommends that this bit be set to 1 for all operations (split mux or skip mux). When set to a 1, this bit enables the robust centering algorithm in the E23 mux FIFOs to compensate for temperature and voltage extremes. This bit is set to 0 on power-up or reset.
	2	E12MCTR	**E12 Mux FIFO Centering Control Bit:** TranSwitch recommends that this bit be set to 1 for all operations (split mux or skip mux). When set to a 1, this bit enables the robust centering algorithm in the E12 mux FIFOs to compensate for temperature and voltage extremes. This bit is set to 0 on power-up or reset.
	1	E23DCTR	**E23 Demux FIFO Centering Control Bit:** TranSwitch recommends that this bit be set to 1 for all operations (split mux or skip mux). When set to a 1, this bit enables the robust centering algorithm in the E23 demux FIFOs to compensate for temperature and voltage extremes. This bit is set to 0 on power-up or reset.
	0	E12DCTR	**E12 Demux FIFO Centering Control Bit:** TranSwitch recommends setting this bit to 1 for all operations (split mux or skip mux). When set to a 1, this bit enables the robust centering algorithm in the E12 demux FIFOs to compensate for temperature and voltage extremes. This bit is set to 0 on power-up or reset.

LOOPBACK CONTROL REGISTERS

Address	Bit	Symbol	Description
0C	7-0	CHnLB (n = 8-1)	**E1 Channel n Remote Loopback for Channels 8 - 1:** A 1 written to any control bit in this register causes the E1 receive data for the corresponding E1 channel n to be looped back as transmit data. AIS is inserted into the receive data stream. Bit 7 represents E1 channel 8. These bits are set to 0 upon power-up.
0D	7-0	CHnLB (n = 16-9)	**E1 Channel n Remote Loopback for Channels 16 - 9:** A 1 written to any control bit in this register causes the E1 receive data for the corresponding E1 channel n to be looped back as transmit data. AIS is inserted into the receive data stream. Bit 7 represents E1 channel 16. These bits are set to 0 upon power-up.
0E	7-4	E12LLm (m = 4-1)	**E12 Local Loopback for Multiplexer/Demultiplexers 4 - 1:** A 1 written to any of these four control bits causes the E2 transmit data of the corresponding multiplexer/demultiplexer m to be looped back as receive data. AIS is inserted into the upstream transmit data stream. The E2 receive data stream is terminated. The E12LLm bits are active in both the E13 skip mux mode and E12/E23 split mux mode. Bit 7 represents E12 multiplexer/demultiplexer number 4. These bits are set to 0 upon power-up.

Address	Bit	Symbol	Description
0E (cont.)	3-0	E12RLm (m = 4-1)	**E12 Remote Loopback for Multiplexer/Demultiplexers 4 - 1:** The E12 remote loopback occurs at the E2 inputs/outputs of the E12 mux block (see Figure 1). When a one is written to any of these control bits, it causes the E2 receive clock and data to be looped back as the E2 transmit clock and data for the specific channel. The E1 channels corresponding to the E12 section in loopback are terminated and AIS is inserted into the downstream E1 receive channels. Bit 3 represents E12 multiplexer/ demultiplexer number 4. Note: The E12RLm bits are active in both E12 split mux and E13 skip mux modes. These bits are set to 0 upon power-up.
0F	7-4	Not Used	**Not Used:** These bits power up in the zero state.
	3-0	E23RLm (m = 4-1)	**E23 Remote Loopback for E2 Channels 4 - 1:** The E23 remote loopback occurs at the E2 inputs/outputs of the E23 mux block (see Figure 1). When a one is written to any of these control bits, it causes the demultiplexed E2 receive clock and data to be looped back as the E2 transmit clock and data for the specific channel. This E2 transmit clock and data is multiplexed up to the E3 level. The E2 channels in loopback are terminated and AIS is inserted into the downstream E2 receive channels. Bit 3 represents E2 channel number 4. Note: The E23RLm bits are active in both E13 skip mux and E23 split mux modes. These bits are set to 0 upon power-up.
10	7-2	Not Used	**Not Used:** These bits power up in the zero state.
	1	E3RLB	**E3 Remote Loopback:** A 1 written to this control bit causes the E3 receive data and clock signals to be looped back as E3 transmit data and clock. AIS is inserted into the downstream E3 receive demultiplexer. The E3 transmit multiplexer output is terminated. This bit is set to 0 upon power-up.
	0	E3LLB	**E3 Local Loopback:** A 1 written to this control bit causes the E3 transmit data to be looped back as E3 receive data. AIS is inserted into the E3 transmit data stream. The E3 receive data stream is terminated. This bit is set to 0 upon power-up.

E2 AND E3 BIT ERROR THRESHOLD REGISTERS

Address	Bit	Symbol	Description
11	7-0	Set E2 BER Threshold	**Threshold Register for E2 Receive Bit Error Rate Measurement:** This register is reset to a value of 63H when the reset is applied. This value represents a BER of 10^{-3}. This BER is valid for all four E12 receive demultiplexers.
12	7-0	Set E3 BER Threshold	**Threshold Register for E3 Receive Bit Error Rate Measurement:** This register is reset to a value of DFH when the reset is applied. This value represents a BER of 10^{-3}.

INTERRUPT INDICATION REGISTER

All interrupt indications are cleared to zero when written with a 1 by the microprocessor. An interrupt indication is latched to 1 by a transition (to 0 or 1) of any corresponding unlatched alarm bit when it is not masked. These bits are set to 0 upon power-up.

Address	Bit	Symbol	Description
07	7	INT	**Software Interrupt Indication:** A 1 indicates that an interrupt indication has been set to 1 in one or more of bits 6 - 0 of this register.
	6	E3	**E3 Interrupt Indication:** A 1 indicates that an E3 alarm has been detected. The corresponding interrupt mask bit for the associated E3 alarm must be set to 0 for this indication to occur.
	5	E2CH4	**E2 Interrupt Indication for E12 Demultiplexer No. 4:** A 1 indicates that an E2 alarm for demultiplexer number 4 has been detected. The corresponding interrupt mask bit for the E2 alarm must be set to 0 for this indication to occur.
	4	E2CH3	**E2 Interrupt Indication for E12 Demultiplexer No. 3:** A 1 indicates that an E2 alarm for demultiplexer number 3 has been detected. The corresponding interrupt mask bit for the E2 alarm must be set to 0 for this indication to occur.
	3	E2CH2	**E2 Interrupt Indication for E12 Demultiplexer No. 2:** A 1 indicates that an E2 alarm for demultiplexer number 2 has been detected. The corresponding interrupt mask bit for the E2 alarm must be set to 0 for this indication to occur.
	2	E2CH1	**E2 Interrupt Indication for E12 Demultiplexer No. 1:** A 1 indicates that an E2 alarm for demultiplexer number 1 has been detected. The corresponding interrupt mask bit for the E2 alarm must be set to 0 for this indication to occur.
	1	E1LOS 9-16	**E1 Interrupt Indication for E1 Channels 9 - 16:** A 1 indicates that an E1 loss of signal alarm for any of the channels 9 to 16 has been detected. The corresponding interrupt mask bit for the E1 alarm must be set to 0 for this indication to occur.
	0	E1LOS 1-8	**E1 Interrupt Indication for E1 Channels 1 - 8:** A 1 indicates that an E1 loss of signal alarm for any of the channels 1 to 8 has been detected. The corresponding interrupt mask bit for the E1 alarm must be set to 0 for this indication to occur.

INTERRUPT MASK BITS REGISTERS

Address	Bit	Symbol	Description
21	7-4	Not Used	**Not Used:** These bits power up in the zero state.
	3-0	CnLSM (n = 4-1)	**E1 Channels 4 - 1 Loss Of Signal Mask Bits:** A 1 disables the generation of the software interrupt and hardware interrupt indications when a loss of signal alarm occurs for E1 channel n. Bit 3 represents channel 4. These bits power up in the zero state.

Address	Bit	Symbol	Description
31	7-4	Not Used	**Not Used:** These bits power up in the zero state.
	3-0	CnLSM (n = 8-5)	**E1 Channels 8 - 5 Loss Of Signal Mask Bits:** A 1 disables the generation of the software interrupt and hardware interrupt indications when a loss of signal alarm occurs for E1 channel n. Bit 3 represents channel 8. These bits power up in the zero state.
41	7-4	Not Used	**Not Used:** These bits power up in the zero state.
	3-0	CnLSM (n = 12-9)	**E1 Channels 12 - 9 Loss Of Signal Mask Bits:** A 1 disables the generation of the software interrupt and hardware interrupt indications when a loss of signal alarm occurs for E1 channel n. Bit 3 represents channel 12. These bits power up in the zero state.
51	7-4	Not Used	**Not Used:** These bits power up in the zero state.
	3-0	CnLSM (n = 16-13)	**E1 Channels 16 - 13 Loss Of Signal Mask Bits:** A 1 disables the generation of the software interrupt and hardware interrupt indications when a loss of signal alarm occurs for E1 channel n. Bit 3 represents channel 16. These bits power up in the zero state.
66	7-6	Not Used	**Not Used:** These bits power up in the zero state.
	5	E2SM1	**E2 Spare Bit Mask Bit for E2 Demultiplexer No. 1:** A 1 disables the generation of the software interrupt and hardware interrupt indications when the E2 spare bit in the G.742 format is equal to 1 for E2 demultiplexer number 1. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	4	E2RM1	**E2 Remote Alarm Mask Bit for E2 Demultiplexer No. 1:** A 1 disables the generation of the software interrupt and hardware interrupt indications when the E2 remote alarm bit in the G.742 format is equal to 1 for E2 demultiplexer number 1. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	3	E2BM1	**E2 BER Mask Bit for E2 Demultiplexer No. 1:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E2 BER alarm bit is detected for E2 demultiplexer number 1. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	2	E2LFM1	**E2 Loss Of Frame Mask Bit for E2 Demultiplexer No. 1:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E2 loss of frame alarm is detected for E2 demultiplexer number 1. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	1	E2AM1	**E2 AIS Mask Bit for E2 Demultiplexer No. 1:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E2 AIS alarm is detected for E2 demultiplexer number 1. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	0	Not Used	**Not Used:** This bit powers up in the zero state.

Address	Bit	Symbol	Description
76	7-6	Not Used	**Not Used:** These bits power up in the zero state.
	5	E2SM2	**E2 Spare Bit Mask Bit for E2 Demultiplexer No. 2:** A 1 disables the generation of the software interrupt and hardware interrupt indications when the E2 spare bit in the G.742 format is equal to 1 for E2 demultiplexer number 2. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	4	E2RM2	**E2 Remote Alarm Mask Bit for E2 Demultiplexer No. 2:** A 1 disables the generation of the software interrupt and hardware interrupt indications when the E2 remote alarm bit in the G.742 format is equal to 1 for E2 demultiplexer number 2. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	3	E2BM2	**E2 BER Mask Bit for E2 Demultiplexer No. 2:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E2 BER alarm bit is detected for E2 demultiplexer number 2. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	2	E2LFM2	**E2 Loss Of Frame Mask Bit for E2 Demultiplexer No. 2:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E2 loss of frame alarm is detected for E2 demultiplexer number 2. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	1	E2AM2	**E2 AIS Mask Bit for E2 Demultiplexer No. 2:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E2 AIS alarm is detected for E2 demultiplexer number 2. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	0	Not Used	**Not Used:** This bit powers up in the zero state.

Address	Bit	Symbol	Description
86	7-6	Not Used	**Not Used:** These bits power up in the zero state.
	5	E2SM3	**E2 Spare Bit Mask Bit for E2 Demultiplexer No. 3:** A 1 disables the generation of the software interrupt and hardware interrupt indications when the E2 spare bit in the G.742 format is equal to 1 for E2 demultiplexer number 3. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	4	E2RM3	**E2 Remote Alarm Mask Bit for E2 Demultiplexer No. 3:** A 1 disables the generation of the software interrupt and hardware interrupt indications when the E2 remote alarm bit in the G.742 format is equal to 1 for E2 demultiplexer number 3. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	3	E2BM3	**E2 BER Mask Bit for E2 Demultiplexer No. 3:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E2 BER alarm bit is detected for E2 demultiplexer number 3. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	2	E2LFM3	**E2 Loss Of Frame Mask Bit for E2 Demultiplexer No. 3:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E2 loss of frame alarm is detected for E2 demultiplexer number 3. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	1	E2AM3	**E2 AIS Mask Bit for E2 Demultiplexer No. 3:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E2 AIS alarm is detected for E2 demultiplexer number 3. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	0	Not Used	**Not Used:** This bit powers up in the zero state.

Address	Bit	Symbol	Description
96	7-6	Not Used	**Not Used:** These bits power up in the zero state.
	5	E2SM4	**E2 Spare Bit Mask Bit for E2 Demultiplexer No. 4:** A 1 disables the generation of the software interrupt and hardware interrupt indications when the E2 spare bit in the G.742 format is equal to 1 for E2 demultiplexer number 4. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	4	E2RM4	**E2 Remote Alarm Mask Bit for E2 Demultiplexer No. 4:** A 1 disables the generation of the software interrupt and hardware interrupt indications when the E2 remote alarm bit in the G.742 format is equal to 1 for E2 demultiplexer number 4. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	3	E2BM4	**E2 BER Mask Bit for E2 Demultiplexer No. 4:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E2 BER alarm bit is detected for E2 demultiplexer number 4. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	2	E2LFM4	**E2 Loss Of Frame Mask Bit for E2 Demultiplexer No. 4:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E2 loss of frame alarm is detected for E2 demultiplexer number 4. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	1	E2AM4	**E2 AIS Mask Bit for E2 Demultiplexer No. 4:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E2 AIS alarm is detected for E2 demultiplexer number 4. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	0	Not Used	**Not Used:** This bit powers up in the zero state.

Address	Bit	Symbol	Description
A6	7-6	Note Used	**Not Used:** These bits power up in the zero state.
	5	E3SPBM	**E3 Spare Bit Mask:** A 1 disables the generation of the software interrupt and hardware interrupt indications when the spare bit (bit 12) in the E3 G.751 frame has been received as a 1. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	4	E3REMM	**E3 Remote Alarm Bit Mask:** A 1 disables the generation of the software interrupt and hardware interrupt indications when the remote alarm bit (bit 11) in the E3 G.751 frame has been received as a 1. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	3	E3BERM	**E3 Bit Error Rate Alarm Bit Mask:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E3 BER alarm bit is detected. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	2	E3LOFM	**E3 Loss Of Frame Alarm Bit Mask:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E3 LOF alarm bit is detected. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	1	E3AISM	**E3 AIS Alarm Bit Mask:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E3 AIS alarm bit is detected. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.
	0	E3LOSM	**E3 Loss Of Signal Alarm Bit Mask:** A 1 disables the generation of the software interrupt and hardware interrupt indications when an E3 LOS alarm bit is detected. A 0 enables the software interrupt indication and hardware interrupt. This bit powers up in the zero state.

ALARM REGISTERS

The following descriptions pertain to the status registers within the E123MUX. There are two readable bit positions per alarm. One bit position indicates the detected alarm as unlatched and reflects the current status of the alarm. The second bit provides the alarm status as a latched indication. A latched bit position is set to 1 on a 0 to 1 transition of the alarm and remains set until it is cleared to 0 during a microprocessor write cycle of its register (writing 1 to a bit clears it to 0, writing 0 to a bit leaves it unchanged). All of these bits are set to the zero state upon power-up.

Address	Bit	Symbol	Description
20	7-4	Not Used	**Not Used:** These read-only bits are indeterminate values.
	3-0	CnLOS (n = 4-1)	**Loss Of Signal Indications for E1 Channels 4 - 1:** A 1 indicates that an E1 loss of signal has been detected for channel n when it is configured for a dual unipolar interface. Loss of signal is detected when there are no transitions in a window of 128 clock periods. Recovery occurs when at least one transition is detected in a window of 8 clock periods for 16 consecutive periods. Bit 3 corresponds to a loss of signal for E1 channel 4. When the NRZ mode is selected, an external loss of indication may be provided as an input on the negative rail input lead. Either loss of signal will result in a CnLOS alarm indication, and an interrupt if the mask bit is set to 0 for channel n. When an E1 loss of signal is declared, an AIS is automatically inserted into the corresponding E1 transmit data stream.
2B	7-4	Not Used	**Not Used:** These read-only bits are indeterminate values.
	3-0	CnLOS (n = 4-1)	**Latched Loss Of Signal Indications for E1 Channels 4 - 1:** These are the same alarms as those in the corresponding bit positions of address 20H, except that these are latched and are reset to 0 when the register bit position is written with a 1.
30	7-4	Not Used	**Not Used:** These read-only bits are indeterminate values.
	3-0	CnLOS (n = 8-5)	**Loss Of Signal Indications for E1 Channels 8 - 5:** A 1 indicates that an E1 loss of signal has been detected for channel n when it is configured for a dual unipolar interface. Loss of signal is detected when there are no transitions in a window of 128 clock periods. Recovery occurs when at least one transition is detected in a window of 8 clock periods for 16 consecutive periods. Bit 3 corresponds to a loss of signal for E1 channel 8. When the NRZ mode is selected, an external loss of indication may be provided as an input on the negative rail input lead. Either loss of signal will result in a CnLOS alarm indication, and an interrupt if the mask bit is set to 0 for channel n. When an E1 loss of signal is declared, an AIS is automatically inserted into the corresponding E1 transmit data stream.
3B	7-4	Not Used	**Not Used:** These read-only bits are indeterminate values.
	3-0	CnLOS (n = 8-5)	**Latched Loss Of Signal Indications for E1 Channels 8 - 5:** These are the same alarms as those in the corresponding bit positions of address 30H, except that these are latched and are reset to 0 when the register bit position is written with a 1.

Address	Bit	Symbol	Description
40	7-4	Not Used	**Not Used:** These read-only bits are indeterminate values.
	3-0	CnLOS (n = 12-9)	**Loss Of Signal Indications for E1 Channels 12 - 9:** A 1 indicates that an E1 loss of signal has been detected for channel n when it is configured for a dual unipolar interface. Loss of signal is detected when there are no transitions in a window of 128 clock periods. Recovery occurs when at least one transition is detected in a window of 8 clock periods for 16 consecutive periods. Bit 3 corresponds to a loss of signal for E1 channel 12. When the NRZ mode is selected, an external loss of indication may be provided as an input on the negative rail input lead. Either loss of signal will result in a CnLOS alarm indication, and an interrupt if the mask bit is set to 0 for channel n. When an E1 loss of signal is declared, an AIS is automatically inserted into the corresponding E1 transmit data stream.
4B	7-4	Not Used	**Not Used:** These read-only bits are indeterminate values.
	3-0	CnLOS (n = 12-9)	**Latched Loss Of Signal Indications for E1 Channels 12 - 9:** These are the same alarms as those in the corresponding bit positions of address 40H, except that these are latched and are reset to 0 when the register bit position is written with a 1.
50	7-4	Not Used	**Not Used:** These read-only bits are indeterminate values.
	3-0	CnLOS (n = 16-13)	**Loss Of Signal Indications for E1 Channels 16 - 13:** A 1 indicates that an E1 loss of signal has been detected for channel n when it is configured for a dual unipolar interface. Loss of signal is detected when there are no transitions in a window of 128 clock periods. Recovery occurs when at least one transition is detected in a window of 8 clock periods for 16 consecutive periods. Bit 3 corresponds to a loss of signal for E1 channel 16. When the NRZ mode is selected, an external loss of indication may be provided as an input on the negative rail input lead. Either loss of signal will result in a CnLOS alarm indication, and an interrupt if the mask bit is set to 0 for channel n. When an E1 loss of signal is declared, an AIS is automatically inserted into the corresponding E1 transmit data stream.
5B	7-4	Not Used	**Not Used:** These read-only bits are indeterminate values.
	3-0	CnLOS (n = 16-13)	**Latched Loss Of Signal Indications for E1 Channels 16 - 13:** These are the same alarms as those in the corresponding bit positions of address 50H, except that these are latched and are reset to 0 when the register bit position is written with a 1.
65	7-6	Not Used	**Not Used:** These read-only bits are indeterminate values.
	5	E2SPB1	**Spare Bit Indication for E12 Mux/Demux No. 1:** A 1 indicates that the spare bit (bit 12) in the E2 G.742 frame has been received as a 1 for E12 multiplexer/demultiplexer number 1. The detection and recovery times are immediate.
	4	E2RA1	**Remote Alarm Indication Received in E12 Mux/Demux No. 1:** A 1 indicates that the remote alarm bit (bit 11) in the E2 G.742 frame has been received as a 1 for E12 mux/demux number 1. The detection and recovery times are immediate.

Address	Bit	Symbol	Description
65 (cont.)	3	E2BER1	**Bit Error Rate Indication for E12 Mux/Demux No. 1:** A 1 indicates that more than one error in 1000 bits has been detected using the E2 G.742 framing pattern for E12 mux/demux number 1. The calculation is made by counting the number of frames received with framing pattern errors in one second compared to the total number of frames received in this period.
	2	E2LOF1	**Loss Of Frame Indication for E12 Mux/Demux No.1:** A 1 indicates that loss of frame has been detected for E12 mux/demux number 1. A loss of frame alignment occurs when four consecutive framing patterns are received in error. Recovery occurs when three consecutive error-free framing patterns are received. See Note 1.
	1	E2AIS1	**Receive AIS Indication for E12 Mux/Demux No.1:** A 1 indicates that an AIS has been detected for E12 mux/demux number 1. An E2 AIS alarm is generated when 4 or fewer zeros are detected in each of two consecutively received E2 frames. Recovery occurs when 5 or more zeros are detected in two consecutive E2 frames. See Note 1.
	0	Not Used	**Not Used:** This read-only bit is an indeterminate value.
67	7-6	Not Used	**Not Used:** These read-only bits are indeterminate values.
	5-1	Latched E2 Channel Alarms (#1)	**Latched Indications for E12 Mux/Demux No. 1:** These are the same alarms as those in the corresponding bit positions of address 65H, except that these are latched and are reset to 0 when the register bit position is written with a 1.
	0	Not Used	**Not Used:** This read-only bit is an indeterminate value.
75	7-6	Not Used	**Not Used:** These read-only bits are indeterminate values.
	5	E2SPB2	**Spare Bit Indication for E12 Mux/Demux No. 2:** A 1 indicates that the spare bit (bit 12) in the E2 G.742 frame has been received as a 1 for E12 multiplexer/demultiplexer number 2. The detection and recovery times are immediate.
	4	E2RA2	**Remote Alarm Indication Received in E12 Mux/Demux No. 2:** A 1 indicates that the remote alarm bit (bit 11) in the E2 G.742 frame has been received as a 1 for E12 mux/demux number 2. The detection and recovery times are immediate.
	3	E2BER2	**Bit Error Rate Indication for E12 Mux/Demux No. 2:** A 1 indicates that more than one error in 1000 bits has been detected using the E2 G.742 framing pattern for E12 mux/demux number 2. The calculation is made by counting the number of frames received with framing pattern errors in one second compared to the total number of frames received in this period.
	2	E2LOF2	**Loss Of Frame Indication for E12 Mux/Demux No.2:** A 1 indicates that loss of frame has been detected for E12 mux/demux number 2. A loss of frame alignment occurs when four consecutive framing patterns are received in error. Recovery occurs when three consecutive error-free framing patterns are received. See Note 1.

Note 1: AIS is inserted into all downstream tributaries when this alarm is active.

Address	Bit	Symbol	Description
75 (cont.)	1	E2AIS2	**Receive AIS Indication for E12 Mux/Demux No.2:** A 1 indicates that an AIS has been detected for E12 mux/demux number 2. An E2 AIS alarm is generated when 4 or fewer zeros are detected in each of two consecutively received E2 frames. Recovery occurs when 5 or more zeros are detected in two consecutive E2 frames. See Note 1.
	0	Not Used	**Not Used:** This read-only bit is an indeterminate value.
77	7-6	Not Used	**Not Used:** These read-only bits are indeterminate values.
	5-1	Latched E2 Channel Alarms (#2)	**Latched Indications for E12 Mux/Demux No. 2:** These are the same alarms as those in the corresponding bit positions of address 75H, except that these are latched and are reset to 0 when the register bit position is written with a 1.
	0	Not Used	**Not Used:** This read-only bit is an indeterminate value.
85	7-6	Not Used	**Not Used:** These read-only bits are indeterminate values.
	5	E2SPB3	**Spare Bit Indication for E12 Mux/Demux No. 3:** A 1 indicates that the spare bit (bit 12) in the E2 G.742 frame has been received as a 1 for E12 multiplexer/demultiplexer number 3. The detection and recovery times are immediate.
	4	E2RA3	**Remote Alarm Indication Received in E12 Mux/Demux No. 3:** A 1 indicates that the remote alarm bit (bit 11) in the E2 G.742 frame has been received as a 1 for E12 mux/demux number 3. The detection and recovery times are immediate.
	3	E2BER3	**Bit Error Rate Indication for E12 Mux/Demux No. 3:** A 1 indicates that more than one error in 1000 bits has been detected using the E2 G.742 framing pattern for E12 mux/demux number 3. The calculation is made by counting the number of frames received with framing pattern errors in one second compared to the total number of frames received in this period.
	2	E2LOF3	**Loss Of Frame Indication for E12 Mux/Demux No.3:** A 1 indicates that loss of frame has been detected for E12 mux/demux number 3. A loss of frame alignment occurs when four consecutive framing patterns are received in error. Recovery occurs when three consecutive error-free framing patterns are received. See Note 1.
	1	E2AIS3	**Receive AIS Indication for E12 Mux/Demux No.3:** A 1 indicates that an AIS has been detected for E12 mux/demux number 3. An E2 AIS alarm is generated when 4 or fewer zeros are detected in each of two consecutively received E2 frames. Recovery occurs when 5 or more zeros are detected in two consecutive E2 frames. See Note 1.
	0	Not Used	**Not Used:** This read-only bit is an indeterminate value.
87	7-6	Not Used	**Not Used:** These read-only bits are indeterminate values.
	5-1	Latched E2 Channel Alarms (#3)	**Latched Indications for E12 Mux/Demux No. 3:** These are the same alarms as those in the corresponding bit positions of address 85H, except that these are latched and are reset to 0 when the register bit position is written with a 1.
	0	Not Used	**Not Used:** This read-only bit is an indeterminate value.

Note 1: AIS is inserted into all downstream tributaries when this alarm is active.

Address	Bit	Symbol	Description
95	7-6	Not Used	**Not Used:** These read-only bits are indeterminate values.
	5	E2SPB4	**Spare Bit Indication for E12 Mux/Demux No. 4:** A 1 indicates that the spare bit (bit 12) in the E2 G.742 frame has been received as a 1 for E12 multiplexer/demultiplexer number 4. The detection and recovery times are immediate.
	4	E2RA4	**Remote Alarm Indication Received in E12 Mux/Demux No. 4:** A 1 indicates that the remote alarm bit (bit 11) in the E2 G.742 frame has been received as a 1 for E12 mux/demux number 4. The detection and recovery times are immediate.
	3	E2BER4	**Bit Error Rate Indication for E12 Mux/Demux No. 4:** A 1 indicates that more than one error in 1000 bits has been detected using the E2 G.742 framing pattern for E12 mux/demux number 4. The calculation is made by counting the number of frames received with framing pattern errors in one second compared to the total number of frames received in this period.
	2	E2LOF4	**Loss Of Frame Indication for E12 Mux/Demux No.4:** A 1 indicates that loss of frame has been detected for E12 mux/demux number 4. A loss of frame alignment occurs when four consecutive framing patterns are received in error. Recovery occurs when three consecutive error-free framing patterns are received. See Note 1.
	1	E2AIS4	**Receive AIS Indication for E12 Mux/Demux No.4:** A 1 indicates that an AIS has been detected for E12 mux/demux number 4. An E2 AIS alarm is generated when 4 or fewer zeros are detected in each of two consecutively received E2 frames. Recovery occurs when 5 or more zeros are detected in two consecutive E2 frames. See Note 1.
	0	Not Used	**Not Used:** This read-only bit is an indeterminate value.
97	7-6	Not Used	**Not Used:** These read-only bits are indeterminate values.
	5-1	Latched E2 Channel Alarms (#4)	**Latched Indications for E12 Mux/Demux No. 4:** These are the same alarms as those in the corresponding bit positions of address 95H, except that these are latched and are reset to 0 when the register bit position is written with a 1.
	0	Not Used	**Not Used:** This read-only bit is an indeterminate value.
A5	7-6	Not Used	**Not Used:** These read-only bits are indeterminate values.
	5	E3SPB	**Spare Bit Indication in E3 Signal:** A 1 indicates that the spare bit (bit 12) in the E3 G.751 frame has been received as a 1. The detection and recovery times are immediate.
	4	E3RA	**Remote Alarm Indication Received in E3 Signal:** A 1 indicates that the remote alarm bit (bit 11) in the E3 G.751 frame has been received as a 1. The detection and recovery times are immediate.

Note 1: AIS is inserted into all downstream tributaries when this alarm is active.

Address	Bit	Symbol	Description
A5 (cont.)	3	E3BER	**Bit Error Rate Indication for E3 Signal:** A 1 indicates that more than one error has been detected in 1000 bits using the E3 G.751 framing pattern. The calculation is made by counting the number of frames received with framing pattern errors in one second compared to the total number of frames received in this period. Note: This bit can be active during an E3 loss of frame condition. It should be disregarded in this instance.
	2	E3LOF	**Loss Of Frame Indication for E3 Signal:** A 1 indicates that loss of frame alignment has been detected in the E3 G.751 signal. A loss of frame alignment occurs when four consecutive framing patterns are received in error. Recovery occurs when three consecutive error-free framing patterns are received. AIS will be inserted into all downstream tributaries when E3LOF alarm is declared.
	1	E3AIS	**Receive AIS Indication for E3 Signal:** A 1 indicates that an AIS has been detected in the E3 signal. An E3 AIS alarm is generated when 4 or fewer zeros are detected in each of two consecutively received E3 frames. Recovery occurs when 5 or more zeros are detected in two consecutive E3 frames. AIS will be inserted into all downstream tributaries when E3AIS alarm is declared.
	0	E3LOS	**Receive E3 Loss Of Signal Indication:** A 1 indicates that an E3 loss of signal has been detected when the interface is configured for a dual unipolar interface. Loss of signal is detected when there are no transitions in a window of 128 clock periods. Recovery occurs when at least one transition is detected in a window of 8 clock periods for 16 consecutive periods. When the NRZ mode is selected, an external loss of signal indication may be provided as an input, using the negative rail input lead. Either loss of signal indication will result in an E3LOS alarm indication and an interrupt if the mask bit is set to 0. AIS will be inserted into all downstream tributaries when E3LOS alarm is declared.
A7	7-6	Not Used	**Not Used:** These read-only bits are indeterminate values.
	5-0	Latched E3 Channel Alarms	**Latched Indications for E3 Interface:** These are the same alarms as those in the corresponding bit positions of address A5H, except that these are latched and are reset to 0 when the register bit position is written with a 1.

COUNTER DESCRIPTIONS

All counters power up in the zero state. The low order byte of each 16-bit counter should be read first, followed by the low order byte.

Address	Bit	Symbol	Description
06	7-0	PRBS Error Counter	**Pseudo Random Binary Sequence Error Counter:** An 8-bit counter that counts the number of bit errors for the E1 receive channel selected by control bits RSEL3-RSEL0 when the 2^{15}-1 PRBS Analyzer is enabled by control bit ANLEN. This is a saturating counter that is cleared on a microprocessor read cycle.
22 24 26 28 32 34 36 38 42 44 46 48 52 54 56 58	7-0	Channel n BPV Counter Low Order Byte (n = 1-16)	**E1 Channels 1 - 16 BPV Counters Low Order Byte.** These are the low order bytes associated with the 16-bit Bipolar Violation counters for each of the sixteen E1 channels. The low order byte must be read first followed by reading the high order byte. Each counter is cleared when its high order byte is read. Address 22 is the low order byte for channel 1. These counters saturate at FFFF(H).
23 25 27 29 33 35 37 39 43 45 47 49 53 55 57 59	7-0	Channel n BPV Counter High Order Byte (n = 1-16)	**E1 Channels 1 - 16 BPV Counters High Order Byte:** These are the high order bytes associated with the 16-bit Bipolar Violation counters for each of the sixteen E1 channels. The low order byte must be read first followed by reading the high order byte. Each counter is cleared when its high order byte is read. Address 23 is the high order byte for channel 1. These counters saturate at FFFF(H).
63 73 83 93	7-0	E12 Frame Error Counters	**E12 Frame Error Counters 1 - 4:** These are 8-bit counters which count the number of framing errors for the four E12 receive interfaces. Address 63 is the counter for E12 mux/demux number 1. This is a saturating counter that is cleared on a microprocessor read cycle.
64 74 84 94	7-0	E12 LOF Error Counters	**E12 Loss Of Frame Error Counters 1 - 4:** These are 8-bit counters which count the number of Loss Of Frame occurrences for the four E12 receive interfaces. Address 64 is the counter for E12 mux/demux number 1. This is a saturating counter that is cleared on a microprocessor read cycle.
6B 7B 8B 9B	7-0	E12 Frame Counter Low Order Byte	**E12 BER Measurement Frame Counters Low Order Byte:** These are the low order bytes associated with the 16-bit frame counters for each of the four E2 channels for BER measurement test purposes. The low order byte must be read first followed by the high order byte. Address 6B is the low order byte for E12 mux/demux number 1. Each counter is cleared when the 16-bit value reaches 26EAH. See Note 1.
6C 7C 8C 9C	7-0	E12 Frame Counter High Byte	**E12 BER Measurement Frame Counters High Order Byte:** These are the high bytes associated with the 16-bit frame counters for each of the four E2 channels for BER measurement test purposes. The low order byte must be read first followed by the high order byte. Address 6C is the high order byte for E12 mux/demux number 1. Each counter is cleared when the 16-bit value reaches 26EAH. See Note 1.

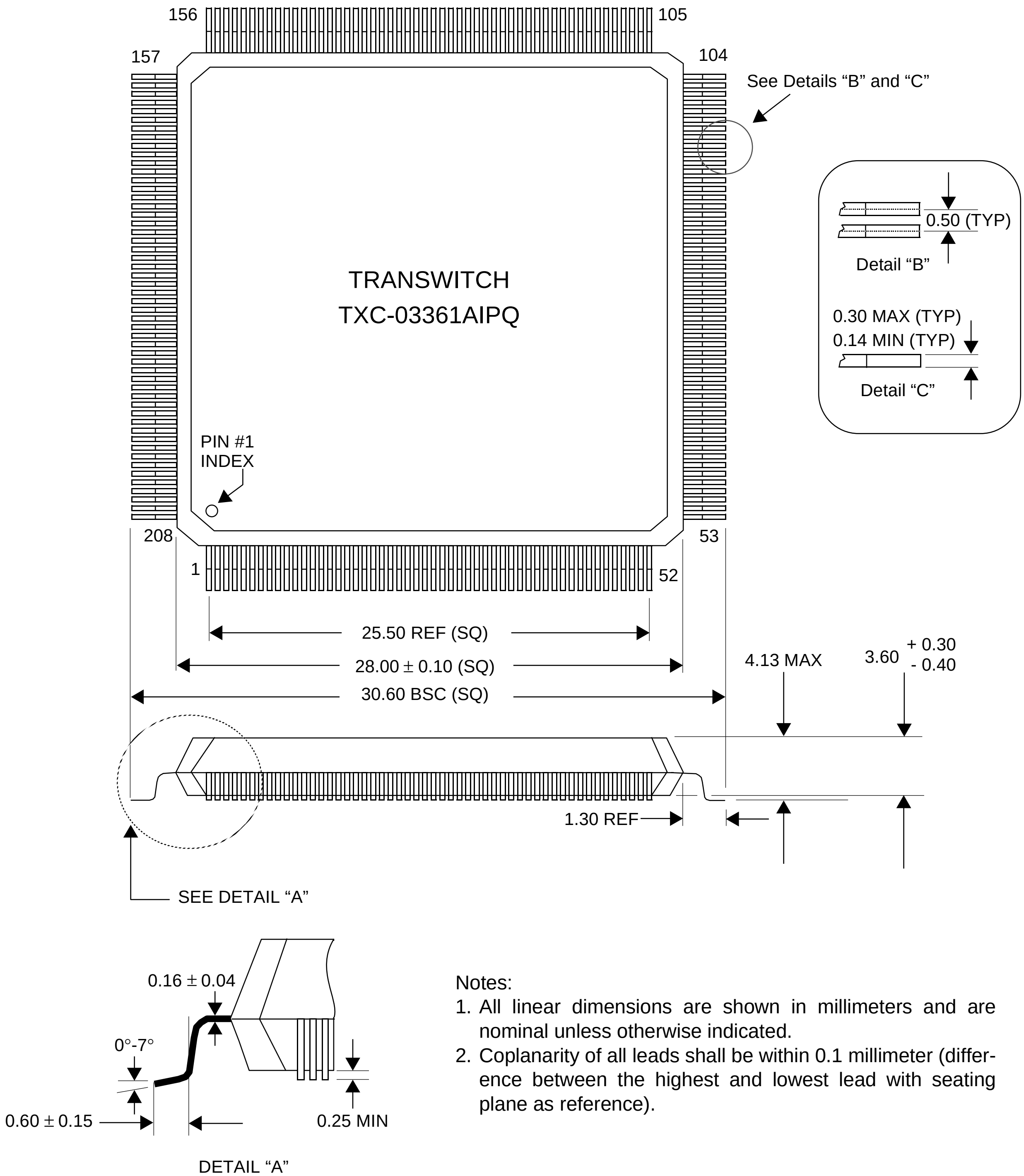
Note 1: This counter is not cleared on a microprocessor read cycle.

Address	Bit	Symbol	Description
6D 7D 8D 9D	7-0	E12 Errored Frame Counters	**E12 BER Measurement Errored Frame Counters:** These are 8-bit counters which count the number of framing patterns that are in error for the four E12 receive interfaces for BER measurement test purposes. Address 6D is the counter for E12 mux/demux number 1. This counter is cleared when the corresponding 16-bit frame counter (addresses 6B and 6C for E12 mux/demux number 1) reaches a count of 26EAH. See Note 1.
A1	7-0	E3 BPV Counter Low Order Byte	**E3 Channel BPV Counter Low Order Byte:** This is the low order byte associated with the 16-bit Bipolar Violation counter for E3 input. The low order byte must be read first followed by the high order byte. The counter rolls over to zero from its maximum count and is cleared when its high order byte is read.
A2	7-0	E3 BPV Counter High Order Byte	**E3 Channel BPV Counter High Order Byte:** This is the high order byte associated with the 16-bit Bipolar Violation counter for E3 input. The low order byte must be read first followed by the high order byte. The counter rolls over to zero from its maximum count and is cleared when its high order byte is read.
A3	7-0	E3 Frame Error Counter	**E3 Receive Frame Error Counter:** This is an 8-bit counter which counts the number of framing errors in the E3 G.751 format. This is a saturating counter that is cleared on a microprocessor read cycle.
A4	7-0	E3 Loss Of Frame Counter	**E3 Receive Loss Of Frame Counter:** This is an 8-bit counter which counts the number of Loss Of Frame occurrences in the E3 G.751 format. This is a saturating counter that is cleared on a microprocessor read cycle.
AA	7-0	E3 Frame Counter Low Order Byte	**E3 BER Measurement Frame Counter Low Order Byte:** This is the low order byte associated with the 16-bit frame counter for the E3 channel for BER measurement test purposes. The low order byte must be read first followed by the high order byte. This counter is cleared when the 16-bit value in the counter reaches 5767H. See Note 1.
AB	7-0	E3 Frame Counter High Byte	**E3 BER Measurement Frame Counter High Order Byte:** This is the high order byte associated with the 16-bit frame counter for the E3 channel for BER measurement test purposes. The low order byte must be read first followed by the high order byte. This counter is cleared when the 16-bit value in the counter reaches 5767H. See Note 1.
AC	7-0	E3 Errored Frame Counter	**E3 BER Measurement Errored Frame Counter:** This is an 8-bit counter which counts the number of framing patterns that are in error for BER measurement test purposes. This counter is cleared when the 16-bit frame counter (addresses AA and AB) reaches the value of 5767H. See Note 1.

Note 1: This counter is not cleared on a microprocessor read cycle.

PACKAGE INFORMATION

The E123MUX device is available in a 208-pin plastic quad flat package (PQFP) suitable for surface mounting, as shown in Figure 21.



Notes:

1. All linear dimensions are shown in millimeters and are nominal unless otherwise indicated.
2. Coplanarity of all leads shall be within 0.1 millimeter (difference between the highest and lowest lead with seating plane as reference).

Figure 21. E123MUX TXC-03361 208-Pin Plastic Quad Flat Package

ORDERING INFORMATION

Part Number: TXC-03361AIPQ 208-pin Plastic Quad Flat Package (PQFP)

RELATED PRODUCTS

TXC-02050, MRT Multi-Rate Line Interface device. The MRT directly interfaces with the E123MUX device and provides the functions for terminating ITU-T-specified 8448 kbit/s (E2) and 34368 kbit/s (E3) line rate signals, or 6312 kbit/s (JT2) line signals specified in the Japanese NTT Technical Reference for High Speed Digital Leased Circuits. An optional HDB3 codec is provided for the two ITU-T line rates.

TXC-03104, QE1F VLSI Device (Quad E1 Framer). Handles all logical interfacing functionality to an E1 line, including slip buffers and termination of the E1 Facility Data Link. A 4-channel E1 Framer, the QE1F provides direct microprocessor access for all control functions. This product is not recommended for use in new designs (use QE1F-*Plus* or E1Fx8).

TXC-03109, E1Fx8 VLSI Device (8-Channel E1 Framer). An 8-channel framer for voice and data communications applications. This device handles all logical interfacing functionality to a T1 line and operates from a power supply of 3.3 volts.

TXC-03114, QE1F-*Plus* VLSI Device (Quad E1 Framer-*Plus*). The QE1F-*Plus* is a 4-channel E1 (2048 kbit/s) framer designed for voice and data communications applications. A dual unipolar or NRZ line interface is supported with full alarm detection and generation per ITU-T G.703 and operates from a power supply of 3.3 or 5 volts.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator Receiver). Programmable multi-rate test pattern generator and receiver in a single chip with serial, nibble, or byte interface capability.

TXC-20163, E3LIM Module (E3 Line Interface Module). A complete and compact full duplex analog line to digital terminal interface that converts an HDB3-encoded line signal, in E3 asynchronous format, to and from NRZ data and clock signals. The E3LIM is packaged as a 2.6 inch x 1.0 inch 50-pin Dual In-Line Package (DIP) Module.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute	Tel: 212-642-4900
11 West 42nd Street	Fax: 212-302-1286
New York, New York 10036	Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

2570 West El Camino Real	Tel: 650-949-6700
Suite 304	Fax: 650-949-6705
Mountain View, CA 94040	Web: www.atmforum.org

ATM Forum Europe Office

Av. De Tervueren 402	Tel: 2 761 66 77
1150 Brussels	Fax: 2 761 66 79
Belgium	Web: www.euroinfo@atmforum.ocm

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F	Tel: 3 3438 3694
1-2-11, Hamamatsucho, Minato-ku	Fax: 3 3438 3698
Tokyo 105-0013, Japan	Web: www.apinfo@atmforum.com

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association	Tel: 800-854-7179 (within U.S.A.)
Global Engineering Documents	Tel: 314-726-0444 (outside U.S.A.)
7730 Carondelet Avenue, Suite 407	Fax: 314-726-6418
Clayton, MO 63105-3329	Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute	Tel: 4 92 94 42 22
650 route des Lucioles	Fax: 4 92 94 43 33
06921 Sophia Antipolis Cedex	Web: www.etsi.org
France	

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)	Tel: 800-669-6857 (within U.S.A.) Tel: 903-769-3717 (outside U.S.A.)
3220 N Street NW, Suite 360	Fax: 508-650-1375
Washington, DC 20007	Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union	Tel: 22 730 5111
Telecommunication Standardization Sector	Fax: 22 733 7256
Place des Nations, CH 1211	Web: www.itu.int
Geneve 20, Switzerland	

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk	Tel: 215-697-2179
Building 4 / Section D	Fax: 215-697-1462
700 Robbins Avenue	Web: www.dodssp.daps.mil
Philadelphia, PA 19111-5094	

PCI SIG (U.S.A.):

PCI Special Interest Group	Tel: 800-433-5177 (within U.S.A.)
2575 NE Kathryn Street #17	Tel: 503-693-6232 (outside U.S.A.)
Hillsboro, OR 97124	Fax: 503-693-8344
	Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.	Tel: 800-521-CORE (within U.S.A.)
Attention - Customer Service	Tel: 908-699-5800 (outside U.S.A.)
8 Corporate Place	Fax: 908-336-2559
Piscataway, NJ 08854	Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunications Technology Committee	Tel: 3 3432 1551 Fax: 3 3432 1553
2nd Floor, Hamamatsucho - Suzuki Building,	Web: www.ttc.or.jp
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo	

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated E123MUX Data Sheet that have significant differences relative to the previous and now superseded E123MUX Data Sheet.

Updated E123MUX Data Sheet: Edition 5, September 1999

Previous E123MUX Data Sheet: Edition 4, February 1999

The page numbers indicated below of this updated Data Sheet include significant changes relative to the previous data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
All	Deleted reference to IEEE 1149.1 standard where applicable.
1, 77, 78	Changed package type to plastic quad flat package (PQFP).
2	Updated Table of Contents and List of Figures.
6	Changed symbols SCANDATA and SCANCK to TESTDATA and TESTCK in the Pin Diagram.
13	Renamed table heading SCAN PINS to TEST PINS. Changed Symbol SCANCK and SCANDATA to TESTCK and TESTDATA for the Symbol columns. Added last sentence to Name/Function column for Symbol $\overline{TRS}$.
16	Changed value for Typ in the Thermal Characteristics table.
22	Changed Max value for $t_{D(2)}$.
36	Added third sentence to second paragraph. Modified the third and fourth paragraph. Modified the IDCODE test instruction for Boundary Scan Operation.
37	Added ‘Device Identification Register’ in Figure 20. Changed Boundary Scan Chain paragraph.
51	Changed first sentence of Device Identifier paragraph.
77	Changed thickness dimensions for package in Figure 21.
79-80	Updated Standard Documentation Sources list.
81	Updated List of Data Sheet Changes.
85	Updated Documentation Update Registration Form.

- NOTES -

- NOTES -

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Marketing	__________	__________

Please describe briefly your intended application(s) and indicate whether you would like to have a TranSwitch applications engineer contact you to provide further assistance:

____

____

____

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If you are also interested in receiving updated documentation for other TranSwitch device types, please list them below rather than submitting separate registration forms:

________ ________ ________ ________ ________ ________ ________

________ ________ ________ ________ ________ ________ ________

Please fold, tape and mail this page (see other side) or fax it to Marketing Communications at 203.926.9453.

Engines for Global Connectivity

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3 Enterprise Drive
Shelton, CT 06484-4694
U.S.A.

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Please complete the registration form on this back cover sheet, and mail or fax it, if you wish to receive updated documentation on selected TranSwitch products as it becomes available.