DS3F Device
DS3 Framer
TXC-03401

DATA SHEET

FEATURES

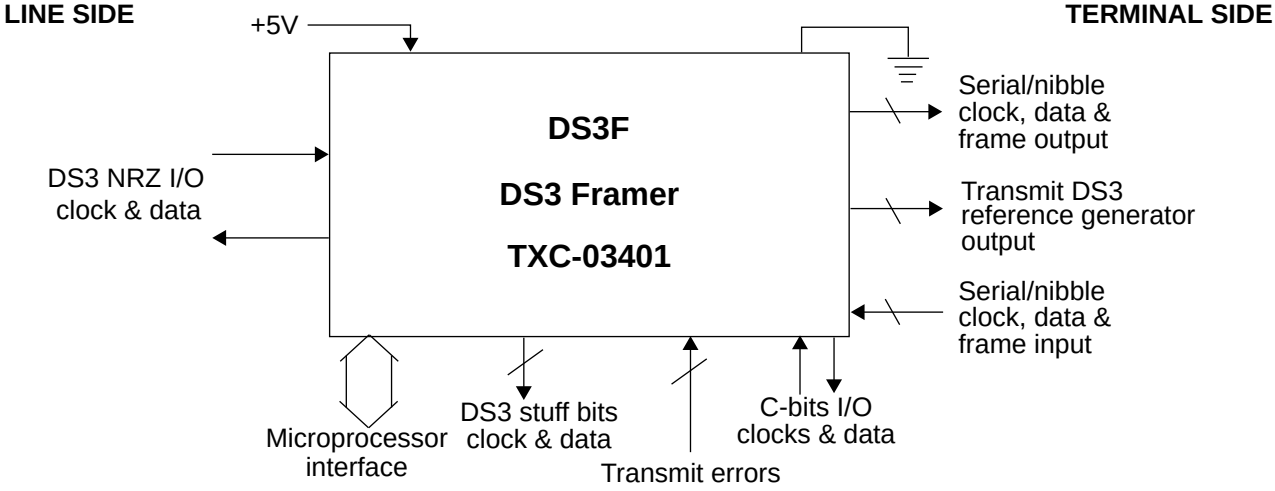
- DS3 payload access, bit-serial or nibble-parallel
- C-bit parity or M13 operating mode
- C-bit interface (13 C-bits in, 14 out)
- Detect and generate DS3 AIS, and idle signals
- Transmit reference generator for serial operation
- Transmit and receive FEAC channel (software)
- Transmit single errors: framing, FEBE, C-bit parity, and P-bit parity
- FEBE, C-bit, and P-bit performance counters
- 68-pin plastic leaded chip carrier

DESCRIPTION

The DS3F is designed for DS3 framer applications in which broadband payloads are mapped into the 44.736 Mbit/s DS3 frame format. Although the C-bit parity format is recommended, the DS3F can also operate in the M13 mode. In the C-bit parity format, the DS3F provides a separate interface for selected C-bits. The DS3F also provides software access for transmitting and receiving the FEAC channel, and generates and detects DS3 AIS, DS3 idle, P-bit parity and C-bit parity. In addition, performance counters are provided, as well as the ability to generate single framing, FEBE, C-bit parity and P-bit parity errors. The payload interface is selectable through software as either a bit-serial or nibble-parallel format.

APPLICATIONS

- Subrate multiplexing
- Wideband data or video transport
- DS3 monitor and test
- Channel extenders
- DS3 test sets



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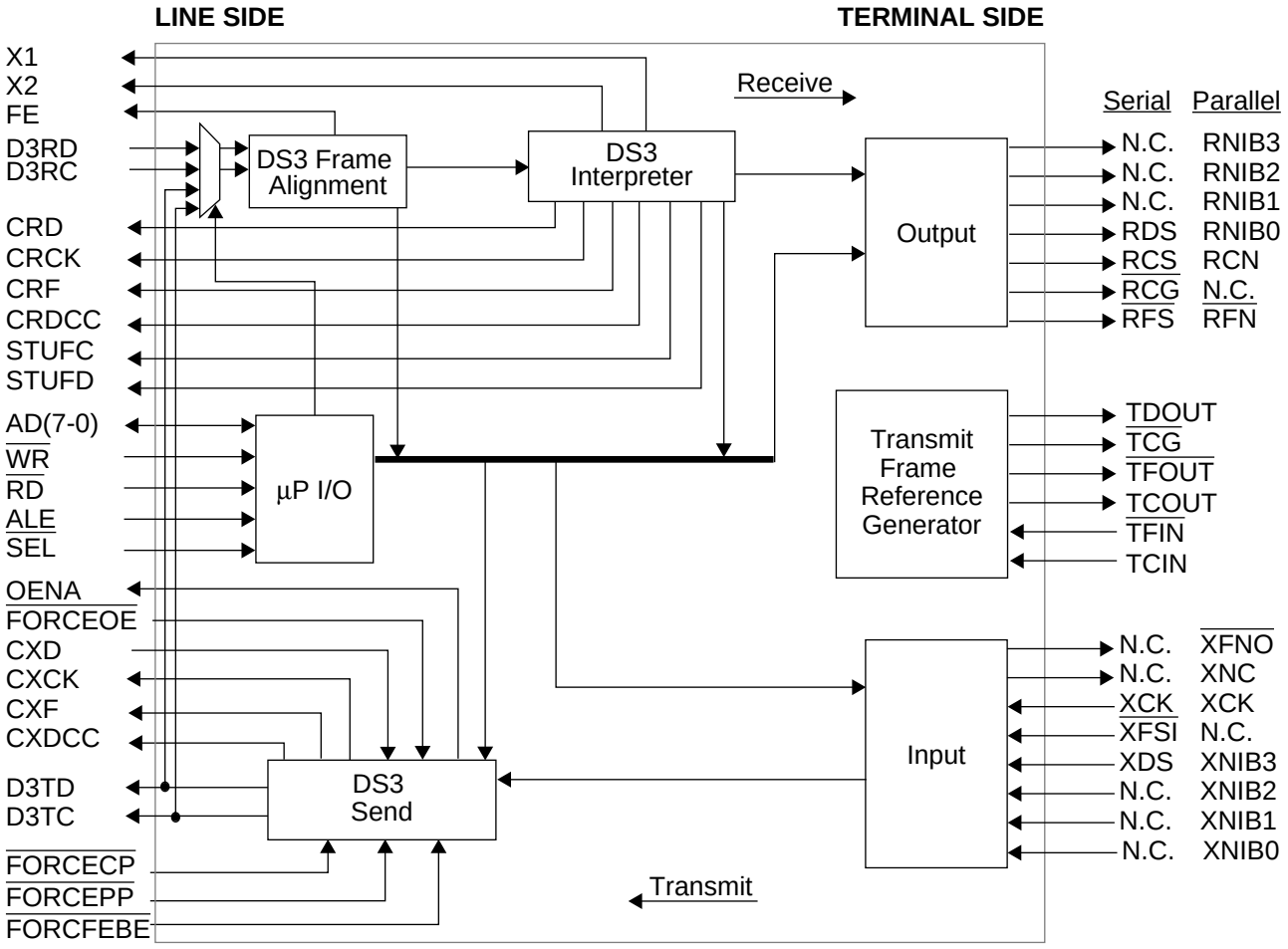


Figure 1. DS3F TXC-03401 Block Diagram

BLOCK DIAGRAM DESCRIPTION

Figure 1 shows the block diagram of the DS3F device

The DS3F receives a line side DS3 data signal (D3RD) and a clock signal (D3RC) from a line interface device such as the TranSwitch ART/ARTE VLSI device (TXC-02020/02021) or DS3LIM-SN module (TXC-20153D). The DS3 Frame Alignment Block performs DS3 frame alignment and monitors the signal and the input clock for loss of signal (LOS), out of frame (OOF), and loss of clock (LOC). A framing error (FE) output is provided to indicate when any of the 28 framing bits in the DS3 signal are in error.

The DS3 Interpreter Block performs P-bit and C-bit parity detection and error counting, receive AIS and idle pattern detection, far end block error (FEBE) detection and error counting, far end alarm and control (FEAC) code word detection, C-bit reception, and X-bit reception. Serial interfaces are provided for the received X-bits and for 14 of the 21 C-bits. The receive C-bit interface consists of a serial data signal (CRD), clock signal (CRCK), framing pulse (CRF), and a data communication link clock signal (CRDCC). The clock signal (CRCK) is gapped and is available only for clocking out C-bits C2 through C6 and C13 through C21. The CRDCC clock signal is present only for C-bits C13, C14, and C15, which are assigned as a data communication channel

when operating in the C-bit parity mode. When operating in the M13 mode, an interface (output pin STUFD) that indicates the state of the stuff opportunity bit during each of the seven DS3 subframes and a clock signal (STUFC) are also provided.

The Output Block provides a bit-serial or a nibble-parallel interface for both C-bit parity and M13 modes of operation. The interface type is selected by writing a control bit in the memory map (SER), and is common to the DS3F receive and transmit circuitry. The signals provided for the bit-serial interface consist of a data signal (RDS), a clock signal (RCS), a receive clock gap signal ($\overline{\text{RCG}}$) and a framing pulse ($\overline{\text{RFS}}$). The nibble-parallel interface consists of the nibble data signal (RNIB3 through RNIB0), a clock out signal (RCN), and a framing pulse out ($\overline{\text{RFN}}$). The RNIB3 bit corresponds to the first bit received in a four-bit serial bit stream segment.

In the transmit direction, the Input Block provides either a bit-serial or nibble-parallel interface. The bit-serial interface consists of a data signal (XDS), a clock signal (XCK), and a framing pulse ($\overline{\text{XFSI}}$). The nibble-parallel interface consists of a data signal (XNIB3 through XNIB0), a clock signal (XCK), a framing pulse ($\overline{\text{XFNO}}$), and a nibble clock signal (XNC). The XNIB3 bit corresponds to the first bit transmitted.

The DS3 Send Block performs P-bit and C-bit parity generation, AIS and idle pattern generation, far end alarm and control (FEAC word) transmission, X-bit insertion, and C-bit insertion. The C-bits may be generated internally (such as C-bit parity), written by the microprocessor (such as the FEAC channel), or provided from the external C-bit interface. The transmit C-bit interface consists of a data input signal (CXD), a clock signal (CXCK), a framing pulse (CXF) and a data communication link clock signal (CXDCC).The DS3 transmit line side interface consists of the data signal (D3TD) and a clock signal (D3TC).

DS3 Transmit-to-Receive (TR) loopback is controlled by setting to 1 a bit in the memory map (3LOOP). The entire device is used when loopback is in effect, but the line side input data and clock are blocked (by the gate preceding the DS3 Frame Alignment Block shown in Figure 1).

The capability to generate and transmit single overhead bit errors is also provided. External interfaces are provided for transmitting a far end block error ($\overline{\text{FORCFEBE}}$), a P-bit parity error ($\overline{\text{FORCEPP}}$), a C-bit parity error ($\overline{\text{FORCECP}}$) and an overhead bit error ($\overline{\text{FORCEOE}}$). The $\overline{\text{FORCEOE}}$ signal is used in conjunction with the enable signal (OENA) for introducing an overhead bit error in the next 85-bit segment of the DS3 frame.

The Transmit Frame Reference Generator Block provides reference timing for bit-serial operation. This block accepts an external 44.736 MHz clock signal (TCIN) and derives a clock signal (TCOUT), a framing pulse ($\overline{\text{TFOUT}}$), a clock gap signal ($\overline{\text{TCG}}$) and a data signal ($\overline{\text{TDOUT}}$). The DS3 data signal consists of framing bits and zeros elsewhere. An optional framing pulse input ($\overline{\text{TFIN}}$) is also provided, but is not required for normal operation.

The DS3F microprocessor bus interface consists of eight bidirectional data and address leads (AD7-AD0), along with other microprocessor control leads. The microprocessor bus is used to write control information and to read status information and alarms.

PIN DIAGRAM

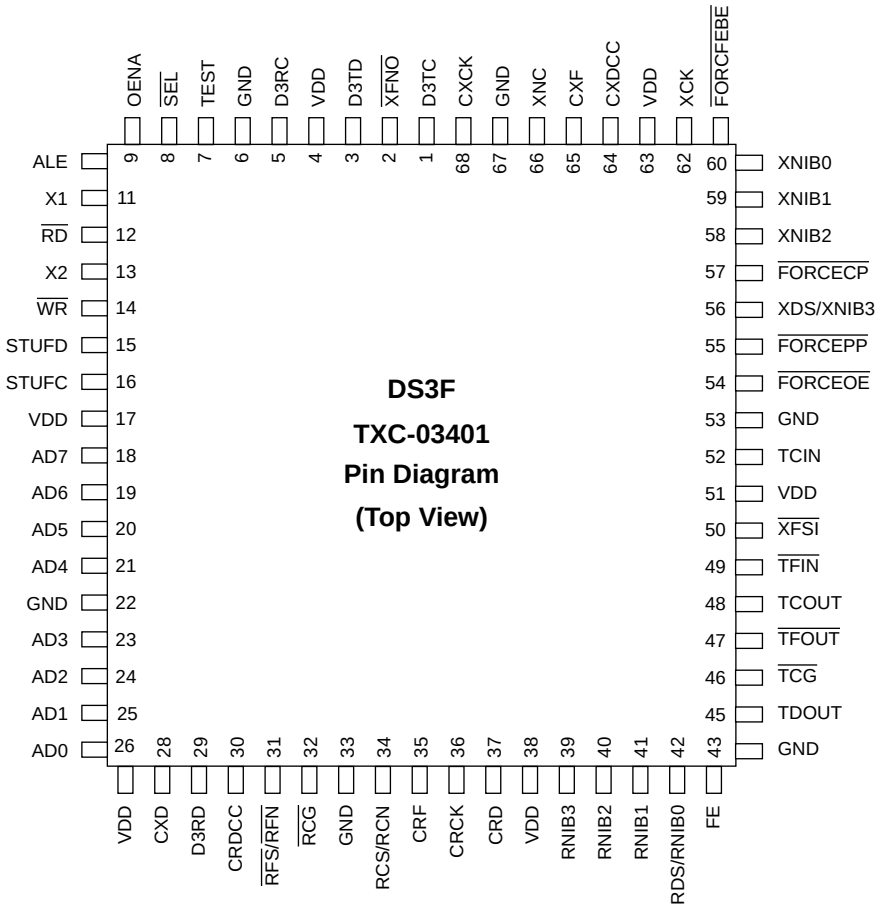


Figure 2. DS3F TXC-03401 Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY AND GROUND

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	4, 17, 27 38, 51, 63	P		**VDD:** +5 volt supply voltage, ± 5%
GND	6, 22, 33 44, 53, 67	P		**Ground:** 0 volts reference.

*Note: I = Input; O = Output; P = Power

DS3 RECEIVE LINE SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type *	Name/Function
D3RC	5	I	CMOS	**DS3 Receive Clock:** A 44.736 MHz clock used for clocking in receive data, and as the time base for the DS3F receiver. Line side serial data is clocked into the DS3F on positive transitions of the clock.
D3RD	29	I	TTL	**DS3 Receive Data:** DS3 line side serial receive data.

DS3 TRANSMIT LINE SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
D3TC	1	O	CMOS4mA	**DS3 Transmit Clock:** A 44.736 MHz clock that is derived from the transmit clock (XCK) signal and is used for clocking out the line side DS3 data signal. Data (D3TD) is clocked out on positive transitions of the clock.
D3TD	3	O	TTL4mA	**DS3 Transmit Data:** DS3 line side serial transmit data.

RECEIVE TERMINAL SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{RFS}}$/$\overline{\text{RFN}}$	31	O	CMOS4mA	**Receive Framing Pulse Serial/Nibble Interface:** The framing pulse is active low for one clock cycle (RCS/RCN), and is synchronous with the first bit 1 in the DS3 frame. For the nibble interface, the framing pulse is synchronous with nibble 1175.
$\overline{\text{RCG}}$	32	O	CMOS4mA	**Receive Clock Gap Signal:** The active low gap signal is synchronous with each overhead bit in the serial DS3 frame (first bit in the 85-bit group).
RCS/RCN	34	O	CMOS4mA	**Receive Clock Serial/Nibble Interface:** Clock used for clocking out the terminal side receive serial and nibble data. This clock is derived from the line side clock (D3RC). Data is clocked out of the DS3F on negative transitions of this clock.
RNIB3 RNIB2 RNIB1 RDS/RNIB0	39 40 41 42	O	TTL4mA	**Receive Nibble/Serial Interface:** Nibble data is clocked out on positive transitions of the nibble clock (RCN). There are 1176 nibbles provided each frame. The data and clock are stretched to accommodate the 56 individual overhead bits (first bit in the 85-bit group), which are not provided at the interface. The first bit received in a nibble is present on RNIB3. The nibble interface is operational in the C-bit parity operating mode only. Serial data (RDS) consists of all the bits in the frame (including the states of the overhead bits), and is operational in either operating mode, M13 or C-bit parity. Serial data is clocked out on negative transitions of the receive clock (RCS).

*See Input, Output and I/O Parameters section for Type definitions.

TRANSMIT TERMINAL SIDE INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{XFNO}}$	2	O	TTL4mA	**Transmit Nibble Interface Framing Pulse:** An active low, one nibble clock cycle wide (XNC) pulse that occurs during the second nibble time.
$\overline{\text{XFSI}}$	50	I	TTLp	**Serial Data Transmit Framing Pulse:** A framing pulse that must be synchronous with bit 1 in the transmit serial data DS3 frame. The DS3F rewrites the 56 overhead bits based on the location of the transmit framing pulse.
XDS/XNIB3 XNIB2 XNIB1 XNIB0	56 58 59 60	I	TTL	**Transmit Nibble/Serial Interface:** Nibble data is clocked in on positive transitions of the nibble clock (XNC). There are 1176 nibbles in each frame. The clock is stretched to accommodate the 56 overhead bits which are not required at the interface. The DS3F inserts the X, F, C, P, and M overhead bits into the transmitted frame based on the framing pulse $\overline{\text{XFNO}}$. The first bit transmitted in a nibble is present on XNIB3. The nibble interface is operational in the C-bit parity mode only. The serial data should consist of all the bits in the frame (4760 bits). The DS3F rewrites the 56 overhead bits in the frame based on the location of the framing pulse $\overline{\text{XFSI}}$, when operating in the C-bit parity mode. In the M13 operating mode, the 21 C-bits are treated as user data, while the other overhead bits (X, F, P, and M bits) are written into the DS3 frame by the DS3F. Serial data is clocked into the DS3F on positive transitions of the transmit clock (XCK).
XCK	62	I	CMOS	**Transmit Clock:** Provides the time base for the transmitter in the DS3F. In order to meet cross-connect objectives, the clock must operate at 44.736 Mbit/s with a stability of ±20 ppm and a duty cycle of 50 ±10%. If XCK fails, the DS3F uses the D3RC receive clock in its place.
XNC	66	O	TTL4mA	**Transmit Nibble Clock:** Clock signal derived from the transmit clock (XCK). This clock is stretched in order to accommodate the 56 overhead bit positions which are not required by the external terminal circuitry for the nibble interface (XNIBn).

TRANSMIT REFERENCE GENERATOR INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
TDOUT	45	O	TTL4mA	**Transmit Reference Generator Data Output:** DS3 frames are provided on this output that contain either all zeros or all ones. The number of frames with ones is 7 of every 18 frames. The pattern of the ones is one frame of every three for 15 frames and two of the last 3 of the 18-frame group; this completes the 7 of 18 pattern. The purpose of this pattern is to ease the requirement to provide an all-ones and all-zeros C-bit pattern to insure a DS2 frequency that is very nearly equal to its specified value.
$\overline{\text{TCG}}$	46	O	TTL4mA	**Transmit Reference Generator Clock Gap Signal:** An active low, one clock cycle wide (TCOUT) signal that is synchronous with bit 1 in each 85-bit group (56 overhead bits) in the DS3 frame.
$\overline{\text{TFOUT}}$	47	O	TTL4mA	**Transmit Reference Generator Framing Pulse:** An active low, one clock cycle wide (TCOUT) pulse that is synchronous with bit 1 in the DS3 frame. May be used as the serial data transmit framing pulse ($\overline{\text{XFSI}}$) if properly delayed by the payload multiplexer circuitry.
TCOUT	48	O	CMOS4mA	**Transmit Reference Generator Clock Out:** Clock signal that is derived from the transmit reference generator clock input (TCIN). Provides a time base for multiplexing an external payload into the serial signal TDOUT provided by the reference generator. May be used as the transmit input clock (XCK) in the serial mode. Transmit reference generator signals are clocked out on positive transitions of this clock.
TCIN	52	I	TTL	**Transmit Reference Generator Clock In:** Provides a time base for generating the various signals in the DS3F transmit reference generator. In order to meet DS3 cross-connect objectives, this clock must operate at 44.736 Mbit/s with a stability of ±20 ppm and a duty cycle of 50 ±10%.

RECEIVE C-BIT INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
CRDCC	30	O	TTL4mA	**C-Bit Receive Data Link Clock:** A gapped clock provided for clocking the three data link bits (C13, C14, and C15) into external circuitry from the serial data (CRD). The rising edge of CRDCC indicates when valid data is available.
CRF	35	O	TTL4mA	**C-Bit Receive Framing Pulse:** Provides a time base reference for clocking in the C-bits in a DS3 frame.

Symbol	Pin No.	I/O/P	Type	Name/Function
CRCK	36	O	TTL4mA	**C-Bit Receive Clock:** A gapped clock which clocks C-bit data out of the DS3F. The falling edge of CRCK indicates when valid data is available.
CRD	37	O	TTL4mA	**C-Bit Receive Data:** Serial interface for receiving the following C-bits in the C-bit parity mode: C2, C3, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21. Availability of data is indicated by the clock signals CRDCC and CRCK, described above.

TRANSMIT C-BIT INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
CXD	28	I	TTL	**C-Bit Transmit Data:** Serial interface for transmitting the following C-bits in the C-bit parity mode: C2, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21. C-bit data is clocked into the DS3F on positive transitions of the C-bit gapped clock (CXCK). A C-bit must be transmitted as a one if not used.
CXDCC	64	O	TTL4mA	**C-Bit Transmit Data Link Clock:** A gapped clock provided for clocking the three data link bits (C13, C14, and C15).
CXF	65	O	TTL4mA	**C-Bit Transmit Framing Pulse:** Identifies the location of the first C-bit in the DS3 frame.
CXCK	68	O	TTL4mA	**C-Bit Transmit Clock:** A gapped clock which clocks the external C-bit serial data into the DS3F on positive transitions.

OTHER SIGNALS

Symbol	Pin No.	I/O/P	Type	Name/Function
TEST	7	I	TTLp	**TranSwitch Test Pin:** Leave open.
OENA	9	O	TTL4mA	**Overhead Enable:** An active high signal that enables an overhead error to be introduced into the overhead bit in the next 85th group by placing a low on the $\overline{\text{FORCEOE}}$ lead.
X1	11	O	TTL4mA	**DS3 Received X-Bit 1:** An output indication of the state of the first X-bit received in the DS3 frame (bit 1). The indication is active until the next X1 state is detected.
X2	13	O	TTL4mA	**DS3 Received X-Bit 2:** An output indication of the state of the second X-bit received in the DS3 frame (bit 680). The indication is active until the next X2 state is detected.

Symbol	Pin No.	I/O/P	Type	Name/Function
STUFD	15	O	TTL4mA	**Stuff Data Status:** This interface provides an indication of the state of the stuff opportunity bit from the received DS3 frame. For an M13 DS3 formatted signal, the first stuff opportunity bit occurs in the first bit after F4 (last 85-bit group) in subframe 1, and the last stuff opportunity bit in the frame occurs in the seventh bit after F4 (last 85-bit group) in subframe 7.
STUFC	16	O	TTL4mA	**Stuff Clock:** Provided for clocking out the stuff opportunity bit state. The positive transition occurs at the start of the first C-bit (Cn1) in a subframe and the negative transition occurs at the end of the 85-bit group.
FE	43	O	TTL4mA	**Framing Error Indication:** The FE pin will go high for every F-bit framing error. It stays high for a period of 1.9µs (85 clock periods). During an Out of Frame condition the FE pin will toggle irregularly between high and low at intervals of 85 clock cycles, depending on frame search pattern matching at each interval.
$\overline{\text{TFIN}}$	49	I	TTLp	**Transmit Framing Input:** An optional active low input signal which resets the counters of the Transmit Frame Reference Generator block to zero and holds the output signals of the block to their corresponding states.
$\overline{\text{FORCEOE}}$	54	I	TTLp	**Force DS3 Overhead Bit Error:** An active low signal used in conjunction with the overhead enable signal (OENA) for introducing an overhead bit error in the next transmitted 85-bit group.
$\overline{\text{FORCEPP}}$	55	I	TTLp	**Force P-Bit Parity Error:** An active low signal generates and transmits a P-bit error by inverting both P-bits. If an active low signal is applied during the first subframe of the DS3 frame, the error is transmitted in that frame. Otherwise the error is transmitted in the next frame.
$\overline{\text{FORCECP}}$	57	I	TTLp	**Force C-Bit Parity Error:** An active low signal generates and transmits a C-bit parity error when operating in the C-bit parity mode. The error is transmitted by inverting C7, C8, and C9 (C-bit parity value) in subframe 3. If the active low signal is applied during the first subframe of the DS3 frame, the error is transmitted in that frame. Otherwise the error is transmitted in the next frame.
$\overline{\text{FORCFEBE}}$	61	I	TTLp	**Force FEBE Error:** An active low signal generates and transmits a far end block error (FEBE) when operating in the C-bit parity mode. If the active low signal is applied during the first subframe of the DS3 frame, the error is transmitted in that frame. Otherwise the error is transmitted in the next frame.

MICROPROCESSOR INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{SEL}$	8	I	TTL	**Microprocessor Select:** A low enables the microprocessor to access the DS3F memory map for control, status and alarm information.
ALE	10	I	TTL	**Address Latch Enable:** An active high signal generated by the microprocessor. Used by the microprocessor to hold an address stable during a read/write bus cycle on the falling edge.
$\overline{RD}$	12	I	TTL	**Read:** An active low signal generated by the microprocessor for reading the registers which reside in the DS3F memory map. The DS3F memory I/O is selected by placing a low on the select lead.
$\overline{WR}$	14	I	TTL	**Write:** An active low signal generated by the microprocessor for writing to the registers which reside in the memory map. The DS3F memory I/O is selected by placing a low on the select lead.
AD(7-4) AD(3-0)	18-21 23-26	I/O	TTL8mA	**Address/Data Bus:** These leads constitute the time multiplexed address and data bus for accessing the registers which reside in the DS3F memory map.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min*	Max*	Unit
Supply voltage	V_{DD}	-0.3	+7.0	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Continuous power dissipation	P_C		1.0	Watts
Ambient operating temperature	T_A	-40	85	^oC
Operating junction temperature	T_J		150	^oC
Storage temperature range	T_S	-55	150	^oC

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		40	42	$^oC/W$	

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}			150	mA	
P_{DD}			790	mW	Inputs switching

INPUT, OUTPUT AND I/O PARAMETERS

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Input Parameters For TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		0.5	1.4	mA	$V_{DD} = 5.25$; Input = 0 volts
Input capacitance		5.5		pF	

Note: Input has a 9K (nominal) internal pull-up resistor.

Input Parameters For CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			1.65	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.8	6.5	9.2	ns	C_{LOAD} = 15 pF
t_{FALL}	1.3	2.3	3.4	ns	C_{LOAD} = 15 pF

Output Parameters For CMOS4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	1.4	2.9	4.2	ns	C_{LOAD} = 15 pF
t_{FALL}	1.3	2.3	3.4	ns	C_{LOAD} = 15 pF

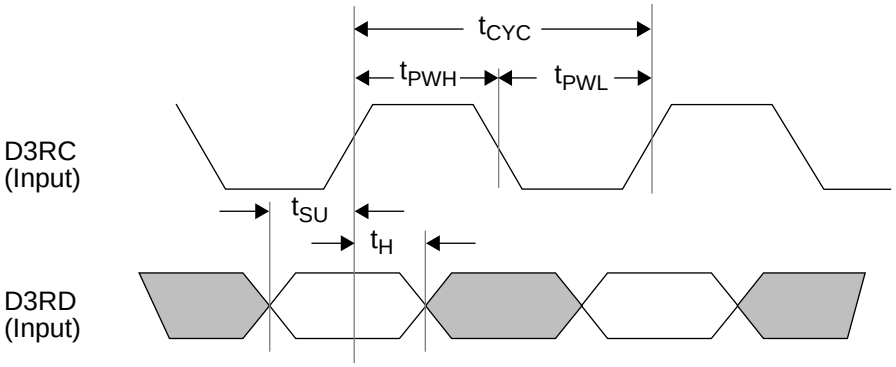
Input/Output Parameters For TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 ≤V_{DD} ≤ 5.25
V_{IL}			0.8	V	4.75 ≤V_{DD} ≤ 5.25
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		5.5		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	2.4	4.9	7.0	ns	C_{LOAD} = 25 pF
t_{FALL}	1.1	1.8	2.5	ns	C_{LOAD} = 25 pF

TIMING CHARACTERISTICS

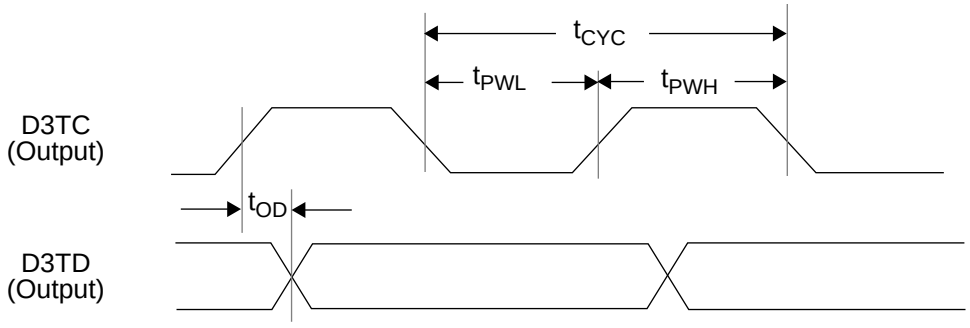
Detailed timing diagrams for the DS3F are illustrated in Figures 3 through 16, with values of the timing intervals following each figure. All output times are measured with a maximum 75 pF load capacitance. Timing parameters are measured at $(V_{OH} + V_{OL})/2$ or $(V_{IH} + V_{IL})/2$, as applicable.

Figure 3. Line Side DS3 Receive Input Timing



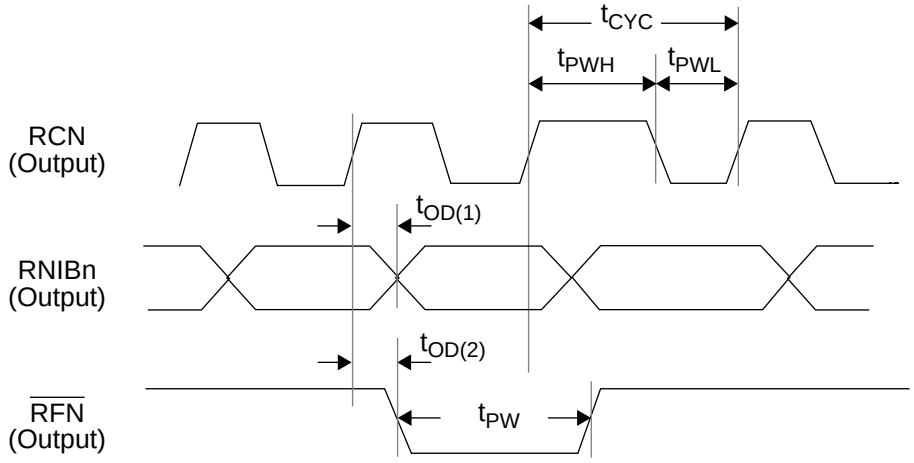
Parameter	Symbol	Min	Typ	Max	Unit
D3RC clock period	t_{CYC}	20	22.35		ns
D3RC high time	t_{PWH}	8			ns
D3RC low time	t_{PWL}	8			ns
D3RC duty cycle (t_{PWH}/t_{CYC})	--	40	50	60	%
D3RD set-up time to D3RC↑	t_{SU}	4			ns
D3RD hold time after D3RC↑	t_H	6			ns

Figure 4. Line Side DS3 Transmit Output Timing



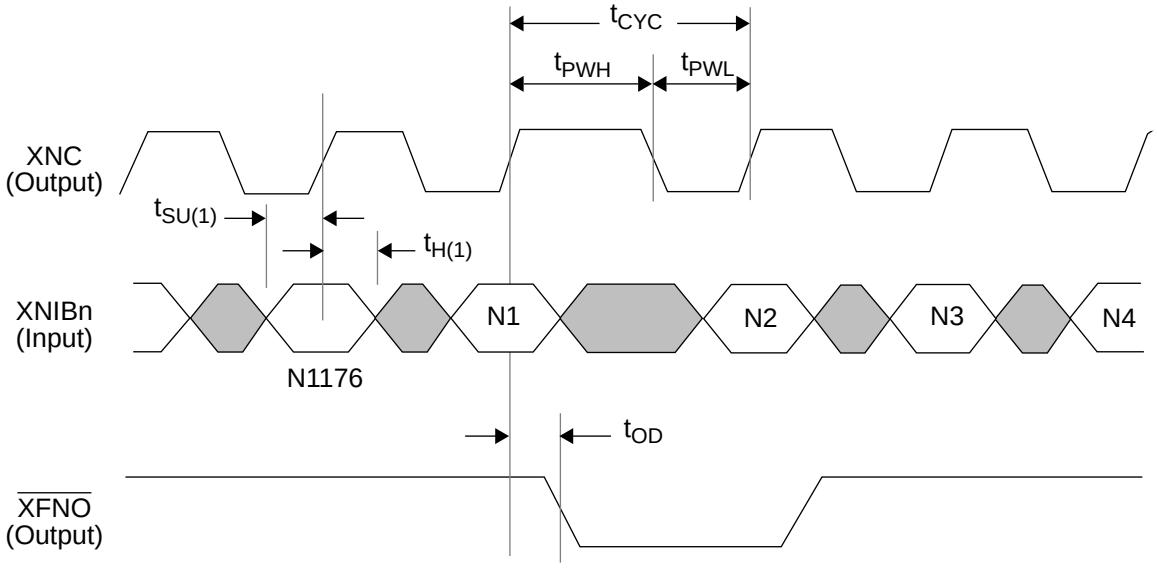
Parameter	Symbol	Min	Typ	Max	Unit
D3TC clock period	t_{CYC}	20	22.35		ns
D3TC high time	t_{PWH}	8			ns
D3TC low time	t_{PWL}	8			ns
D3TD output delay after D3TC↑	t_{OD}	4		8	ns

Figure 5. Terminal Side Receive Nibble Output Timing



Parameter	Symbol	Min	Typ	Max	Unit
RCN clock period	t_{CYC}	89	90.5	111	ns
RCN high time	t_{PWH}	40			ns
RCN low time	t_{PWL}	40			ns
RNIBn delay after RCN ↑	$t_{OD(1)}$	20	23	26	ns
$\overline{RFN}$ delay after RCN ↑	$t_{OD(2)}$	20	23	26	ns
$\overline{RFN}$ pulse width	t_{PW}	89	1 t_{CYC}	93	ns

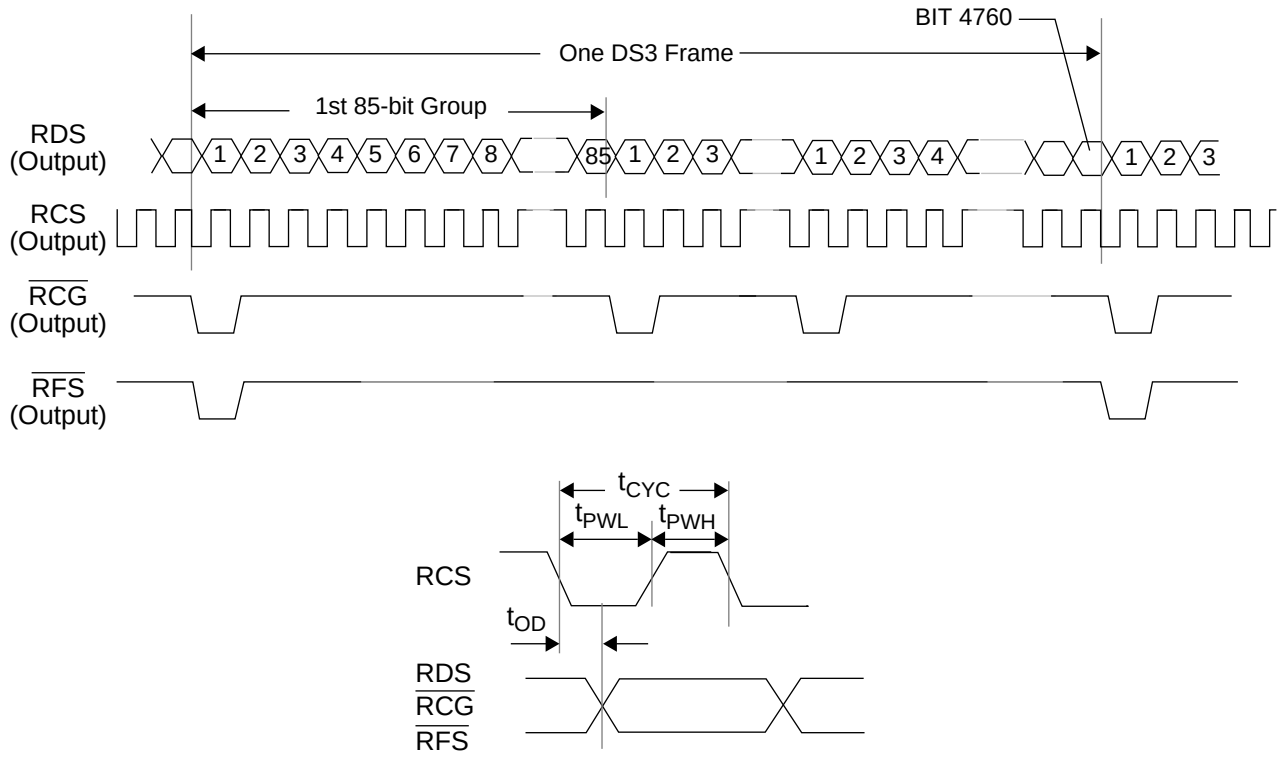
Figure 6. Terminal Side Transmit Nibble Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
XNC clock cycle	t_{CYC}	89.0	90.5	111	ns
XNC high time	t_{PWH}	40		63	ns
XNC low time	t_{PWL}	40		50	ns
XNIBn set-up time to XNC↑	$t_{SU(1)}$	26			ns
XNIBn hold time after XNC↑	$t_{H(1)}$	-14			ns
$\overline{\text{XFNO}}$ output delay after XNC↑	t_{OD}	8	10	12	ns

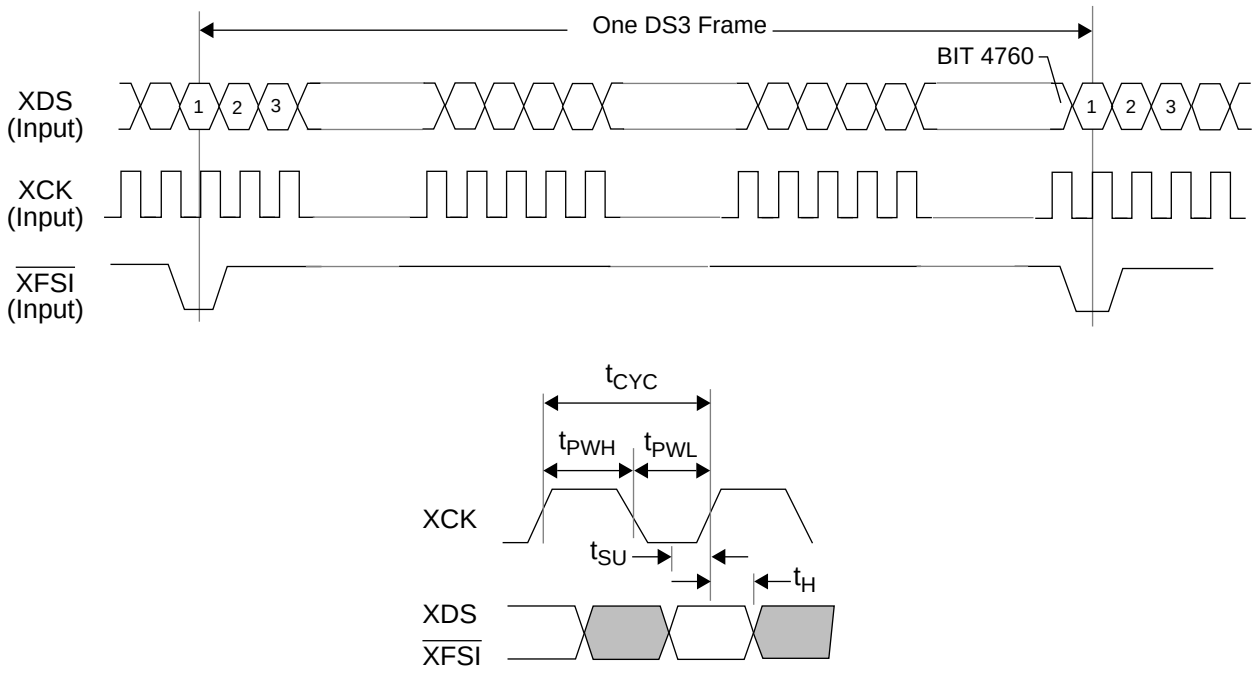
Note: XNIB data input is latched at the midpoint of XNC low.

Figure 7. Terminal Side Receive Serial Output Timing



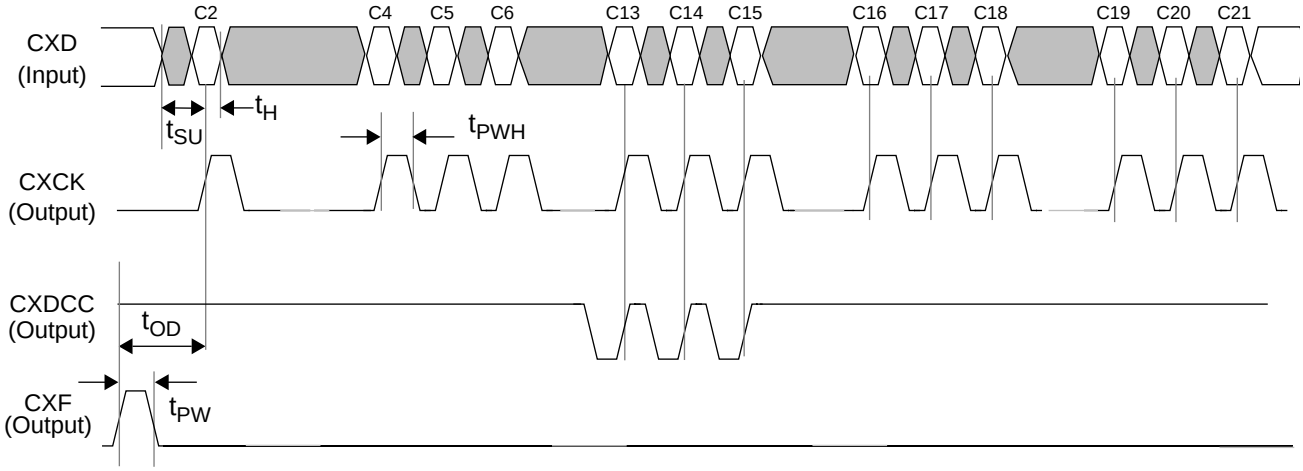
Parameter	Symbol	Min	Typ	Max	Unit
RCS clock period	t_{CYC}	20	22.35		ns
RCS high time	t_{PWH}	8			ns
RCS low time	t_{PWL}	8			ns
RDS, $\overline{RCG}$, $\overline{RFS}$ output delay after RCS↓	t_{OD}	0	2.5	5	ns

Figure 8. Terminal Side Transmit Serial Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
XCK clock period	t_{CYC}	20	22.35		ns
XCK high time	t_{PWH}	8			ns
XCK low time	t_{PWL}	8			ns
XDS, $\overline{XFSI}$ set-up time to XCK↑	t_{SU}	6		10	ns
XDS, $\overline{XFSI}$ hold time after XCK↑	t_H	4		10	ns

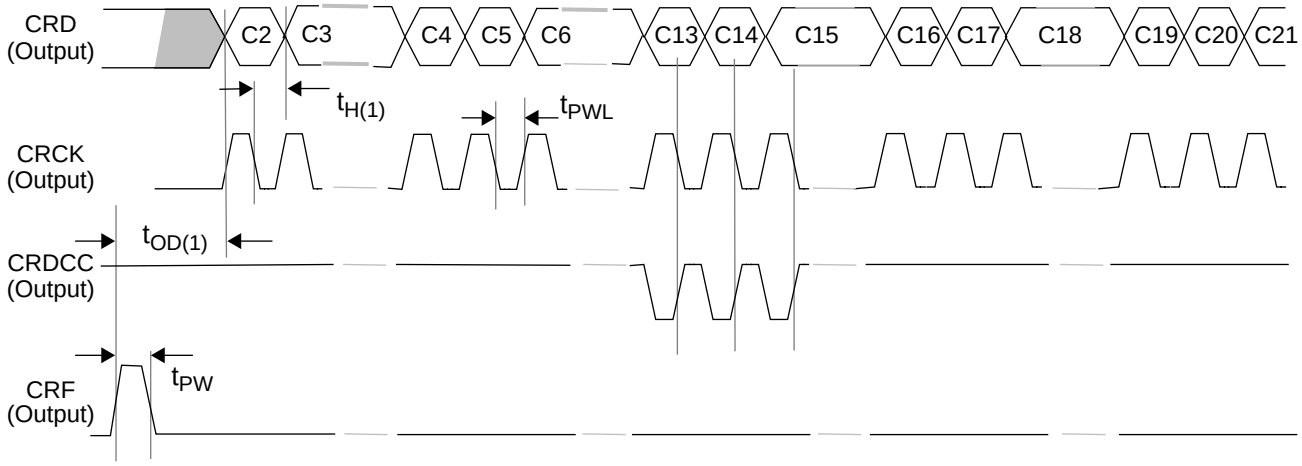
Figure 9. C-Bit Transmit Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
CXCK high time	t_{PWH}		85 t_{CYC}		ns
CXD set-up time to CXCK↑	t_{SU}	20			ns
CXD hold time after CXCK↑	t_H	40			ns
CXCK output delay after CXF↑	t_{OD}		170 t_{CYC}		ns
CXF pulse width	t_{PW}		85 t_{CYC}		ns

Note: t_{CYC} is the D3TC clock period (see Figure 4).

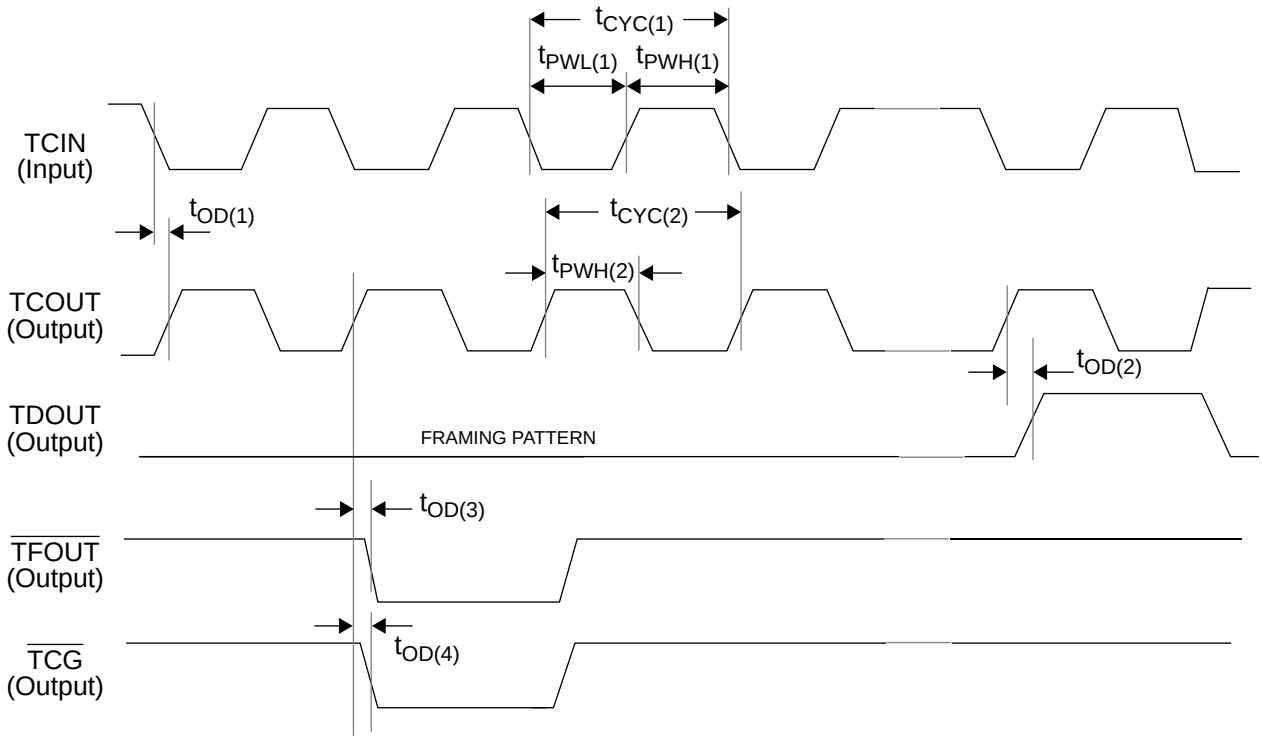
Figure 10. C-Bit Receive Output Timing



Parameter	Symbol	Min	Typ	Max	Unit
CRCK low time	t_{PWL}		85 t_{CYC}		ns
CRD hold time after CRCK↓	$t_{H(1)}$		85 t_{CYC}		ns
CRCK output delay after CRF↑	$t_{OD(1)}$		170 t_{CYC}		ns
CRF pulse width (high)	t_{PW}		85 t_{CYC}		ns

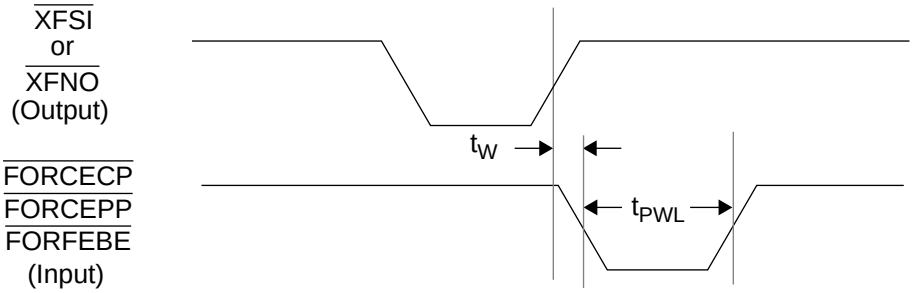
Note: t_{CYC} is the RCS clock period (see Figure 7).

Figure 11. Transmit Reference Generator Timing



Parameter	Symbol	Min	Typ	Max	Unit
TCIN clock period	$t_{CYC(1)}$	20	22.3		ns
TCIN high time	$t_{PWH(1)}$	10	11.2		ns
TCIN low time	$t_{PWL(1)}$	10	11.2		ns
TCIN duty cycle ($t_{PWH(1)}/t_{CYC(1)}$)	--	40	50	60	%
TCOUT clock period	$t_{CYC(2)}$	$t_{CYC(1)}$	22.3		ns
TCOUT high time	$t_{PWH(2)}$	$t_{PWH(1)}$	11.2		ns
TCOUT output delay after TCIN↓	$t_{OD(1)}$	2	4		ns
TDOUT output delay after TCOUT↑	$t_{OD(2)}$	2	4	7	ns
$\overline{\text{TFOUT}}$ output delay after TCOUT↑	$t_{OD(3)}$	2	4	7	ns
$\overline{\text{TCG}}$ output delay after TCOUT↑	$t_{OD(4)}$	2	4	7	ns

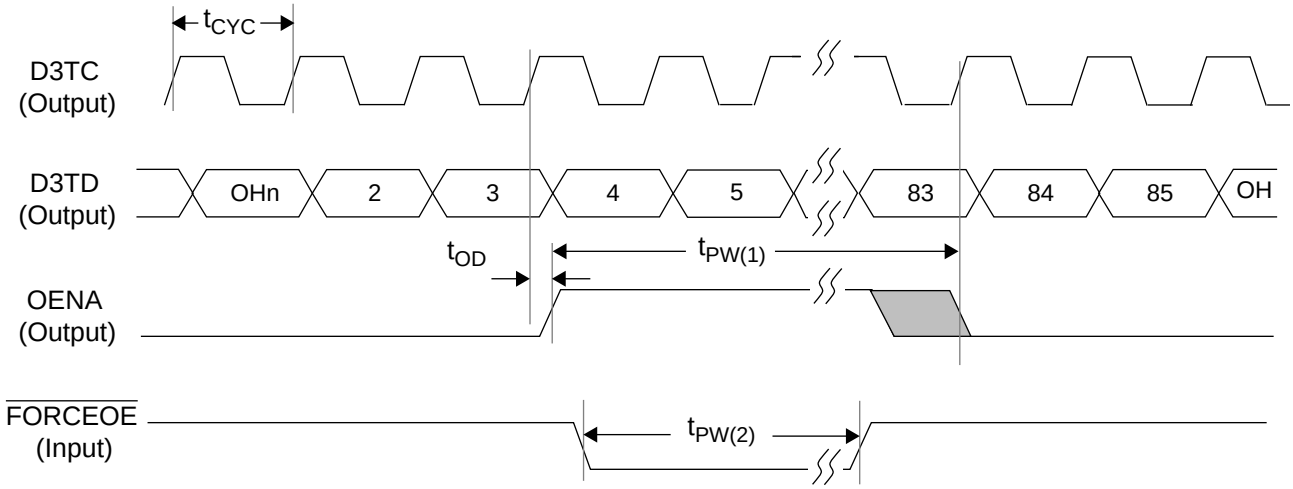
Figure 12. Force Error Timing (C-Bit Parity, P-Bit Parity, FEBE)



Parameter	Symbol	Min	Typ	Max	Unit
Force error wait time after framing pulse	t_W			Note	ns
Force error low time	t_{PWL}	20	22		ns

Note: If the force error signal occurs during the first subframe of the DS3 frame (680 XCK clock cycles), then the error occurs during that frame. Otherwise, the error is transmitted in the next frame.

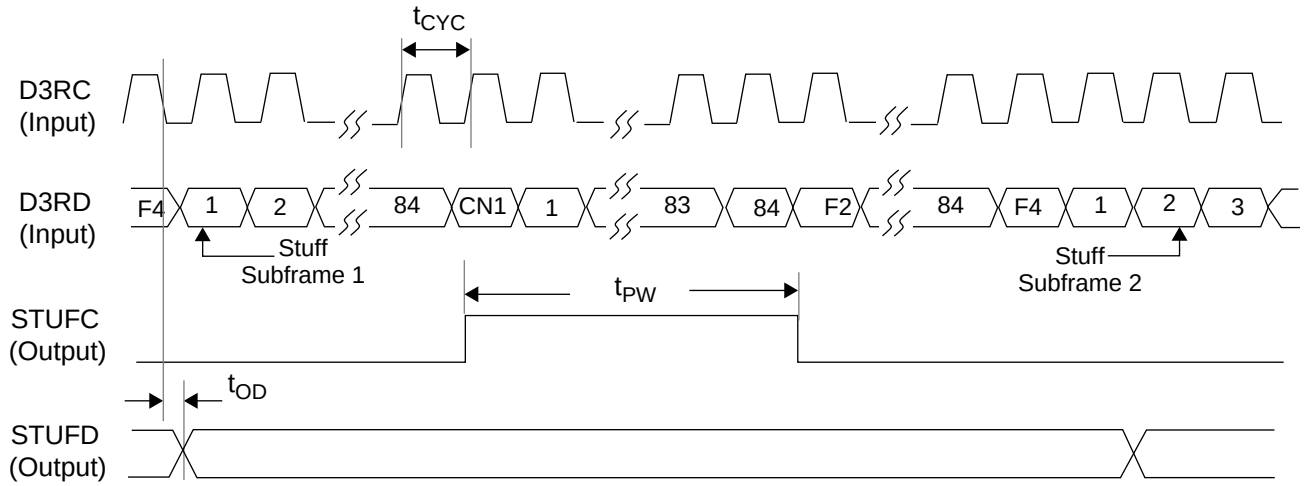
Figure 13. Force Overhead Bit Error Timing (FORCEOE)



Parameter	Symbol	Min	Typ	Max	Unit
D3TC clock period	t_{CYC}	20	22.35		ns
OENA output delay after D3TC↑	t_{OD}	10			ns
OENA pulse width (high)	$t_{PW(1)}$	9 t_{CYC}		80 t_{CYC}	ns
FORCEOE pulse width (low)	$t_{PW(2)}$	9 t_{CYC}		45 t_{CYC}	ns

Note: FORCEOE↑ resets OENA.

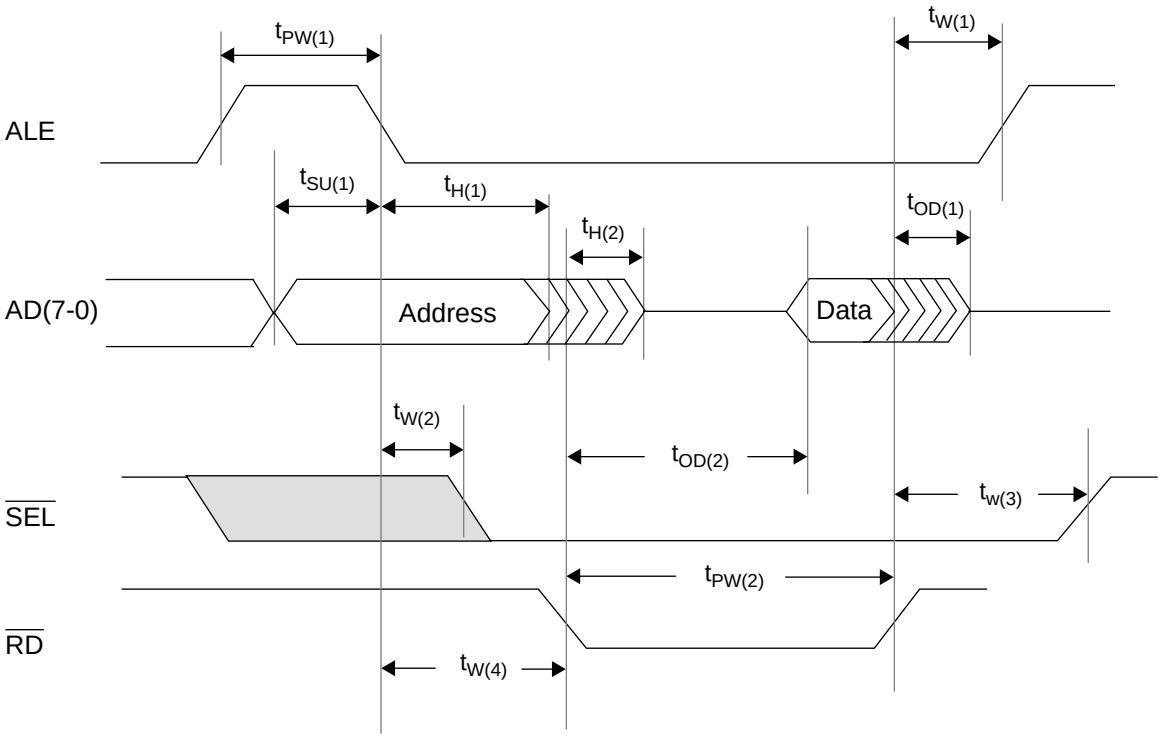
Figure 14. Stuff Opportunity Bit Timing (M13 Mode)



Parameter	Symbol	Min	Typ	Max	Unit
D3RC clock period	t_{CYC}		22.35		ns
STUFC pulse width (high)	t_{PW}		1900		ns
STUFD output delay after D3RC↓	t_{OD}		See Note		ns

Note: The clock STUFC is intended to be used to strobe the data STUFD. It is a low-frequency signal, with a 7.6 microseconds setup of STUFD to STUFC↑ and more than 3.8 microseconds hold time of STUFD after STUFC↑. The timing is counted down from the D3RC clock and will vary accordingly.

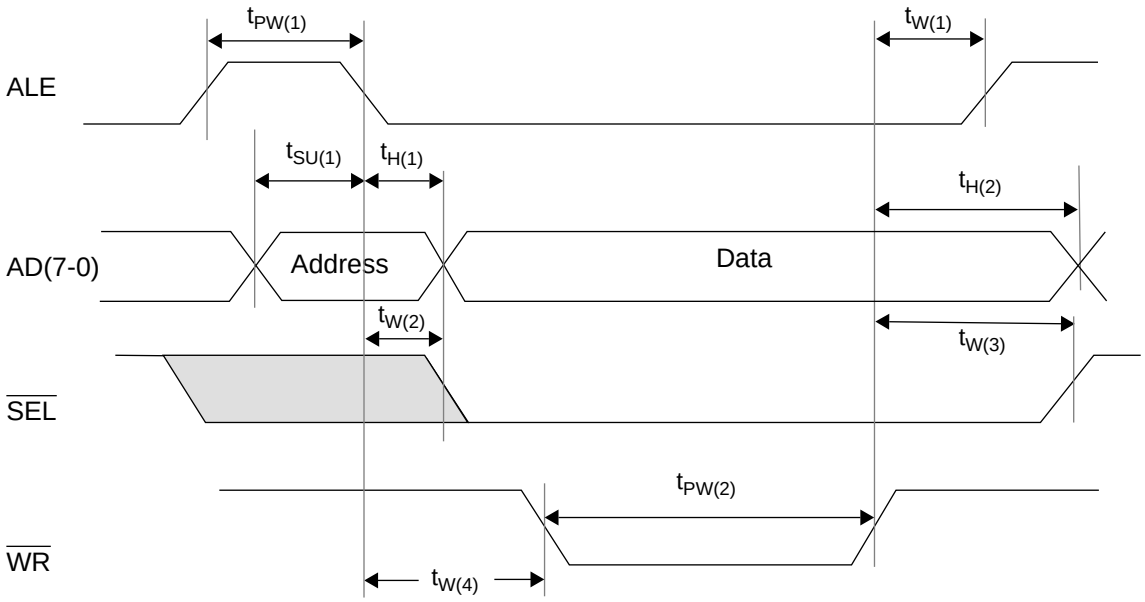
Figure 15. Microprocessor Read Cycle



Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	30			ns
ALE wait after $\overline{RD}$ ↑	$t_{W(1)}$	0			ns
Address set-up time to ALE ↓	$t_{SU(1)}$	20			ns
Address hold time after ALE ↓	$t_{H(1)}$	10			ns
Address hold time after $\overline{RD}$ ↓	$t_{H(2)}$			50	ns
Data output delay (to tristate) after $\overline{RD}$ ↑	$t_{OD(1)}$	10		20	ns
Data output delay after $\overline{RD}$ ↓	$t_{OD(2)}$			80	ns
$\overline{SEL}$ wait after ALE↓	$t_{W(2)}$			40	ns
$\overline{SEL}$ wait after $\overline{RD}$ ↑	$t_{W(3)}$	40			ns
$\overline{RD}$ pulse width	$t_{PW(2)}$	100			ns
$\overline{RD}$ wait after ALE ↓	$t_{W(4)}$	50			ns

Notes:
1. The transmit clock (XCK) or receive clock (D3RC) must be present for the microprocessor bus interface to operate.
2. A minimum of 10 clock cycles must occur after power-up, before the read cycles are valid.

Figure 16. Microprocessor Write Cycle



Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	50			ns
ALE wait after $\overline{WR}$ ↑	$t_{W(1)}$	0			ns
Address set-up time to ALE ↓	$t_{SU(1)}$	30			ns
Address hold time after ALE ↓	$t_{H(1)}$	10			ns
Data hold time after $\overline{WR}$ ↑	$t_{H(2)}$	20			ns
$\overline{SEL}$ wait after ALE↓	$t_{W(2)}$			40	ns
$\overline{SEL}$ wait after $\overline{WR}$↑	$t_{W(3)}$	40			ns
$\overline{WR}$ pulse width	$t_{PW(2)}$	50			ns
$\overline{WR}$ wait after ALE ↓	$t_{W(4)}$	50			ns

Notes:
1. The transmit clock (XCK) or receive clock (D3RC) must be present for the microprocessor bus interface to operate.
2. A minimum of 10 clock cycles must occur after power-up, before the write cycles are valid.

OPERATION

POWER, GROUND AND EXTERNAL COMPONENTS

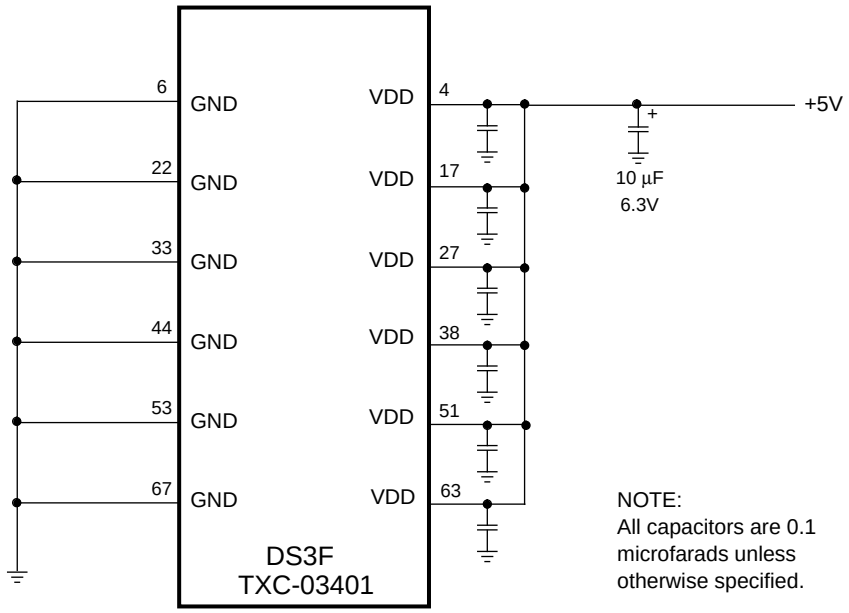


Figure 17. Power Supply Connections

Figure 17 shows the recommended power and ground connection method for the DS3F device. Separate planes should be employed for VDD and GND. Bypass networks consist of a 10 µF capacitor in parallel with 0.1 µF capacitors for each VDD pin, as shown. These 0.1 µF capacitors should be RF-quality and closely connected to each of the device's VDD pins to decouple them to ground.

THROUGHPUT DELAYS

The DS3F throughput delays for the serial terminal interface are given below in terms of DS3 bit times (1 bit = 22.35 nsec nominal):

1. The throughput delay from the transmit terminal side input to the transmit line side output is 3 bit times.

2. The throughput delay from the receive line side input to the receive terminal side output is 2 bit times.

MEMORY MAP

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	R	RXLOS	RXOOF	RXAIS	RXIDL	RXLOC	TXLOC	XRX2	XRX1
01	R/W	NOFEBE	TXAIS	ENAIS	TXIDL	M13MODE	SER	3LOOP	XTX
02	R	FEBE / Framing Bit Error Performance Counter (saturating counter, clears when read)							
03	R	C-Bit Parity Error Performance/Number of Frames Counter (saturating counter, clears when read)							
04	R	P-Bit Parity Error Performance Counter (saturating counter, clears when read)							
05	R/W	TEST	START	FEAC Transmit Data					
06	R	--	NEW	FEAC Receive Data					
07	R(L)	RXLOS	RXOOF	RXAIS	RXIDL	CERR	LOC	X2ERR	X1ERR

*Note: R = Read-only; R(L) = Read-only, latched (clears on read); R/W = Read/Write.

MEMORY MAP DESCRIPTIONS

Address	Bit	Symbol	Description
00	7	RXLOS	**Receive DS3 Loss of Signal:** A receive LOS alarm occurs when the incoming DS3 data (D3RD) is stuck low for at least 1987 clock cycles (D3RC). Recovery occurs when two or more ones are detected in the incoming data bit stream.
	6	RXOOF	**Receive DS3 Out Of Frame:** A Receive Out Of Frame condition is declared, and the RXOOF bit is set to 1, when five out of twelve consecutive F-bits are in error. Recovery to 0 occurs when the repeating F-bit framing sequence 1001.... is detected for twelve consecutive F-bits and the M-bit framing sequence of 010 is detected for one frame. Recovery takes approximately 0.95 ms, worst case. When RXOOF is 1, the performance counters at Addresses 02H, 03H and 04H are inhibited, and the terminal side output is all ones.
	5	RXAIS	**Receive DS3 Alarm Indication Signal (AIS):** A Receive DS3 AIS condition is declared, and the RXAIS bit is set to 1, when RXOOF is 0 and all of the following events have occurred during a frame: the three C-bits in each subframe are 0, and at least 95% of the payload of subframe 1 contains a repeating 1010.... bit sequence which begins after each overhead bit. Recovery to 0 occurs when 31 C-bits with 1 values are counted before 128 C-bits with 0 values are counted, or when less than 95 per cent of the payload of subframe 1 contains a repeating 1010.... bit sequence which begins after each overhead bit. The AIS detection conforms to the bit error rate requirement stated in Bellcore document TR-TSY-000191 (Issue 1, May 1986), "Alarm Indication Signal Requirements and Objectives."

Address	Bit	Symbol	Description
00	4	RXIDL	**Receive DS3 Idle:** A Receive DS3 Idle condition is declared, and the RXIDL bit is set to 1, when RXOOF is 0 and all of the following events have occurred during a frame: the C7, C8 and C9 bits in subframe 3 are 0, and at least 95 per cent of the payload of subframe 7 contains a repeating 1100.... bit sequence which begins after each overhead bit. Recovery to 0 occurs at the end of the first subsequent frame during which not all of these events occur.
	3	RXLOC	**Receive DS3 Loss of Clock:** An alarm occurs when the receive clock (D3RC) is stuck high or low for 125-175 ns. The demultiplexer does not function when the receive clock is lost. Recovery occurs on the first clock transition.
	2	TXLOC	**External (Transmit) DS3 Clock Failure:** A transmit DS3 clock failure alarm occurs when the input clock (XCK) is stuck high or low for 125-175 ns. A failure causes the receive clock to become the transmit clock. This permits the microprocessor interface and transmitter to continue to function. Recovery occurs when the first clock transition is detected.
	1	XRX2	**Receive X-Bit Number 2:** This bit position indicates the receive state of X2. This bit position is updated each frame.
	0	XRX1	**Receive X-Bit Number 1:** This bit position indicates the receive state of X1. This bit position is updated each frame.
01	7	NOFEBE	**FEBE Transmission Disabled:** A one written into this position disables the transmission of a FEBE when a frame alignment error or C-bit parity occurs.
	6	TXAIS*	**Transmit DS3 Alarm Indication Signal:** A one written into this bit position causes the DS3F to transmit a DS3 AIS. A one must also be written (if not already written) into bit 0 (XTX) in this register location in order to satisfy the definition of DS3 AIS.
	5	ENAIS	**Enable Transmit DS3 Alarm Indication Signal Automatically:** A one written into this bit position causes the DS3F to transmit DS3 AIS when the RXOOF bit (Register 00, bit 6) is set to 1.
	4	TXIDL*	**Transmit DS3 Idle Signal:** A one written into this bit position causes the DS3F to transmit a DS3 idle signal. A one must also be written (if not already written) into bit 0 (XTX) in this register location, in order to satisfy the definition of DS3 idle.
	3	M13MODE	**M13 Operating Mode:** A one enables the DS3F to operate in the M13 mode as specified in Bellcore TR-TSY-000009, and the ANSI T1.107-1988 standard. The M13 operating mode is only operational when the terminal side is a serial interface. A zero enables the DS3F to operate in the C-bit parity mode that is specified in the ANSI T1.107-1988 T1X1/89-034R2 draft supplement. The C-bit operating mode is operational for either a terminal side serial or parallel interface.

*Note: If both TXAIS and TXIDL are set, TXAIS takes precedence.

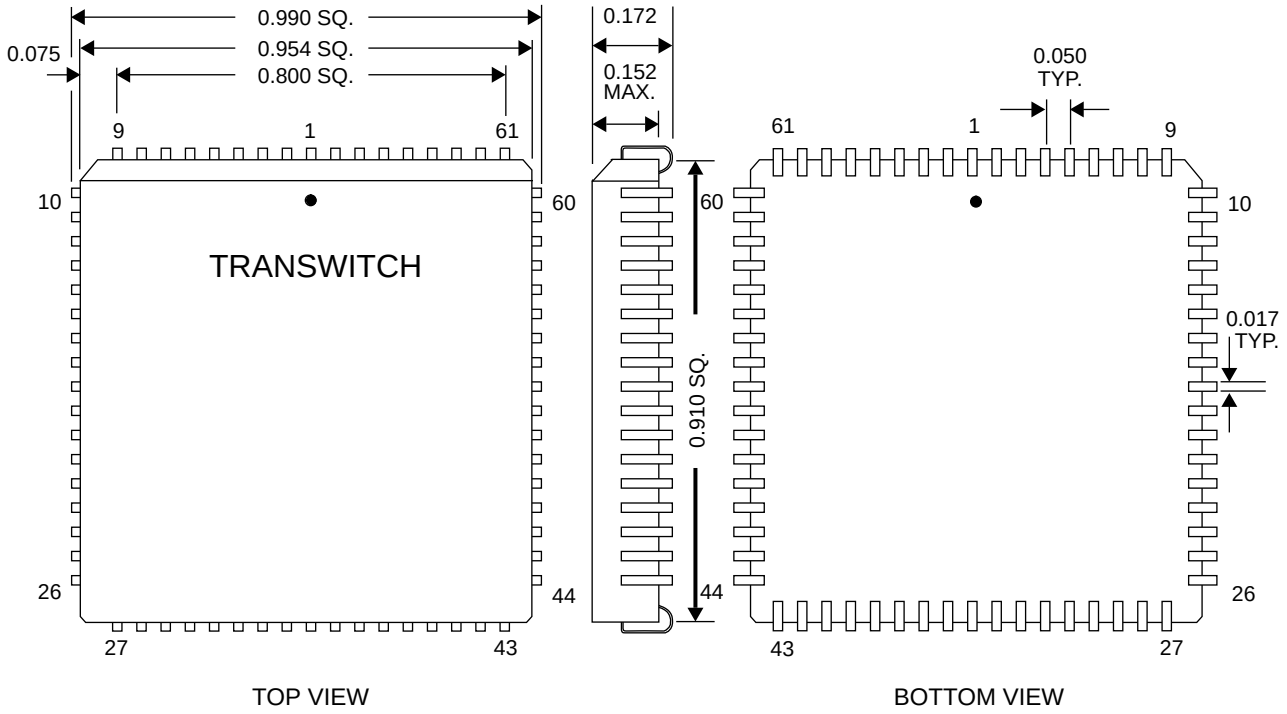
Address	Bit	Symbol	Description
01	2	SER	**Serial Interface Terminal Side:** A one configures the DS3F terminal side to be a serial interface for both receive and transmit. A zero configures the terminal side to be a nibble interface. The serial interface is operational in either the M13 or C-bit parity mode. In the M13 operating mode, the transmit C-bit interface is disabled and terminal side C-bits are transmitted as user data. The nibble interface is operational for the C-bit parity mode only.
	1	3LOOP	**DS3 Transmit-to-Receive Loopback:** A one written into this bit position disables the receive input and causes the transmit output to be looped back as receive data. Transmit data is provided at the output (D3TD).
	0	XTX	**Transmit X-Bits:** The X-bits may be used to transmit a yellow alarm or as a low-speed signaling channel. A one written into this bit position causes the DS3F to transmit a one for both X1 and X2.
02	7-0	FBn	**FEBE / Framing Bit Error Performance Counter:** This is a read-only 8-bit saturating counter that stops at a count of 255 and is automatically cleared to zero when it is read by the microprocessor. The integrity of the count is partially protected when the microprocessor reads the counter or the DS3F is in process of incrementing the counter. If an incoming count indication is received during one of these times, the indication is held and the counter is incremented once after completion of the read or increment cycle (i.e., any multiple indications received are recorded as a single increment). When the DS3F is operating in the C-bit parity mode, this counter counts the FEBE indications received. A FEBE indication occurs for a received DS3 frame if any one or more of the C10, C11, or C12 bits in the frame is zero. When the DS3F is operating in the M13 mode, this counter counts framing bit error indications. An error indication occurs for each F-bit in a received DS3 frame that has a value different from the expected framing pattern. For each such indication, the DS3F also provides a FEBE indication in the transmit line output, unless control bit NOFEBE is 1. In the M13 mode, the counter is frozen during a DS3 loss of signal or an out of frame condition.

Address	Bit	Symbol	Description
03	7-0	CPn	**C-Bit Parity Error Performance / Number of Frames Counter:** This is a read-only 8-bit saturating counter that stops at a count of 255 and is automatically cleared to zero when it is read by the microprocessor. The integrity of the count is partially protected when the microprocessor reads the counter or the DS3F is in process of incrementing the counter. If an incoming count indication is received during one of these times, the indication is held and the counter is incremented once after completion of the read or increment cycle (i.e., any multiple indications received are recorded as a single increment). When the DS3F is operating in the C-bit parity mode, this counter counts C-bit parity error indications. An error indication occurs for each received DS3 frame in which the majority (i.e., two or more) of the C7, C8 and C9 parity bits differ from the parity bit which was calculated by the DS3F over all 4704 received payload data bits of the preceding frame. For each such indication, the DS3F also provides a FEBE indication in the transmit line output, unless control bit NOFEBE is 1. When the DS3F is operating in the M13 mode, this counter counts DS3 frames. It takes approximately 27 milliseconds to count 255 frames. The application's software may use this DS3 frame count in conjunction with the count contained in the framing bit error counter (Address 04H) to determine an approximate bit error rate (BER). In the M13 mode, the counter is frozen during a DS3 loss of signal or an out of frame condition.
04	7-0	PPn	**P-Bit Parity Error Performance Counter:** This is a read-only 8-bit saturating counter that stops at a count of 255 and is automatically cleared to zero when it is read by the microprocessor. The integrity of the count is partially protected when the microprocessor reads the counter or the DS3F is in process of incrementing the counter. If an incoming count indication is received during one of these times, the indication is held and the counter is incremented once after completion of the read or increment cycle (i.e., any multiple indications received are recorded as a single increment). This counter counts P-bit parity error indications in either C-bit parity or M13 operating mode. An error indication occurs for each received DS3 frame during which one or both of the P1 and P2 bits differ from the parity bit calculated by the DS3F over all 4704 received payload data bits of the preceding DS3 frame. The DS3F does not provide a FEBE indication in the transmit line output for each such indication. The counter is frozen during a DS3 loss of signal or an out of frame condition.

Address	Bit	Symbol	Description
05	7	TEST	**TEST FEAC:** This bit is used by TranSwitch for FEAC testing purposes, and it must be written with a 0.
	6	START	**Start FEAC Message:** When START is set to 1, the DS3F starts to send repetitively the 16-bit FEAC code word, including the XXXXXX bits in bit positions 5-0, using the third C-bit (C3). If START is 0, then the third C-bit is always zero and the FEAC channel is disabled.
	5-0	FEAC Transmit Data	**Transmit FEAC Message:** The third C-bit (C3) is used as a far end alarm and control (FEAC) channel. The FEAC channel uses a 16-bit code word that has the form 0XXXXXX0 11111111 to convey information, where the XXXXXX bits are the FEAC message. Bit 0 corresponds to the right-most bit in the FEAC message. The FEAC word is inserted for the X's and the DS3F inserts the necessary 0's and trailing 1's to complete the 16-bit word. Specific words that are transmitted for alarm or status conditions must be sent for the duration of the condition or a minimum of 10 code repetitions. When the FEAC channel is used for control purposes, the two-word control codes are repeated 10 times. For example, to activate or deactivate a loopback, the first loopback control code word must be transmitted 10 times, followed by 10 repetitions of the second DS3 (or DS1) line code word. The controlling software must set the duration of the FEAC message by setting to 1, and clearing to 0, bit 6 of this register (START).
06	6	NEW	**New Received FEAC Message:** The DS3F sets NEW to 1 when it receives a FEAC message (following a series of 1's) for five consecutive FEAC message intervals (5 x 16 = 80 frames). NEW is reset to zero when register 06 is read.
	5-0	FEAC Receive Data	**Receive FEAC Message:** The received code word (in the C3 FEAC channel bit) must be repeated at least five times before it is inserted in bits 5-0. The most significant bit position is located in bit 0.
07	7-0	RXLOS RXOOF RXAIS RXIDL CERR LOC X2ERR X1ERR	**Latched-Bit Register:** Bits 7-4 in this location are the latched values of the corresponding bits in location 00H. All of the bits in this register latch and are cleared on a read cycle, but RXAIS maintains its value when the DS3F is in TR loopback or no TX terminal input is present. Bit 3 (CERR) latches when the DS3F receives a C1 bit equal to zero. Bit 2 (LOC) latches when either an RXLOC (bit 3 - 00H) or an TXLOC (bit 2 - 00H) occurs. The X2ERR and X1ERR bits (bits 1 and 0) are latched at the inverse of the XRX2 and XRX1 values (normally 1), so they are normally 0, and a value of 1 indicates an error in the corresponding received X-bit.

PACKAGE INFORMATION

The DS3F device is packaged in a 68-pin plastic leaded chip carrier (PLCC) suitable for socket or surface mounting, as shown in Figure 18.



Note: All dimensions are shown in inches and are nominal unless otherwise indicated.

Figure 18. DS3F TXC-03401 68-Pin Plastic Leaded Chip Carrier

ORDERING INFORMATION

Part Number: TXC-03401-AIPL	68-pin plastic leaded chip carrier

RELATED PRODUCTS

TXC-02020 (02021), ART (ARTE) VLSI Device (Advanced DS3/STS-1 Receiver/Transmitter). Performs the receive and transmit line interface functions required for transmission of DS3 (44.736 Mbit/s) or STS-1 (51.840 Mbit/s) signals across a coaxial interface. The ARTE is an extended-feature version of the ART, in a larger package.

TXC-03301, M13 VLSI Device (DS3/DS1 Mux/Demux). This single-chip multiplex/demultiplex device provides the complete interfacing function between a single DS3 signal and 28 independent DS1 signals.

TXC-03303, M13E VLSI Device. Extended feature version of the TXC-03301 (M13).

TXC-05101C, HDLC VLSI Device (HDLC Controller). Provides an interface to packet. Performs flag generation/detection, zero insertion/deletion, abort detection and byte framing.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator Receiver). Programmable multi-rate test pattern generator and receiver in a single chip with serial, nibble, or byte interface capability.

TXC-20153D, DS3/STS-1 Line Interface Module (DS3LIM-SN). Complete and compact analog to digital interface serving B3ZS encoded DS3 signals.

TXC-21005, DS3F/XBERT Evaluation Board. A complete, ready-to-use test system that demonstrates the functions and features of the DS3F VLSI device. Includes on-board microprocessor, RS-232 interface, XBERT, and MS-DOS compatible PC software for control and monitor.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

IEEE (U.S.A.)

The Institute of Electrical and Electronics Engineers, Inc.
Customer Service Department
445 Hoes Lane
P. O. Box 1331
Piscataway, NJ 08855-1331
Tel: 800-701-4333 (In U.S.A.)
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LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated DS3F Data Sheet that have technical differences relative to the previous and now superseded DS3F Data Sheet:

Updated DS3F Data Sheet:	Edition 8, July 1995
Superseded DS3F Data Sheet:	Edition 7, June 1993

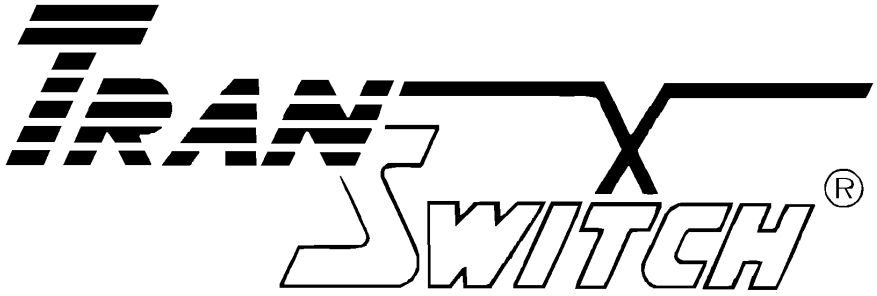
The page numbers indicated below of this updated data sheet include changes relative to the superseded data sheet.

Page Number of Updated Data Sheet	Summary of the Change
1	Added the last item to the Feature list and modified the Description.
1	Changed edition number and date.
2-39	Added edition number and date.
2	Added Table of Contents and List of Figures.
3	Modified Figure 1.
3-4	Made changes to Block Diagram Description.
5	Added TXC Product Number to Figure 2.
6	Added a note to the bottom to explain Type column heading.
7	Changed Type column for $\overline{\text{XFSI}}$ (Pin 50) and Name/Function column for XCK (Pin 62).
8	Made changes to Name/Function column for TDOUT (Pin 45) and CRDCC (pin 30).
9	Made changes to Name/Function column for CRCK (Pin 36), CRD (pin 37) and X1 (Pin 11).
10	Made changes to Name/Function column for STUFD (pin 15), FE (Pin 43) and $\overline{\text{TFIN}}$ (pin 49).
11	Changed “processor” to “microprocessor” in Name/Function column for $\overline{\text{SEL}}$ (Pin 8), ALE (Pin 10), $\overline{\text{RD}}$ (Pin 12) and $\overline{\text{WR}}$ (Pin 14).
12	Changed Min column on T_S and Max column on P_{DD}.
13	Deleted “Input Parameters For TTLd” table.
14	Made changes to Test Conditions column for V_{OH} and V_{OL} rows of the tables.

Page Number of Updated Data Sheet	Summary of the Change
15	Modified voltage level formula specified for timing parameter measurements.
16	Changed RNC to RCN and $\overline{RNF}$ to $\overline{RFN}$.
17	Modified Figure 6 and the corresponding table.
18	Changed RSD to RDS and RSC to RCS.
18	Changed Typ column on t_{CYC}.
19	Modified Figure 8 and the corresponding table.
21	Modified Figure 10 and the corresponding table.
22	Modified Figure 11 and the corresponding table.
23	Modified Figure 13.
24	Modified the note.
25	Modified Figure 15, the corresponding table and the notes.
26	Modified Figure 16, the corresponding table and the notes.
27	Added Power, Ground and External Components and Throughput Delays sections.
28	Modified Address 00H, Bit 2, Addresses 02H, 03H and 04H, and Note in Memory Map section.
28-29	Made changes to Description column for Bits 7-3 of Address 00 and Symbol column for Bit 2.
30	Made changes to Description column for Bit 1 of Address 01 (3LOOP).
30-32	Changed Addresses 02 through 07.
33	Made changes to Package Information section.
34	Modified Related Products section.
35	Added Standards Documentation Sources.
36-37	Added List of Data Sheet Changes.
41	Added Documentation Update Registration Form.

- NOTES -

- NOTES -



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