DS3LIM-SN
DS3/STS-1 Line Interface Module
NRZ Clock/Data Output
TXC-20153D, TXC-20153G

DATA SHEET

FEATURES

- Complete B3ZS analog to NRZ digital DS3/ STS-1 line interface unit in a compact 2.6 square inch, 50-pin DIP Module
- Single +5V power supply
- Analog inputs and outputs are transformer coupled
- Meets DSX cross connect frame mask requirements (ANSI Standard T1.102-1993)
- Adaptive equalization for zero to 900 feet of cable
- Input dynamic range of 20 dB (100mV - 0.95V)
- Meets DS3/STS-1 jitter requirements of Bellcore Technical References
- Full loopback capability
- Coding violation and loss of signal detection for received signal
- TXC-20153D has monitor pin for received signal input. TXC-20153G has pull-up for external clock input and improved performance margins.
- Speeds time to market for prototype development
- Eases parts inventory and acquisition
- Eases field maintenance

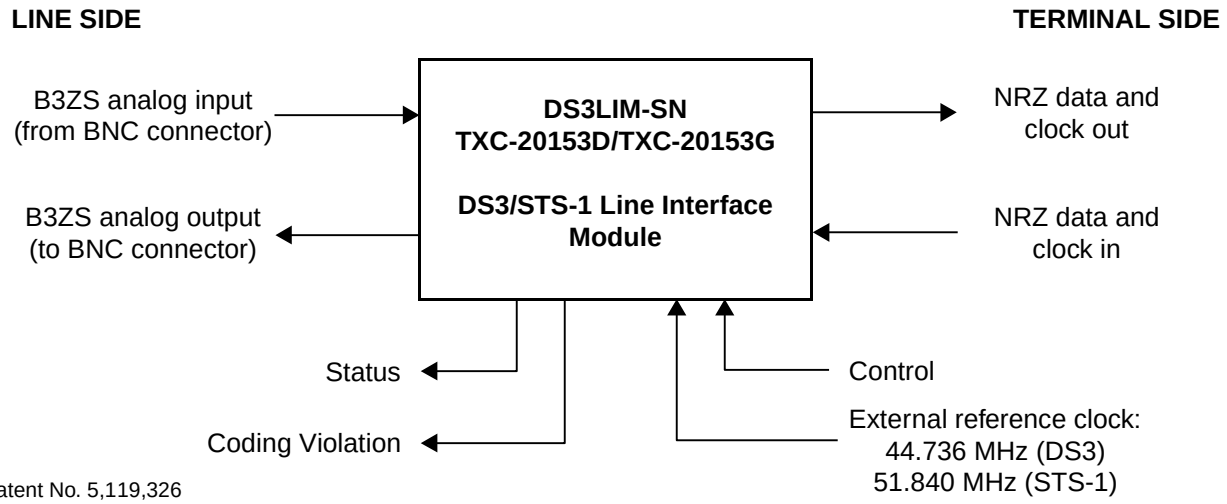
DESCRIPTION

The DS3/STS-1 Line Interface Module (DS3LIM-SN) is a complete and compact full duplex analog line to digital terminal interface. It converts B3ZS-encoded line signals, in either DS3 asynchronous or STS-1 synchronous format, to and from NRZ data and clock signals. In addition to the synchronous signal option, this Module offers other improvements relative to the TranSwitch DS3 Line Interface Module (DS3LIM, TXC-20049D), which it can replace in some existing DS3 applications.

Sensitive analog circuitry meets DS3/STS-1 performance requirements for signal recovery and transmission, with direct line connection via on-board transformers. Integration of functions into a single Module frees the user from complex printed circuit board design and testing for the DS3/STS-1 analog section, reducing the time required for applications development and product introduction.

APPLICATIONS

- DS3/STS-1 interface for quick “time to market” products



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* Please note that TranSwitch provides documentation for all of its products. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

LIST OF FIGURES

PRODUCT OVERVIEW

The DS3LIM-SN Module employs TranSwitch's latest DS3/STS-1 receiver/transmitter VLSI device on a small printed circuit board assembly with line-coupling transformers and dual-port terminal interface circuits. Use of the TranSwitch ART VLSI device (Advanced DS3/STS-1 Receiver/Transmitter, TXC-02020) provides improved performance and reduced cost relative to the TranSwitch DS3LIM Module, which is based on the DS3-only DS3RT receiver/transmitter VLSI device. In addition to the STS-1 synchronous capability, the ART device has on-board AGC, equalization and output amplification, functions which had to be provided with external components on the DS3LIM.

The DS3LIM-SN is mechanically compatible with the DS3LIM and is intended to supersede it for both existing and new applications. The reduced cost and improved performance (wider dynamic range, simultaneous loopback capability) are advantages for existing applications, providing that certain constraints imposed by electrical differences from the DS3LIM can be accommodated (see the section below entitled "Functional Differences between DS3LIM-SN and DS3LIM Modules"). For new applications the STS-1 capability and single power supply are additional advantages.

Three versions of the DS3LIM-SN Module are available, with two different product numbers and part numbers (please see the Ordering Information section). The TXC-20153D product is the original version. It provides a pin (MON, pin 46) for monitoring the received signal input at the 75 ohm terminating resistor on the secondary side of the input transformer. Since this pin has electrical characteristics different from those of the corresponding pin on the DS3LIM Module, the TXC-20153D may not be suitable for substitution in DS3LIM applications where this pin is not used for monitoring but has a termination that takes advantage of the superior DS3LIM output characteristics. The TXC-20153G product was introduced for use in such applications. The first version of the TXC-20153G (Edition 1) has two layout differences relative to the TXC-20153D: it has no monitor output connection to pin 46, and it has a pull-up resistor on the external clock input (DCK, pin 27). However, this Edition 1 is less immune to noise than the TXC-20153D. In applications where excessive board noise is present, and when receiving a signal greater than 800 mV peak, bit errors may occur. Edition 2 of the TXC-20153G was introduced for use in such applications. It is identical to Edition 1, except for a modification to the receive input circuit that provides 4 dB attenuation of the input signal at the input to the ART device.

BLOCK DIAGRAM

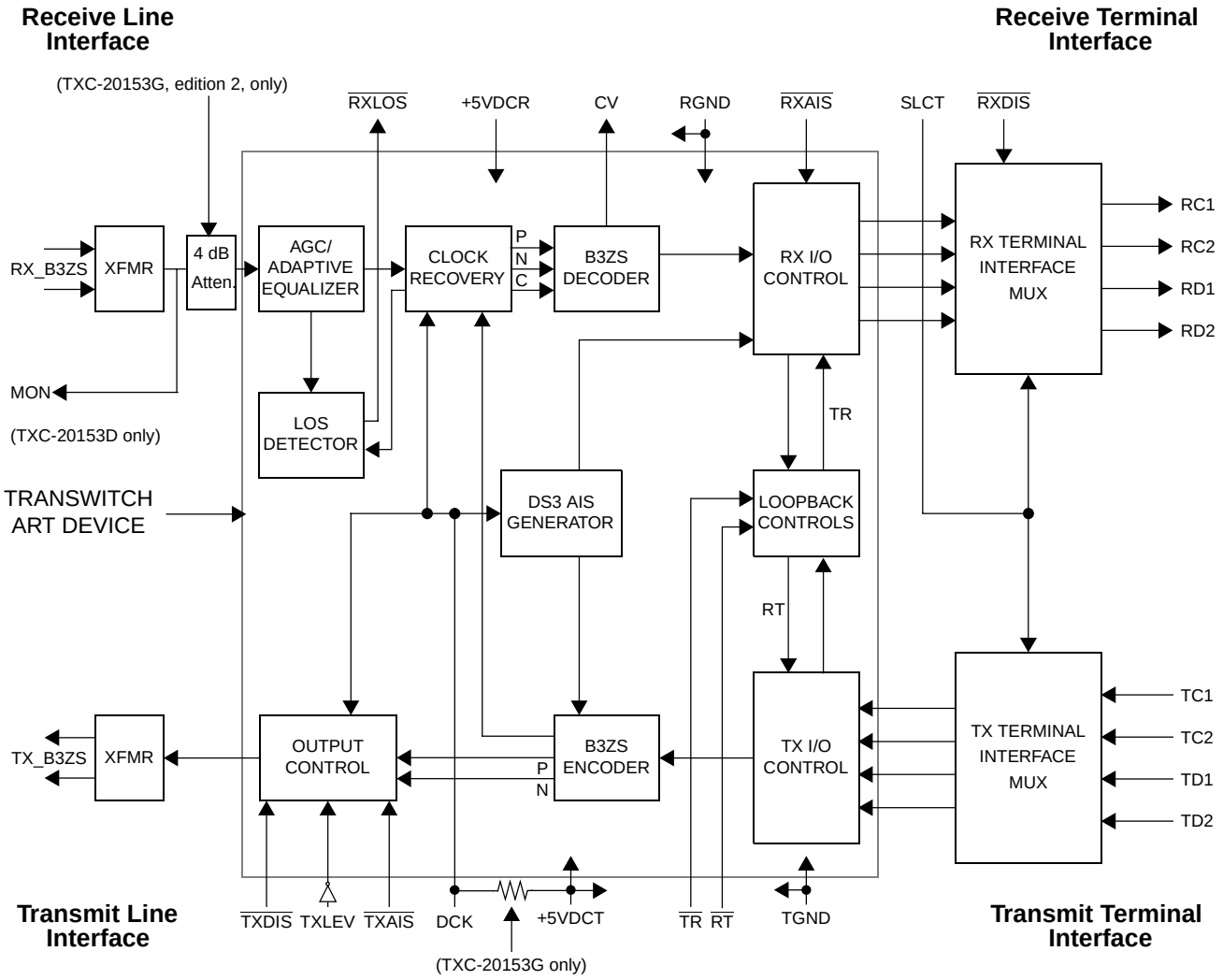


Figure 1. DS3LIM-SN Block Diagram

BLOCK DIAGRAM DESCRIPTION

A block diagram for the DS3LIM-SN Module is shown in Figure 1, which is explained below.

In the receive direction, the DS3LIM-SN receives a bipolar B3ZS-encoded DS3 or STS-1 signal from the line via a BNC or other connector. This signal (RX_B3ZS) is AC-coupled into the DS3LIM-SN through a 1:1 transformer (XFMR). From the transformer, the signal is terminated into a 75 ohm resistance, either as a single 75 ohm shunt resistor or as a 27/47 ohm resistor pair that provides 4 dB attenuation at its junction (in TXC-20153G Edition 2 only). The resulting signal is then routed to the input of an Automatic Gain Control (AGC) circuit in the ART device (dotted outline). A Monitor pin (MON) is provided for observing the received signal in the TXC-20153D only. The AGC provides the Adaptive Equalizer circuit with a constant signal level. The equalizer is switched in and out to recover narrow or wide width DS3/STS-1 signals, respectively. From the equalizer, the bipolar signal is connected to the LOS Detector and Clock Recovery blocks. The line signal is monitored for transitions, and a loss of signal indication is provided on the signal pin labelled $\overline{\text{RXLOS}}$.

The Clock Recovery block requires an external 44.736 MHz (DS3) or 51.840 MHz (STS-1) clock (DCK) with a stability of ± 200 ppm. The stability of DCK must be increased to ± 20 ppm if the transmit or receive AIS features are used. The average time to recover the clock is approximately 1 ms when the line signal is applied.

The B3ZS (bipolar with 3-zero substitution) line coded data is decoded by the B3ZS Decoder block. Indications of coding violation errors, other than normal B3ZS coding substitutions, are provided on the signal pin CV. The decoder detects coding violation errors in the same fashion as the Telecommunication Techniques Corporation's TBERD™ model 305 DS3 Analyzer for system test purposes, but some differences may be encountered when testing with Scientific Atlanta or Wandel and Goltermann equipment. These errors can occur because of noise and other impairments on the line. The application that uses the DS3LIM-SN can count the CV pulses over a known time interval to calculate a close estimate for the Bit Error Rate (BER) performance of the line.

The DS3LIM-SN provides the capability to generate and insert a DS3 Alarm Indication Signal (AIS) into the NRZ receive data signal at the RD1 or RD2 pins. A low placed on the $\overline{\text{RXAIS}}$ pin enables the DS3 AIS insertion from the DS3 AIS Generator block. This pin may be connected to the receive loss of signal ($\overline{\text{RXLOS}}$) pin to generate AIS. The DS3LIM-SN does not provide a corresponding capability for STS-1 operation.

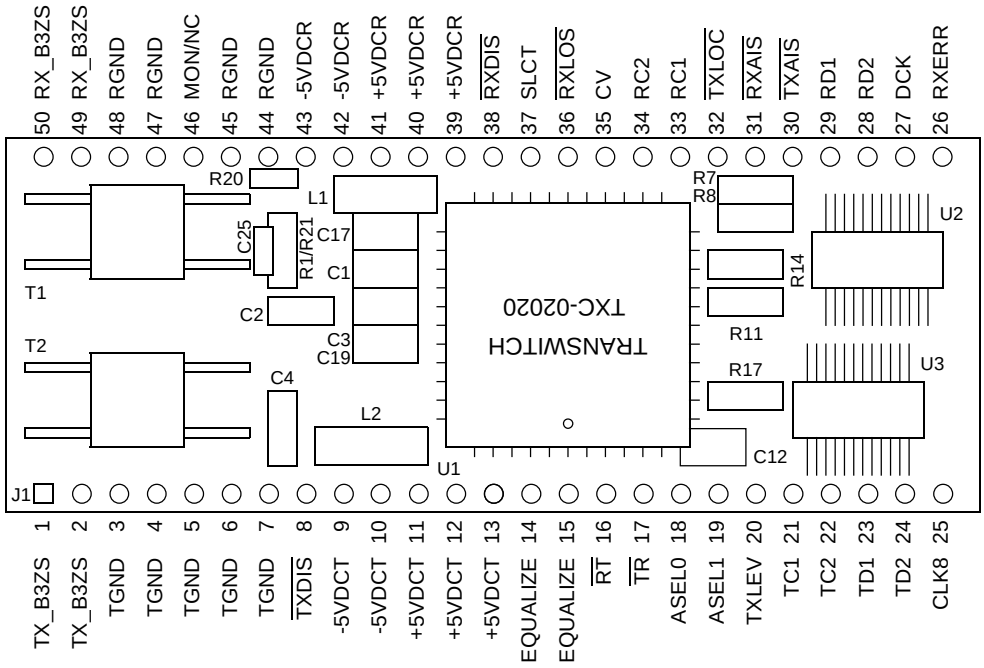
The decoded signal is processed by the Receive I/O Control and Receive Terminal Interface Multiplexer blocks. Two receive output ports consisting of a clock and data signal are provided. The first receive output port has pins labelled RC1 and RD1; the second is labelled RC2 and RD2. Only one port can be active at a time. Data (RD1/RD2) is clocked out of the DS3LIM-SN with respect to the falling edge of the receive clock (RC1/RC2). The selection of the receive output port is controlled by the state of the select pin (SLCT, high for port 1). The unused port is forced into a high impedance state. In addition, the two receive ports can both be disabled and forced into a high impedance state by placing a low on the $\overline{\text{RXDIS}}$ pin.

In the transmit direction, two transmit ports consisting of clock and data are also provided. The first transmit port has pins labelled TC1 and TD1; the second is labelled TC2 and TD2. Transmit input data (TD1/TD2) is clocked into the DS3LIM-SN on positive transitions of the clock signal (TC1/TC2). As in the receiver section, the SLCT pin determines the transmit input port selection (high for port 1).

The transmit input clock and data signals are processed by the Transmit Terminal Interface Multiplexer and Transmit I/O Control blocks. The incoming data is encoded by the B3ZS encoder. In the B3ZS line code, each block of three consecutive zeros is removed and replaced by either of two codes that contain bipolar violations. These replacement codes are B0V and 00V, where B represents a pulse that conforms to the bipolar rule and V represents a pulse violating the rule. The choice of these codes is made so that an odd number of bipolar conforming pulses (B) is transmitted between consecutive bipolar violation pulses (V). The encoded data is connected to the Output Control block, which contains the formatting circuitry to transform the B3ZS-encoded data into pulses that meet the requirements for the DS3 or STS-1 line rates and a 75-ohm driver for the 1:1 output transformer. This block also provides the capability to transmit a DS3 Alarm Indication Signal (AIS), which is independent of the transmit data. A low placed on the $\overline{\text{TXAIS}}$ pin enables the transmit DS3 AIS insertion. A low placed on the $\overline{\text{TXDIS}}$ pin deactivates the transmit output. When $\overline{\text{TXDIS}}$ is set low, the output impedance of the TX_B3ZS port becomes a high impedance state. The Output Control block contains a feature to adjust the output signal for cables longer than 50 feet, which is activated by setting the TXLEV pin low.

In addition to the alarms and control signals, the DS3LIM-SN provides two loopback capabilities for testing transmit and receive loopback via the Loopback Controls block. Transmit-to-Receive (terminal) loopback connects the data path from the Transmit I/O Control block output to the Receive I/O Control block input, and disables the external receiver input. Transmit-to-Receive loopback is activated by placing a low on the $\overline{\text{TR}}$ signal pin. Receive-to-Transmit (line) loopback connects the receive data output path to the transmit input circuits and disables the NRZ transmit input. Receive-to-Transmit loopback is activated by placing a low on the $\overline{\text{RT}}$ pin. Terminal and line loopbacks may be applied together, or at the same time as DS3 AIS insertion into the receive or transmit data output signals, as described under the heading "AIS and Loopback Control Signal Arbitration" in the Operation section of this Data Sheet.

PIN DIAGRAM



Note: Some pins do not perform the functions suggested by their labels, as explained in the Pin Descriptions section.

Figure 2. DS3LIM-SN Pin Diagram

PIN DESCRIPTIONS

Symbol *	Pin No.	I/O/P **	Type ***	Name/Function
TX_B3ZS	1, 2	O	Analog	**Transmit DS3/STS-1 B3ZS Output:** These pins are AC-coupled, B3ZS-encoded DS3 or STS-1 output signals. They may be applied directly to a 75Ω BNC connector. It is recommended that pin 2 should be connected to the center pin and pin 1 to the shield of the BNC connector. Under normal operation, this output has a 75Ω source impedance. When $\overline{\text{TXDIS}}$ is low, this output is placed into a high-impedance disabled condition.
TGND	3, 4, 5, 6, 7	P		**Transmit Ground:** Ground pin for transmit side circuitry.
$\overline{\text{TXDIS}}$	8	I	TTLp	**Transmit Disable:** An active low on this pin disables the DS3 or STS-1 transmitted signal. An external 10kΩ pull-up resistor to +5V is required to enable transmission.
-5VDCT	9, 10	P		**Unused:** These pins are not connected within the Module, which does not require a -5V power supply. They may be connected to the -5V power supply in applications originally designed to use the DS3LIM Module. Otherwise they must be left floating.

* **Note: Symbols used here are the same as for the DS3LIM Module, although there are some pins for which the function is different or absent in the DS3LIM-SN, as indicated under Name/Function.**

** Note: I=Input; O=Output; P=Power

*** Note: See the Input and Output Parameters section below for digital input and output Type definitions.

Symbol	Pin No.	I/O/P	Type	Name/Function
+5VDCT	11, 12, 13	P		**Transmit +5VDC:** +5V, ±5% DC power supply for transmit side circuitry.
EQUALIZE	14, 15	--	--	**Unused:** These pins are not connected within the Module, which does not require a strap for short cable equalization. They may be left open or joined together for applications originally designed to use the DS3LIM Module.
$\overline{RT}$	16	I	TTLp	**Receive-To-Transmit Loopback:** An active low enables the receive (line) loopback feature. This loopback connects the receive terminal NRZ data and clock outputs to the transmit terminal NRZ data and clock inputs, and disables the NRZ transmit inputs. (See Note 1)
$\overline{TR}$	17	I	TTLp	**Transmit-To-Receive Loopback:** An active low enables the transmit (terminal) loopback feature. This loopback connects the B3ZS transmit line outputs to the B3ZS receive line inputs, and disables the DS3/STS-1 receive line signal input. (See Note 1)
ASEL0 ASEL1	18 19	-- --	-- --	**Unused:** These pins are not connected within the Module, which does not require amplifier gain select bias. Each may be connected to +5V by a 10kΩ resistor in applications originally designed to use the DS3LIM Module. Otherwise they must be left floating.
TXLEV	20	I	TTL	**Transmit Level:** This pin alters the shape of the transmitted pulse to meet ANSI T1.102 pulse mask requirements at the DSX with different cable lengths. The pin must be pulled high (with a 10kΩ resistor to +5V) for cables shorter than 50 feet and must be set low for cables between 50 and 450 feet long. For applications originally designed to use the DS3LIM Module to meet ANSI mask requirements with 0-450 feet of cable this pin is tied low, and the DS3LIM-SN may not operate correctly with short cables. The transmit output mode is indeterminate if TXLEV is left floating.
TC1	21	I	TTLr	**Transmit Input Clock #1:** When a high is placed on the SLCT lead, TC1 is the input pin for the NRZ transmit clock. This clock has a 50% ± 5% duty cycle.
TC2	22	I	TTLr	**Transmit Input Clock #2:** When a low is placed on the SLCT lead, TC2 is the input pin for the NRZ transmit clock. This clock has a 50% ± 5% duty cycle.
TD1	23	I	TTL	**DS3/STS-1 Transmit Input Data Port 1:** Data is clocked in on positive transitions of TC1. This port is enabled by placing a high on the SLCT lead.

Note 1: An external 10kΩ pull-up resistor to +5V is required to disable loopback. Setting $\overline{RT}$ and $\overline{TR}$ low simultaneously will enable both line and terminal side loopbacks (see Operation section for additional information on AIS and loopback control signal arbitration).

Symbol	Pin No.	I/O/P	Type	Name/Function
TD2	24	I	TTL	**DS3/STS-1 Transmit Input Data Port 2:** Data is clocked in on positive transitions of TC2. This port is enabled by placing a low on the SLCT lead.
CLK8	25	--	--	**Unused:** This pin is not connected within the Module, which does not require an 8 kHz clock input as a time base for bit error rate measurement. The pin may have this clock connected in applications originally designed to use the DS3LIM Module. Otherwise it must be left floating.
RXERR	26	O	Tied low	**Unused:** This pin is tied low within the Module to simulate a low receive bit error rate indication for applications originally designed to use the DS3LIM Module, in which this pin goes high to indicate a high error rate. This pin should otherwise be left floating, since the DS3LIM-SN does not indicate error rate.
DCK	27	I	CMOS	**External Clock**: An external 44.736 MHz (DS3) or 51.840 MHz (STS-1) clock having a stability of ± 200 ppm (± 20 ppm if the AIS feature is used), and a duty cycle of 50% ± 5%. If the duty cycle is relaxed, the transmitted mask may not meet pulse mask requirements. (See Note 4.)
RD2	28	O	TTL4mA	**DS3/STS-1 Receive Output Data Port 2:** Data is clocked out on negative transitions of RC2 (see Note 1). This port is enabled by placing a low on the SLCT lead. When this port is disabled, by placing a high on SLCT or a low on the $\overline{\text{RXDIS}}$ control lead, the output goes to a high impedance state.
RD1	29	O	TTL4mA	**DS3/STS-1 Receive Output Data Port 1:** Data is clocked out on negative transitions of RC1 (see Note 1). This port is enabled by placing a high on the SLCT lead. When this port is disabled, by placing a low on SLCT or a low on the $\overline{\text{RXDIS}}$ control lead, the output goes to a high impedance state.
$\overline{\text{TXAIS}}$	30	I	TTLp	**Transmit AIS:** An active low placed on this pin disables the transmit data input, and causes a DS3 alarm indication signal to be generated and sent as transmitted data on the TX_B3ZS output when the Module is operating with DS3 signals. (See Notes 2 and 3.)

Note 1: Data is also clocked out on negative clock transitions in the DS3LIM Module. The Edition 3 Data Sheet for this Module incorrectly specifies positive transitions in the pin description.

Note 2: An external 10kΩ pull-up resistor to +5V is required to enable data and disable the AIS.

Note 3: DS3 AIS is defined as a valid M-frame with proper subframe structure. The data payload is a 1010 ... sequence starting with a 1 after each overhead bit. Overhead bits are as follows: F0=0, F1=1, M0=0, M1=1; C-bits are set to 0; X-bits are set to 1; and P-bits are set for valid parity.

Note 4: In the TXC-20153G Module, the DCK input is connected to the Transmit +5VDC supply line via a 10 kΩ pull-up resistor and its input current characteristics are modified accordingly.

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{RXAIS}}$	31	I	TTLp	**Receive AIS:** An active low placed on this pin disables the receive data, input, and causes a DS3 alarm indication signal to be generated and sent on the RD1 or RD2 output pins when the Module is operating with DS3 signals. (See Notes 2 and 3)
$\overline{\text{TXLOC}}$	32	O	Pulled high	**Unused:** This pin is pulled high within the Module to simulate an error-free indication for applications originally designed to use the DS3LIM Module, in which this pin goes low to indicate that the transmit input clock (TC1, TC2) is stuck high or low. This pin should otherwise be left floating, since the DS3LIM-SN does not indicate loss of clock.
RC1	33	O	CMOS8mA	**DS3/STS-1 Receive Output Clock Port 1:** This port is enabled by placing a high on the SLCT lead. When this port is disabled by placing a low on SLCT or a low on the $\overline{\text{RXDIS}}$ control lead, the output goes to a high impedance state.
RC2	34	O	CMOS8mA	**DS3/STS-1 Receive Output Clock Port 2:** This port is enabled by placing a low on the SLCT lead. When this port is disabled by placing a high on SLCT or a low on the $\overline{\text{RXDIS}}$ control lead, the output goes to a high impedance state.
CV	35	O	CMOS	**Coding Violation:** A positive pulse having a duration of one clock cycle is provided on this pin whenever a B3ZS coding violation occurs.
$\overline{\text{RXLOS}}$	36	O	CMOS	**Receive Loss of Signal:** An active low alarm is generated when 175 ± 75 consecutive zeros appear in the incoming data stream. It is cleared when ones pulse density is in the range of 28% to 33% (or more than 33%) for 175 ± 75 consecutive pulses.
SLCT	37	I	CMOSr	**Select Port 1 or 2:** The ports are enabled and disabled according to the following table:

Select	High	Low
RD1	Enabled	High Z
RC1	Enabled	High Z
TD1	Enabled	Disabled
TC1	Enabled	Disabled
RD2	High Z	Enabled
RC2	High Z	Enabled
TD2	Disabled	Enabled
TC2	Disabled	Enabled

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{RXDIS}}$	38	I	CMOSr	**Receive Disable Ports 1 and 2:** An active low placed on this pin disables port 1 (RD1 and RC1), and port 2 (RD2 and RC2). The data and clock output signal leads are forced to a high impedance state. An external 10kΩ pull-up resistor to +5V is required to enable port 1 and port 2.
+5VDCR	39, 40, 41	P		**Receive +5VDC:** +5V, ±5% DC power supply input for receive side circuitry.
-5VDCR	42, 43	P		**Unused:** These pins are not connected within the Module, which does not require a -5V power supply. They may be connected to the -5V power supply in applications originally designed to use the DS3LIM Module. Otherwise they must be left floating.
RGND	44, 45, 47, 48	P		**Receive Ground:** Ground pins for receive side circuitry.
MON/NC	46	O/-	Analog/-	**For TXC-20153D:** **DS3/STS-1 Received Signal Monitor Point:** This output is directly tied to the terminating resistor after transformer coupling. Care must be taken to ensure very short trace lengths to the MON buffer, or oscillation of the AGC may occur. If a monitor output is not required, it is suggested that this pin be left open. **For TXC-20153G (Edition 1 and Edition 2):** **No Connect:** This pin is not connected within the Module, which provides no capability to monitor the received input signal. This pin may be connected to an external termination in applications originally designed to use the DS3LIM Module, but it should otherwise be treated as a “No Connect” pin and should be left floating.
RX_B3ZS	49, 50	I	Analog	**Receive DS3/STS-1 B3ZS Input:** These pins are the AC-coupled B3ZS-encoded DS3 or STS-1 input signal. They may come directly from a 75Ω ohm BNC connector. If these signals originate from a BNC connector, it is recommended that the center pin should be connected to pin 50 and the shield to pin 49.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
+5V supply voltages	V_{DD}		+7.0	V	Note 1
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	Note 1
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient operating temperature	T_A	0	70	^oC	0 ft/min linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, in-circuit	RH	0	100	%	Non-condensing. Note 2.

Notes:
1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which the Modules are supplied.

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}			290	mA	V_{DD} = 5.25V
P_{DD}			1.5	W	V_{DD} = 5.25V

INPUT AND OUTPUT PARAMETERS

Input Parameters for CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	V_{DD} - (V_{DD} / 3)		V_{DD} + 0.3	V	
V_{IL}	- 0.3		(V_{DD} / 3)	V	
I_{IH}			- 10	µA	V_{DD} = 5.25V
I_{IL}			10	µA	V_{DD} = 5.25V
Input Capacitance			10	pF	

Input Parameters For CMOSr

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 ≤V_{DD} ≤ 5.25
V_{IL}			0.8	V	4.75 ≤V_{DD} ≤ 5.25
Input leakage current		50	120	µA	V_{DD} = 5.25
Input capacitance		5.5		pF	

Note: Input has a 100k (nominal) internal pull-up resistor.

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	4.75 ≤V_{DD} ≤ 5.25
V_{IL}			0.8	V	4.75 ≤V_{DD} ≤ 5.25
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		5.5		pF	

Input Parameters for TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		V_{DD} + 0.3	V	
V_{IL}	- 0.3		0.8	V	
I_{IH}			- 10	µA	V_{DD} = 5.25V
I_{IL}			550	µA	V_{DD} = 5.25V
Input Capacitance			10	pF	

Note: All TTLp inputs have an internal pull-up resistor.

Input Parameters For TTLr

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		50	120	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Note: Input has a 100k (nominal) internal pull-up resistor.

Output Parameters for CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	4 mA source
V_{OL}			0.5	V	4 mA sink
I_{OH}			- 4.0	mA	$V_{DD} = 4.75V$
I_{OL}			4.0	mA	$V_{DD} = 4.75V$
t_{RISE}	1.7	2.7	4.2	ns	$C_{LOAD} = 15$ pF
t_{FALL}	1.9	2.8	4.1	ns	$C_{LOAD} = 15$ pF

Output Parameters For CMOS8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -8.0$ mA
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 8.0$ mA
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}	1.3	2.4	3.8	ns	$C_{LOAD} = 25$ pF
t_{FALL}	1.1	1.8	2.5	ns	$C_{LOAD} = 25$ pF

Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	$V_{DD} = 4.75$; $I_{OH} = -4.0$ mA
V_{OL}			0.6	V	$V_{DD} = 4.75$; $I_{OL} = 4.0$ mA
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	2.8	6.5	9.2	ns	$C_{LOAD} = 15$ pF
t_{FALL}	1.3	2.3	3.4	ns	$C_{LOAD} = 15$ pF

Receiver Sensitivity

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	100		950	mVp	

Input Parameters For Transformer Coupling

Parameter	Min	Typ	Max	Unit	Test Conditions
Return Loss		- 26		dB	DS3: 22.368 MHz; 25^{o}C STS-1: 25.920 MHz; 25^{o}C
Isolation Voltage			300	Vrms	
Turns Ratio		1:1			
Input Impedance	67.5	75	82.5	ohms	

Output Parameters For Transformer Coupling

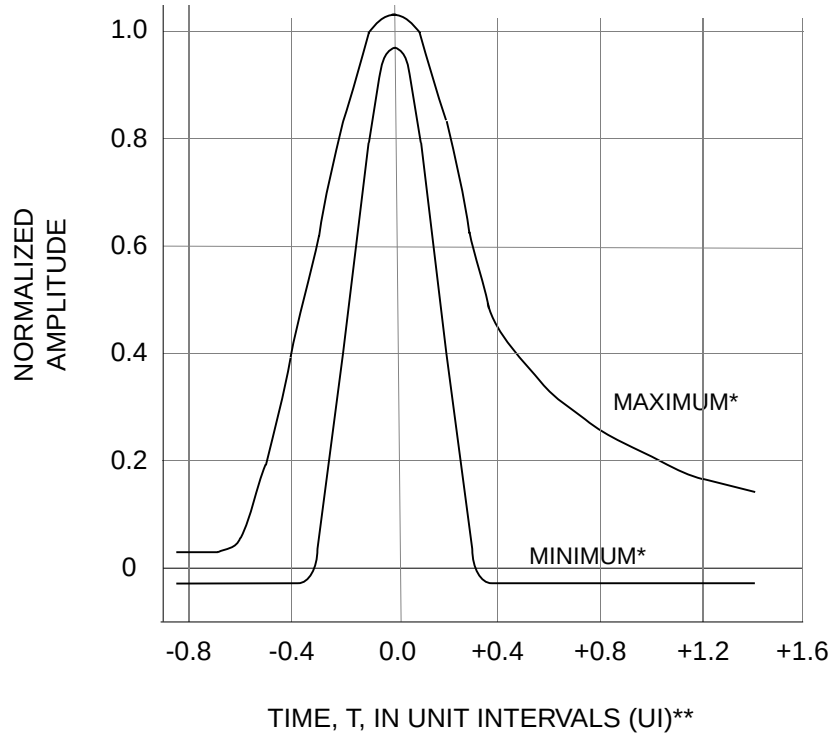
Parameter	Min	Typ	Max	Unit	Test Conditions
Isolation Voltage			300	Vrms	
Turns Ratio		1:1			
Output Impedance ($\overline{\text{TXDIS}}$ = 1)	67.5	75	82.5	ohms	
Output Impedance ($\overline{\text{TXDIS}}$ = 0)	100k	200k		ohms	

TIMING CHARACTERISTICS

Detailed timing diagrams for the DS3LIM-SN are illustrated in Figures 3 through 6. All output times are measured with the maximum load capacitance appropriate for the pin type. Timing parameters are measured at signal levels of $(V_{OH} + V_{OL})/2$ for outputs or $(V_{IH} + V_{IL})/2$ for inputs.

Line Side Timing Characteristics

The line side signal characteristics are designed so that the output meets the requirements of ANSI standard T1.102-1993. When terminated into a test load of 75Ω ± 5% using ATT 734A coaxial cable the DS3LIM-SN Module will meet the DS3 or STS-1 interface isolated pulse masks defined below in Figures 3a through 3c for a cable length of 0 to 450 feet. For STS-1 pulse sequences, the output also meets the STS-1 interface eye diagram mask shown in Figure 3d.



* Note: The DS3 curves shown are approximate representations of the equations in Figure 3b. The corresponding STS-1 curves (not shown) would be slightly different, as indicated by the equations in Figure 3c.

**Note: UI = 1 / (System Clock Frequency)

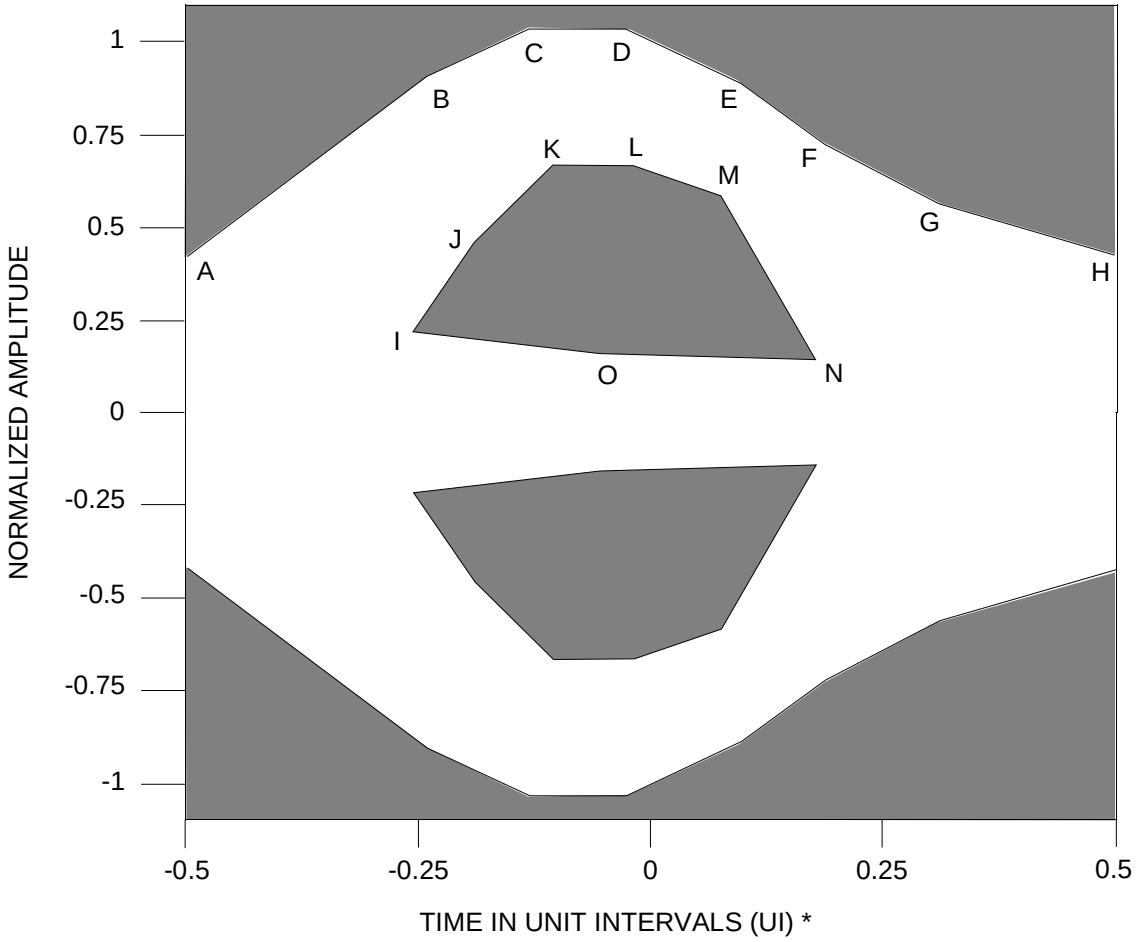
Figure 3a. DS3 Interface Isolated Pulse Mask

CURVE	TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
MAXIMUM (UPPER) CURVE	$-0.85 \leq T \leq -0.68$ $-0.68 \leq T \leq 0.36$ $0.36 \leq T \leq 1.4$	0.03 $0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.34}\right)\right]+0.03$ $0.08 + 0.407e^{-1.84(T-0.36)}$
MINIMUM (LOWER) CURVE	$-0.85 \leq T \leq -0.36$ $-0.36 \leq T \leq 0.36$ $0.36 \leq T \leq 1.4$	-0.03 $0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.18}\right)\right]-0.03$ -0.03

Figure 3b. DS3 Interface Isolated Pulse Mask Equations

CURVE	TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
MAXIMUM (UPPER) CURVE	$-0.85 \leq T \leq -0.68$ $-0.68 \leq T \leq 0.26$ $0.26 \leq T \leq 1.4$	0.03 $0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.34}\right)\right]+0.03$ $0.1 + 0.61e^{-2.4(T-0.26)}$
MINIMUM (LOWER) CURVE	$-0.85 \leq T \leq -0.38$ $-0.38 \leq T \leq 0.36$ $0.36 \leq T \leq 1.4$	-0.03 $0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.18}\right)\right]-0.03$ -0.03

Figure 3c. STS-1 Interface Isolated Pulse Mask Equations



*Note: UI = 1 / (System Clock Frequency)

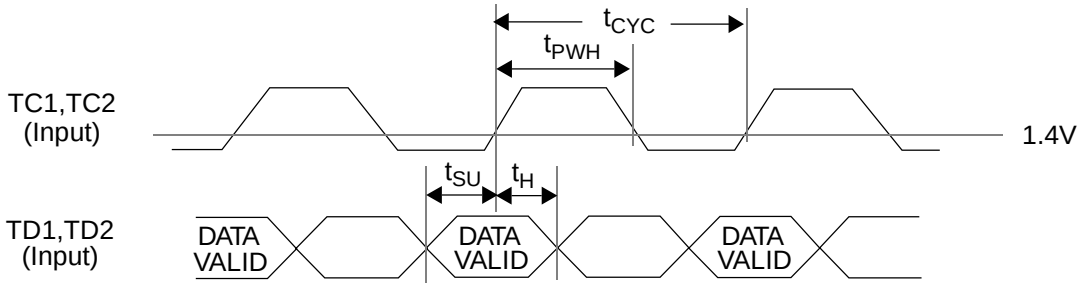
Outer region corner points			Inner region corner points		
Point	**Time**	**Amplitude**	**Point**	**Time**	**Amplitude**
A	-0.5	0.426	I	-0.245	0.214
B	-0.261	0.904	J	-0.187	0.455
C	-0.136	1.03	K	-0.104	0.67
D	-0.028	1.03	L	-0.017	0.67
E	0.094	0.883	M	0.077	0.581
F	0.187	0.723	N	0.18	0.14
G	0.31	0.566	O	-0.054	0.16
H	0.5	0.426			

Note - Both inner and outer regions are symmetric about zero amplitude axis.

Figure 3d. STS-1 Interface Eye Diagram Mask

Terminal Side Timing Characteristics

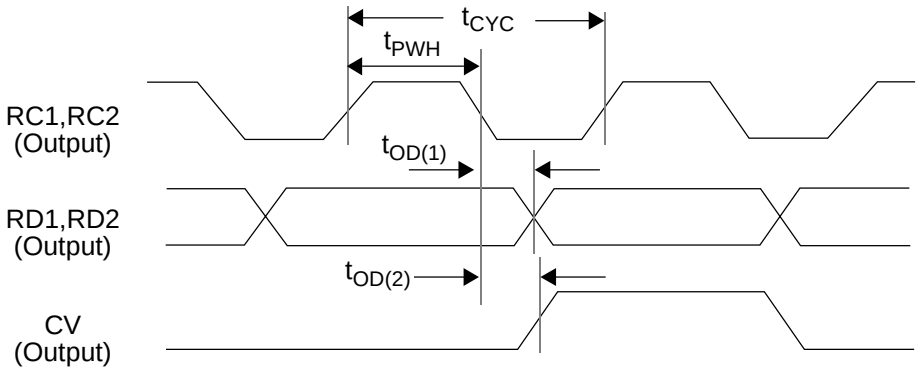
Figure 4. NRZ Transmit Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
TC1, TC2 DS3 input clock period	t_{CYC}		22.353		ns
TC1, TC2 STS-1 input clock period	t_{CYC}		19.290		ns
TC1, TC2 high time	t_{PWH}	10			ns
TC1, TC2 duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
TD1, TD2 set-up time to TC1↑, TC2↑	t_{SU}	4.0			ns
TD1, TD2 hold time after TC1↑, TC2↑	t_H	3.0			ns

Note: TC1, TC2 symmetry is measured about the 1.4VDC threshold in order to assure symmetric output waveforms.

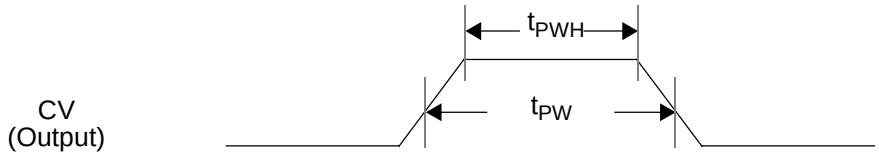
Figure 5. NRZ Receive Output Timing



Parameter	Symbol	Min	Typ	Max	Unit
RC1, RC2 DS3 output clock period	t_{CYC}		22.353		ns
RC1, RC2 STS-1 output clock period	t_{CYC}		19.290		ns
RC1, RC2 high time	t_{PWH}	10			ns
RC1, RC2 duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
$\overline{RD1}$, $\overline{RD2}$ output delay after RC1↓, RC2↓ ($\overline{RXAIS}$ = 1)	$t_{OD(1)}$	1.0		5.5	ns
$\overline{RD1}$, $\overline{RD2}$ output delay after RC1↓, RC2↓ ($\overline{RXAIS}$ = 0)	$t_{OD(1)}$	1.0		6.5	ns
CV output delay after RC1↓, RC2↓	$t_{OD(2)}$	1.0		5.5	ns

Note: RC1, RC2 symmetry is measured about the 50% amplitude point.

Figure 6. Coding Violation Pulse Timing



Parameter	Symbol	Min	Typ	Max	Unit*
CV pulse width	t_{PW}	0.9	1.0	1.1	UI
CV pulse high time	t_{PWH}	0.8	0.9	1.0	UI
CV delay from occurrence of violation	t_D		7.0		UI

*Note: UI = 1 / (System Clock Frequency)

OPERATION

Receiver Input Requirements

Parameter	Value
Interface Cable	AT&T 728A/734A coaxial (or equivalent)
Bit Rate:	
DS3	44.736 Mbit/s ± 20 ppm
STS-1	51.840 Mbit/s ± 20 ppm
Line Code	B3ZS
Input Signal Amplitude:	100 mVp - 0.95 Vp AC (differential input)
Cable Length	0 - 900 feet
Input Return Loss:	
DS3	> 26 dB at 22.368 MHz with external 75Ω resistor
STS-1	> 26 dB at 25.920 MHz with external 75Ω resistor
Input Resistance	> 5kΩ
Signal-to-Noise Tolerance	No greater than either the value produced by adjacent pulses in the data stream or ±10% of the peak pulse amplitude, whichever is greater.
Input Jitter Tolerance	As defined by Figures 7a, 7b and 7c: “Input Jitter Tolerance”*

*Note: Refer to the Operation - Jitter Tolerance subsection below for DS3 and STS-1 minimum requirements and measured values.

Interfering Tone Tolerance

The DS3LIM-SN will properly recover clock and present error-free output to the receive terminal side interface* in the presence of a sinusoidal interfering tone signal at the following line rates:

Interfering Tone Tolerance

Data Rate (Mbit/s)	Tone Frequency (MHz)	Maximum Tone Level
51.84	25.97	-20 dB
44.736	22.4	-20 dB

*Note: See Figure 8: “Interference Margin Test Configuration”

Receiver Output Specifications

Parameter	Value
Clock Recovery Jitter Peaking	1 dB maximum
Clock Recovery PLL pull-in time	< 100 μS
Sequences Reported as Coding Violations	++, --, not B0V, not 00V, three or more consecutive zeros (excessive zeros)

Transmitter Specifications

Note: A 75Ω ±5% output load is assumed in these specifications. Measurements made at transmitter unless otherwise noted.

Parameter	Value
TX_B3ZS Output Characteristics, TXLEV low:	The two pulse shapes specified below are to be measured at the end of 50-450 feet of cable, terminated by a 75Ω resistor.
Pulse Shape (DS3)	As defined by Figure 2 in ANSI TI.404-1994
Pulse Shape (STS-1)	As defined by Figure 4-10 in GR-253-CORE, Issue 2, December 1995
Amplitude	±0.81 Volts ±10% for DS3; ±0.95 for STS-1
Output jitter	0.05 UI maximum with jitter-free input clock on TC1, TC2
TX_B3ZS Output Characteristics, TXLEV high:	The two pulse shapes specified below are to be measured at the end of 0-50 feet of cable, terminated by a 75Ω resistor.
Pulse Shape (DS3)	As defined by Figure 2 in ANSI TI.404-1994
Pulse Shape (STS-1)	As defined by Figure 4-10 in GR-253-CORE, Issue 2, December 1995
Amplitude	±0.67 Volts ±10% for DS3; ±0.8 for STS-1
Output jitter	0.05 UI maximum with jitter-free input clock on TC1, TC2

*Note: UI = 1 / (System Clock Frequency)

AIS and Loopback Control Signal Arbitration

The response of the Module to combinations of the $\overline{\text{RXAIS}}$, $\overline{\text{TXAIS}}$, $\overline{\text{RT}}$ and $\overline{\text{TR}}$ input signals is tabulated below:

$\overline{\text{RXAIS}}$ *	$\overline{\text{TXAIS}}$ *	$\overline{\text{RT}}$ (line)	$\overline{\text{TR}}$ (term.)	Terminal Output	Line Output
1	1	1	1	Normal	Normal
1	0	X	1	Normal	AIS
1	0	X	0	Term Loopback	AIS
0	1	1	X	AIS	Normal
0	1	0	X	AIS	Line Loopback
0	0	X	X	AIS	AIS
1	1	1	0	Term Loopback	Normal
1	1	0	1	Normal	Line Loopback
1	1	0	0	Term Loopback	Line Loopback

Note: X = Don't Care
* These signals may only be applied (active low) when the Module is operating with DS3 signals.

Jitter Transfer

Transfer of jitter through an individual unit of digital equipment is characterized by the relationship between the applied input jitter and the resulting output jitter as a function of frequency.

For DS3, Bellcore Technical Reference GR-499-CORE, Issue 1, December 1995 further describes and defines jitter transfer.

For STS-1, Bellcore Technical Reference GR-253-CORE, Issue 2, December 1995 further describes and defines jitter transfer.

In a looped back configuration (through the receive path and externally looped back through the transmit path), in the absence of applied input jitter the amount of jitter introduced by the DS3LIM-SN is maximum 0.065 Unit Intervals (UIs, where UI is 1 / System Clock Frequency) of peak-to-peak jitter over a jitter frequency range of 20 Hz to 1 MHz (filter with high-pass of 10 Hz and a low-pass of 1.1 MHz).

With applied input jitter, the maximum output jitter is the applied input jitter plus the above jitter introduced by the DS3LIM-SN.

Jitter Generation

Jitter generation is the process whereby jitter appears at the output port of an individual unit of digital equipment in the absence of applied input jitter.

For DS3, Bellcore Technical Reference GR-499-CORE, Issue 1, December 1995 specifies the maximum jitter generation to be 1.0 UI of peak-to-peak at the output of the terminal receiver for Category I equipment.

For STS-1, Bellcore Technical Reference GR-253-CORE, Issue 2, December 1995 specifies the maximum jitter generation to be 1.5 UI peak-to-peak maximum at the output of the terminal receiver for Category I equipment.

In a looped back configuration (through the transmit path and externally looped back through the receive path), the DS3/STS-1 jitter generation within the DS3LIM-SN is 0.145 UI peak-to-peak maximum for all frequencies specified in these two standards.

Jitter Tolerance

DS3:

Input jitter tolerance is the maximum amplitude of sinusoidal jitter at a given jitter frequency, which, when modulating the signal at an equipment port, results in no more than two errored seconds cumulative, where these errored seconds are integrated over successive 30-second measurement intervals, and the jitter amplitude is increased in each succeeding measurement interval.

Requirements for input jitter tolerance are specified in terms of compliance with a jitter mask, which represents a combination of points. Each point corresponds to minimum amplitude of sinusoidal jitter at a given jitter frequency which, when modulating the signal at an equipment input port, results in two or fewer errored seconds in a 30-second measurement interval. Bellcore Technical Reference GR-499-CORE, Issue 1, December 1995 specifies the minimum requirement mask for Category I and Category II equipment, which are shown in Figures 7a and 7b.

Jitter tolerance within the DS3LIM-SN meets and exceeds the performance requirements. Figures 7a and 7b present the Bellcore DS3 minimum jitter tolerance requirement masks for Category I and Category II, respectively, and show the measured performance of the DS3LIM-SN, which exceeds both requirements.

STS-1:

For STS-1, jitter tolerance is specified in Bellcore Technical Reference GR-253-CORE, Issue 2, December 1995. The minimum requirement mask is shown in Figure 7c.

Jitter tolerance within the DS3LIM-SN meets and exceeds performance requirements. Figure 7c presents the Bellcore STS-1 minimum jitter tolerance requirement mask and the measured STS-1 performance of the DS3LIM-SN.

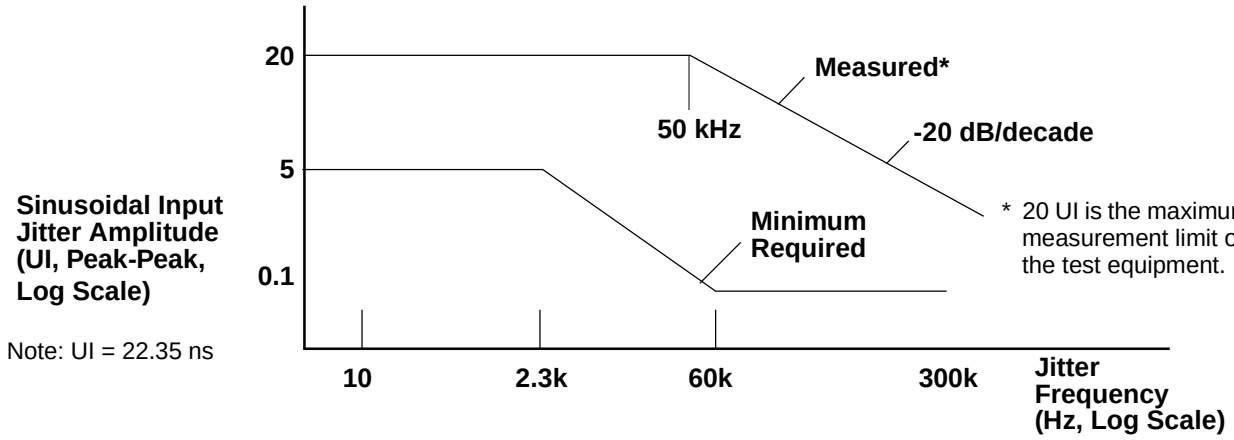


Figure 7a. DS3LIM-SN Input Jitter Tolerance for DS3 (Category I)

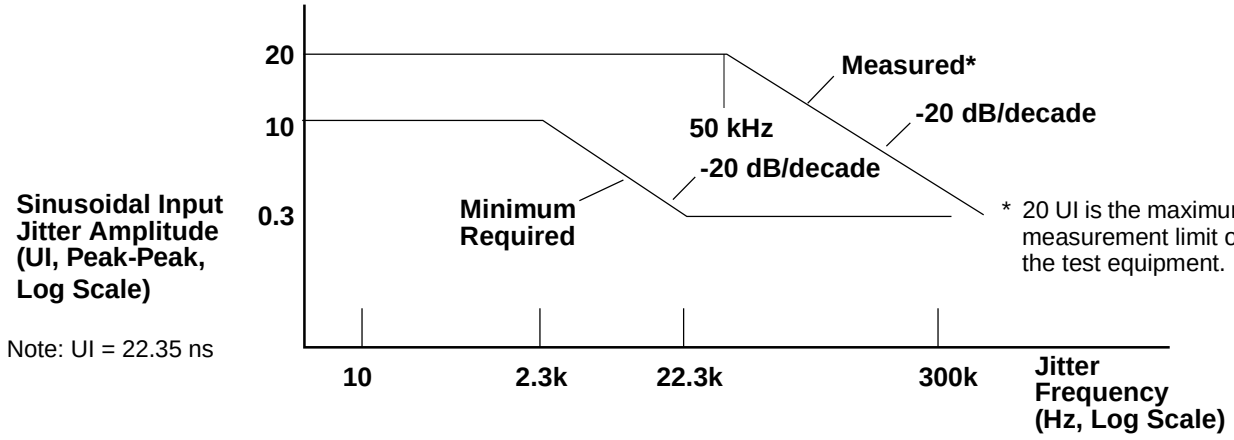


Figure 7b. DS3LIM-SN Input Jitter Tolerance for DS3 (Category II)

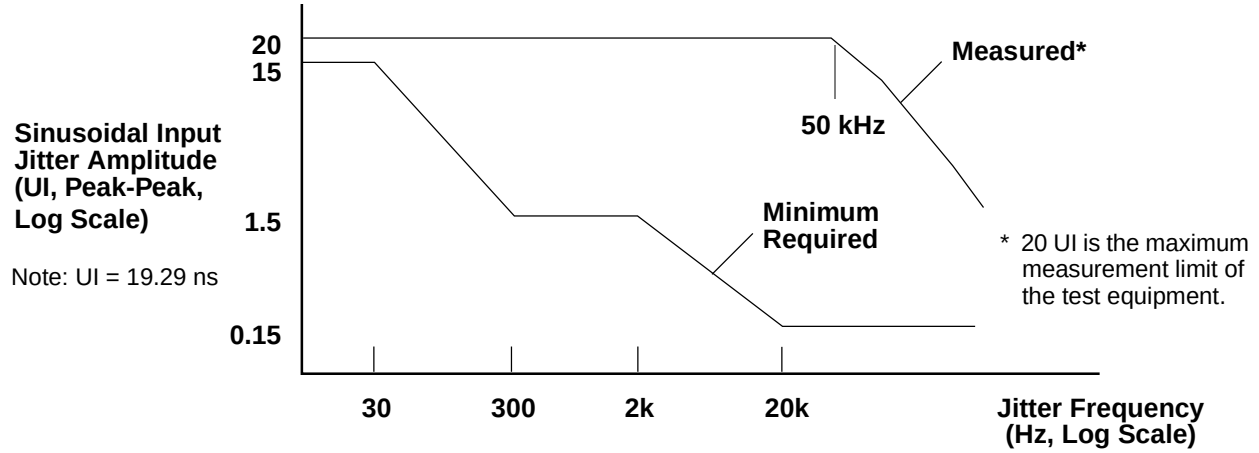
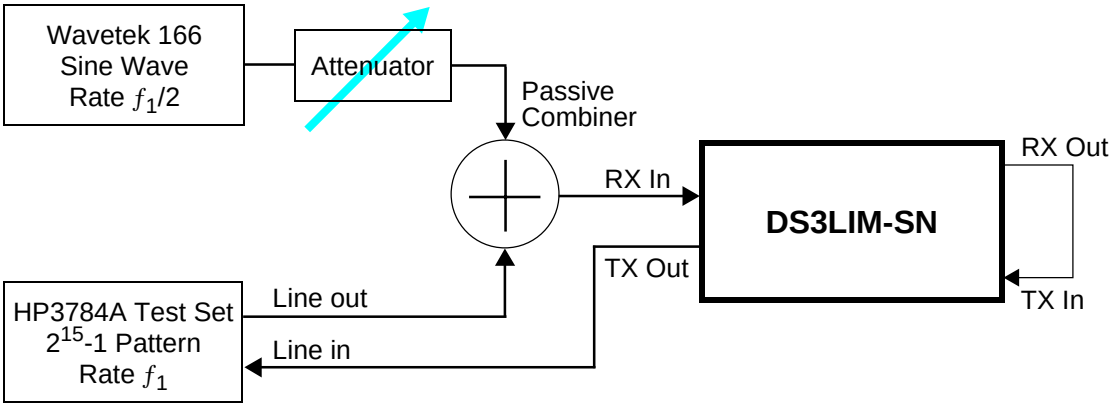


Figure 7c. DS3LIM-SN Input Jitter Tolerance for STS-1

Interference Margin

The interference margin of the DS3LIM-SN is measured using the test configuration shown in Figure 8.



Note: Wavetek generator is set for same pk-pk voltage as test pattern at 0 dB attenuator setting.

Signal	f_1, MHz	VCC, V	Min attenuation for no errors, dB
DS3	44.736	4.75 - 5.25	20
STS-1	51.84	4.75	20

Figure 8. Interference Margin Test Configuration

Physical Design of Motherboard

High-frequency design techniques must be employed for layout of the printed circuit board on which the DS3LIM-SN Module is mounted. The following guidelines and suggestions should be adhered to for a successful board design. At the DS3 and STS-1 frequencies it is important to use high-frequency layout techniques. The techniques discussed below are the bare minimum set that should be used.

A solid ground plane should be used. 'Solid' in this instance means that the impedance from any point in the plane to the board ground connection should be low. This is very important in regards to the location of the analog DS3LIM-SN device since its SNR can be severely degraded by I*Z drops in these planes. Under no circumstances should a DS3LIM-SN ground pin be connected to ground through a trace. The trace has a finite impedance at high frequencies; it is not a short. Ground currents through the trace impedance will cause voltage noise.

Do not use a solid power plane. Break the +5V power plane into regions as shown in Figure 9. Additionally, there should be a +5V region for board logic. Use as wide a path as possible back to the common connecting point. If the power and ground planes are placed in adjacent layers there will be an additional noise reduction due to capacitive coupling. For example, a six-layer board could be signal-signal-power(ground)-ground(power)-signal-signal.

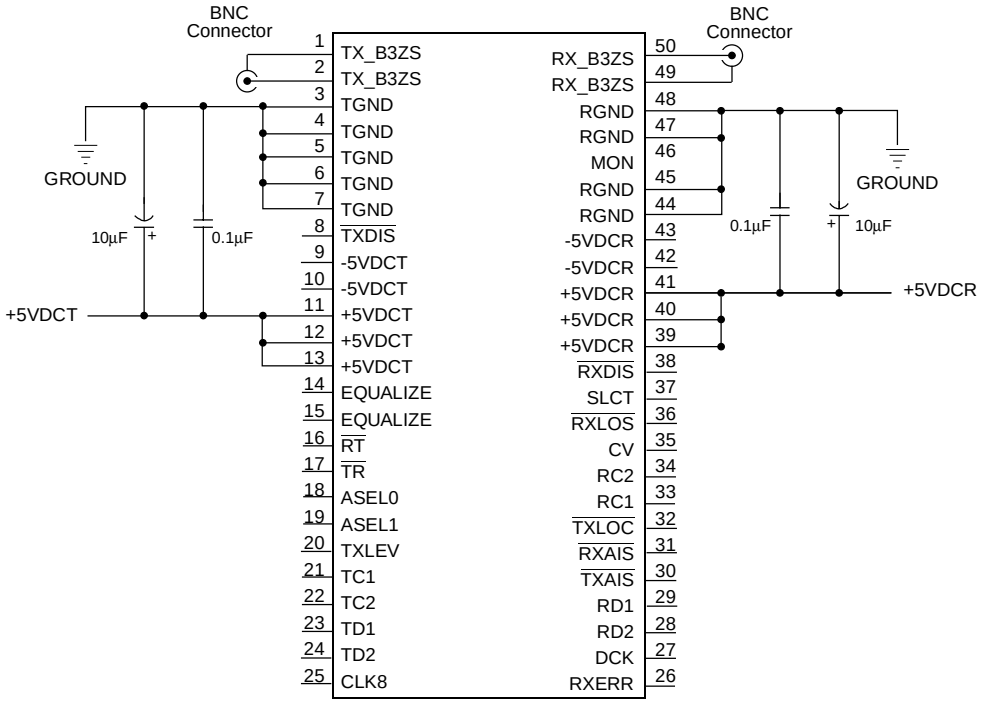


Figure 9. Power Supply and Ground Connections

For the input and output signal connections of the DS3LIM-SN Module a board trace at high frequencies is not a zero-impedance metal interconnection. It is a distributed L/C network. The values of the L and C parasitic components are determined by trace geometry (width and height) and the surrounding material. Component layout should be arranged to permit the use of short traces, especially for the analog inputs. These input traces should be restricted to one side of the motherboard, since vias have been found to cause degraded performance due to output signal coupling. A trace with a given geometry will have a different impedance if it is on an

outside board layer from the same trace placed instead in an internal layer. Large branches off a main trace will change the impedance at the branch point due to the effect of impedances in parallel, so branch lengths should be kept to a minimum (less than a quarter wavelength). This is very important for clock lines where load/source impedance mismatches can cause severe ringing, which leads to timing problems. Use clock buffers to reduce the difficulty of distributing a clock with many loads.

If relays are used to switch the transceivers in and out, use the 50 ohm shielded variety to minimize crosstalk, especially from the power used to energize the relay. Match the impedance of the board traces of the transmitter outputs and receiver inputs to the transmission line impedance (75 ohms if a 1:1 transformer is used) to minimize reflections, and do not use vias in these signal paths. Physically separate the analog signal lines from the digital lines. Route the differential receiver lines side by side to make coupled noise common-mode. Avoid ninety-degree corners in the board lands; keep lands as straight and short as possible. Use terminating (i.e., 51 ohm series-damping) resistors in the digital signals lines where appropriate (i.e., if the line is longer than a quarter wavelength of the highest signal frequency of importance, reflections will start causing problems).

The above comments are guidelines only. High-frequency board layout is difficult and must be done with care. A bad board layout will reduce the SNR of the transceiver and cause timing problems with the board logic, perhaps to the point of requiring a complete board redesign.

FUNCTIONAL DIFFERENCES BETWEEN THE DS3LIM-SN AND DS3LIM MODULES

The following nine functional differences between the DS3LIM-SN and DS3LIM Modules affect the utilization of the pins of the Module. The first two of these differences do not affect the ability of the DS3LIM-SN to be used as a direct replacement for the DS3LIM. The others represent performance differences which may require special accommodation by the user.

1. Equalization (Pins 14, 15)

The DS3LIM requires provision of a strap between the two EQUALIZE input pins (14, 15) for line input cable lengths less than 200 feet. Due to incorporation of the ART VLSI device, which has adaptive equalization, the DS3LIM-SN can provide equalization for all line input cable lengths from zero to 900 feet automatically, without any such special settings based on cable length. The EQUALIZE pins are unused in the DS3LIM-SN.

2. Amplifier Gain Select (Pins 18, 19)

The DS3LIM requires external pull-up resistors connected to the ASEL0 and ASEL1 input pins (18, 19) for line input amplifier gain selection. Due to its use of the ART device the DS3LIM-SN has AGC and does not use these two pins.

3. -5V Power Supply (Pins 9, 10, 42, 43)

The DS3LIM-SN does not require the -5V power supply used by the DS3LIM. The four -5V power input pins (9, 10, 42, 43) are unused. However, the +5V power supply current requirement of the Module increases from 200 mA for the DS3LIM to 290 mA for the DS3LIM-SN.

4. TXLEV Input (Pin 20, Transmit Level select for DS3LIM)

The DS3LIM can meet line output pulse mask requirements for all cable lengths from zero to 450 feet with the TXLEV input (pin 20) set low. With TXLEV set high or left floating a higher transmit level is provided, which may permit satisfactory performance with longer cables. For the DS3LIM-SN the TXLEV input must be set according to cable length: low for cable lengths from 50 to 450 feet and high (10kΩ resistor to +5V) for cables shorter than 50 feet. There is no special provision for cables longer than 450 feet.

For cable lengths from 50 to 450 feet (TXLEV low) the DS3LIM-SN is compatible with the DS3LIM. For cables shorter than 50 feet the low TXLEV setting provided for the DS3LIM is not suitable, and TXLEV

must be changed to high. For cables longer than 450 feet the DS3LIM-SN may not be able to match the DS3LIM output pulse performance with TXLEV set high even if TXLEV is changed to low.

Unlike the DS3LIM, the TXLEV pin has no pull-up resistor in the DS3LIM-SN, so the pin does not pull high if it is left floating and the transmit output mode selection is indeterminate. It is necessary for the pin to be driven either high or low by an external connection.

5. RXERR Output (Pins 25 and 26, Receive Error Rate for DS3LIM)

The DS3LIM-SN indicates B3ZS coding violations like the DS3LIM, but it does not measure bit error rates using an 8 kHz clock input (CLK8, pin 25), and it cannot indicate error rates above 10^{-6}, which the DS3LIM does by setting the RXERR output (pin 26) high. (Note: The Edition 3 Data Sheet for the DS3LIM incorrectly describes this as an active low signal, $\overline{\text{RXERR}}$.)

The DS3LIM-SN has the CLK8 pin internally disconnected and the RXERR pin internally tied low to simulate an error-free condition at all times, so that it can be used in place of the DS3LIM, but it will not report bit error rates that exceed the 10^{-6} threshold. The bit error rate may be calculated externally in the user's application, based on monitoring of the coding violation pulses that are provided as the CV output (pin 35) of the DS3LIM-SN.

6. Loopback Capability (Pins 16, 17)

The DS3LIM Module suffers data corruption at the terminal and line interfaces if the line ($\overline{\text{RT}}$, pin 16) and terminal ($\overline{\text{TR}}$, pin 17) loopback features are selected simultaneously. The DS3LIM-SN exhibits the extended loopback capabilities of the ART VLSI device, as described in the Operation section of this Data Sheet, and is not subject to data corruption with simultaneous loopbacks.

The implementation of extended loopback capabilities in the ART VLSI device required the use of internal loopback path configurations different from those in the DS3RT VLSI device of the DS3LIM. The different path used for terminal loopback results in a requirement for user application accommodations in treatment of the $\overline{\text{RXLOS}}$ and CV output signals when the DS3LIM-SN is substituted for the DS3LIM, as described below.

The DS3LIM implements terminal loopback (Transmit-to-Receive (TR) loopback) close to the line side inputs and outputs within its DS3RT receiver/transmitter VLSI device. When TR loopback is active, the $\overline{\text{RXLOS}}$ and CV output signals are driven by the looped-back transmit input signal and will usually indicate normal operation (i.e., no receive loss of signal or coding violations).

The DS3LIM-SN implements terminal loopback close to the terminal side inputs and outputs within its ART receiver/transmitter VLSI device. When TR loopback is active, the receive input path connection through to the receive output is disabled, but the $\overline{\text{RXLOS}}$ and CV output signals are still driven by the receive input signal. If there is no valid input signal, or the receive input is disconnected during TR loopback so that there is noise pickup, the $\overline{\text{RXLOS}}$ and CV output signals will reflect this indeterminate receive input condition rather than the looped-back transmit input signal. Spurious receive loss of signal and coding violation indications may result. The user application should either disregard the $\overline{\text{RXLOS}}$ and CV outputs during TR loopback or arrange to apply a valid signal to the receive input so that these outputs do not become active.

7. $\overline{\text{TXLOC}}$ Output (Pin 32, Transmit Loss of Clock for DS3LIM)

The DS3LIM-SN does not have the capability to detect and indicate when the transmit input clock (TC1, TC2) is stuck high or low, which the DS3LIM does by setting the $\overline{\text{TXLOC}}$ output pin (32) low.

The DS3LIM-SN has the $\overline{\text{TXLOC}}$ pin internally pulled up to simulate an error-free condition at all times, so that it can be used in place of the DS3LIM but will not report a loss of clock condition.

8. Receive Loss of Signal Modified ($\overline{\text{RXLOS}}$, pin 36)

The DS3LIM detects and indicates receive loss of signal when a positive or negative data transition does not occur for 128 or more clock cycles. Recovery occurs on the first positive or negative transition.

The DS3LIM-SN detects and indicates receive loss of signal when 175 ± 75 zeroes appear in the incoming data stream. Recovery occurs when the ones pulse density is in the range of 28% to 33% (or more than 33%) for 175 ± 75 consecutive pulses.

9. Receive Signal Monitor Output (MON, pin 46)

The TXC-20153D version of the DS3LIM-SN is more sensitive to external loading of this output pin than is the DS3LIM Module. The TXC-20153G version does not have a monitor output connection to pin 46.

10. Digital Input and Output Parameter Type Changes (Pins Listed Below)

The pins listed below have different Types of input or output parameter in the DS3LIM-SN and the DS3LIM. Electrical parameter definitions for these Types are provided in the Input and Output Parameters Section of this Data Sheet.

Symbol	Pin No.	I/O	Parameter Type	
			DS3LIM-SN	DS3LIM
$\overline{\text{TXDIS}}$	8	I	TTLp	CMOS or TTL
$\overline{\text{RT}}$	16	I	TTLp	CMOSr
$\overline{\text{TR}}$	17	I	TTLp	CMOSr
DCK	27	I	CMOS(1)	TTL
$\overline{\text{TXAIS}}$	30	I	TTLp	TTLr
$\overline{\text{RXAIS}}$	31	I	TTLp	CMOSr
CV	35	O	CMOS	TTL2mA
$\overline{\text{RXLOS}}$	36	O	CMOS	TTL2mA
TXLEV(2)	20	I	TTL	CMOSr

Notes:
1. A 10 kΩ pull-up resistor is provided in the TXC-20153G Module only.
2. No pull-up resistor is provided in the DS3LIM-SN Modules.

CIRCUIT DIAGRAMS

The circuit diagram for the TXC-20153D and TXC-20153G Edition 1 versions of the DS3LIM-SN Module is provided in Figure 10. Note 1 of this figure indicates the differences between the TXC-20153D and TXC-20153G versions. The resistors marked X are not installed, since the Module has the NRZ interface. Figure 11 shows the corresponding circuit diagram for the TXC-20153G Edition 2, which provides 4 dB attenuation at the receive line input. Both circuit diagrams are reduced versions of larger drawings, so the annotation text is unavoidably small. Enlarged versions of the diagrams may be viewed or printed from the PDF file version of this Data Sheet on the TranSwitch World Wide Web Site (www.transwitch.com) using Acrobat Reader software. The Reader can zoom portions of the diagram for viewing. A zoomed area may then be selected with Tools/ Select Graphics and Edit/Copy to move it via the clipboard to any word processor (Edit/Paste) for printing.

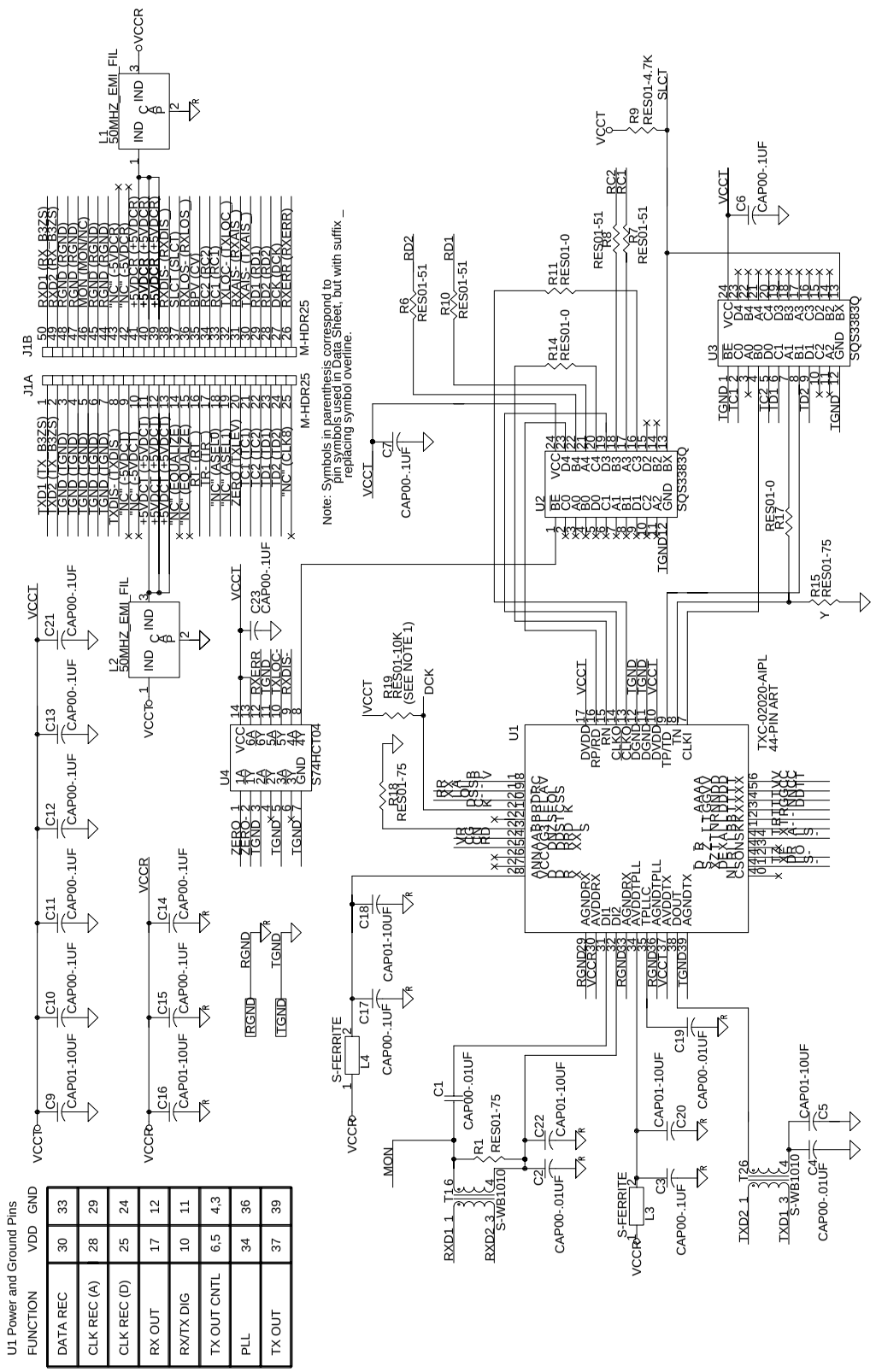


Figure 10. DS3LIM-SN Circuit Diagram (TXC-20153D, TXC-20153G Edition 1)

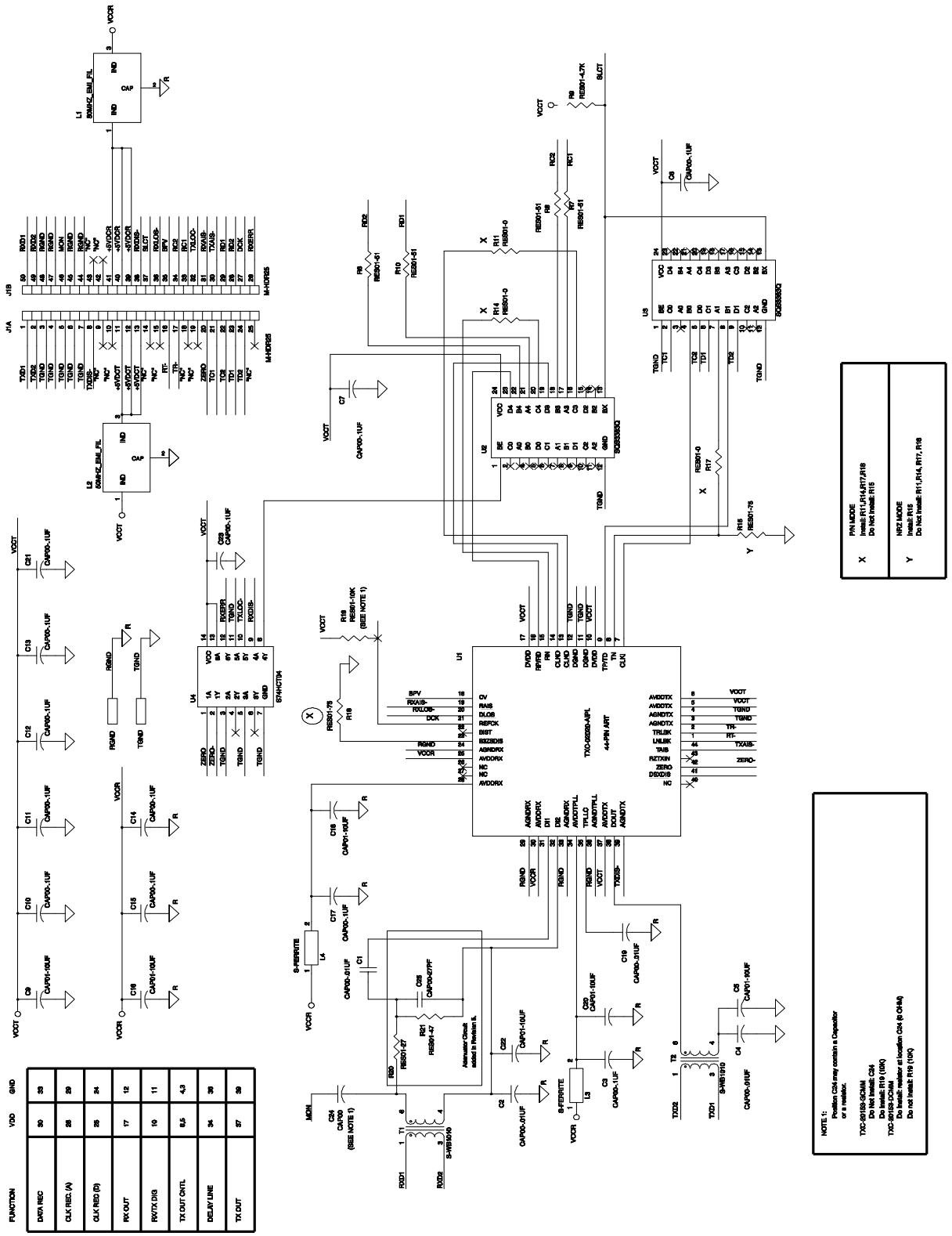
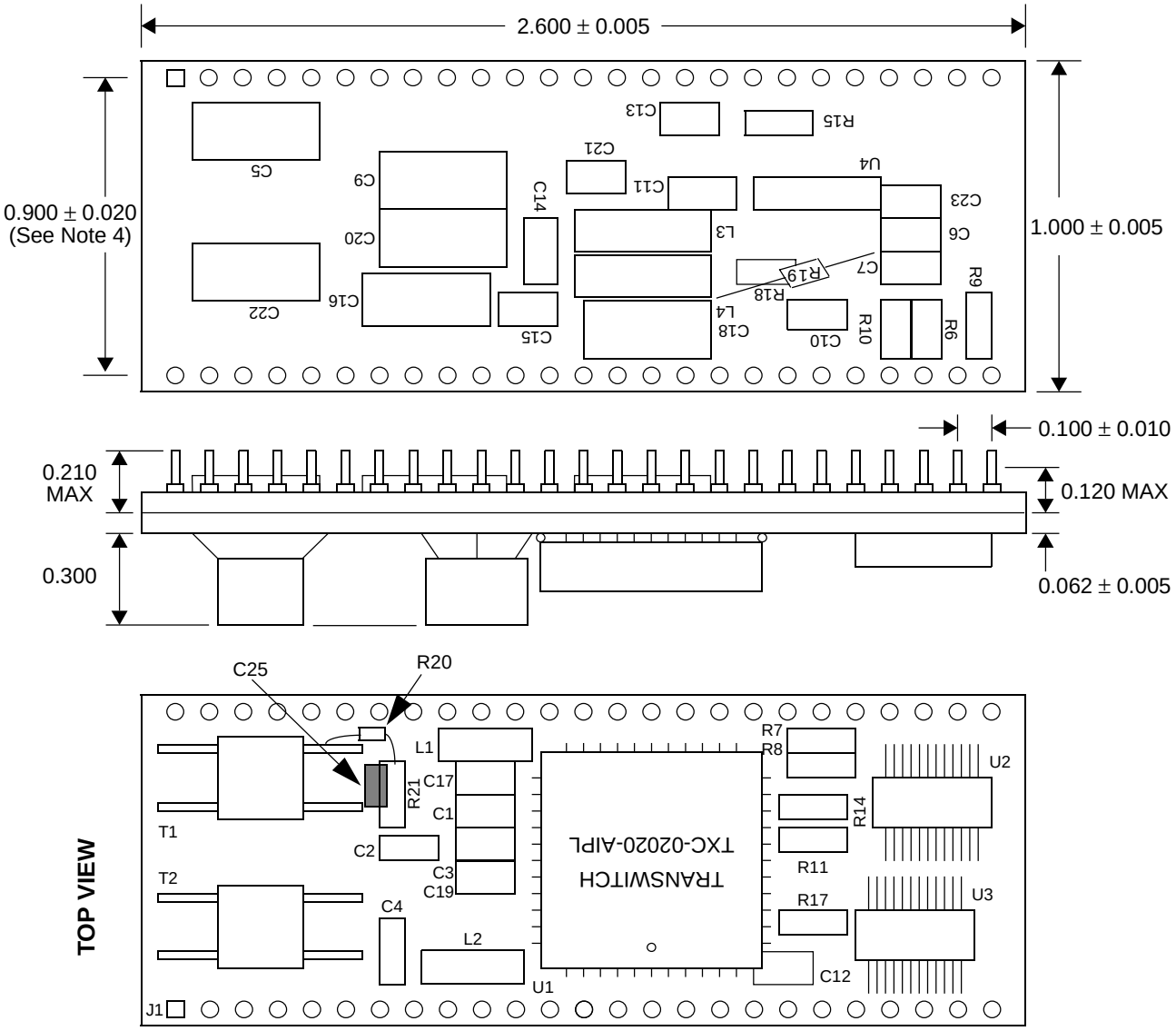


Figure 11. DS3LIM-SN Circuit Diagram (TXC-20153G Edition 2)

PACKAGE INFORMATION

The DS3/STS-1 Line Interface Module consists of a 2.6 x 1.0 inch multi-layer printed circuit board with surface mounted components on both sides and 50 signal/power pins at 0.1 inch spacing on the two long edges to provide a DIP configuration. Figure 12 is a simplified drawing that shows three views of the Module. All dimensions are in inches and are nominal unless otherwise indicated.



Notes:

1. Module is shown approximately twice full size.
2. All dimensions are in inches, and are nominal unless otherwise indicated.
3. R11, R14, R17 and R18 are not installed. R19 (10 kΩ) is a coaxial-lead resistor.
4. The axis of each pin is located within ± 0.010 inch vertically and ± 0.005 inch horizontally from its nominal position.
5. This figure shows the component layout for TXC-20153G Edition 2 (also refer to Figure 11).
6. The component layout for TXC-20153D and TXC-20153G Edition 1 has C25 and R20 removed, and R21 replaced by R1 (refer to Figure 10).

Figure 12. DS3LIM-SN Simplified Outline Drawing

The DS3LIM-SN can be installed without or with a socket on the motherboard, as shown in Figures 13 and 14, respectively. All dimensions are shown in inches and are nominal unless otherwise indicated.

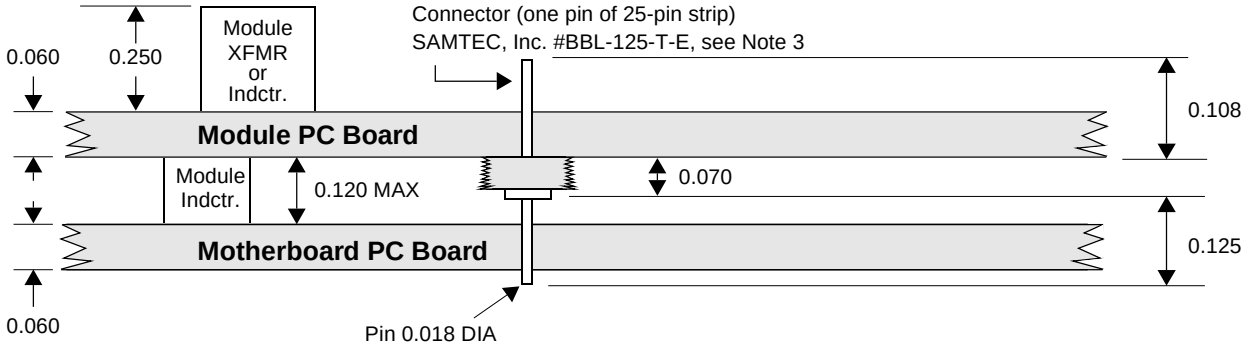


Figure 13. Installation Without Motherboard Socket

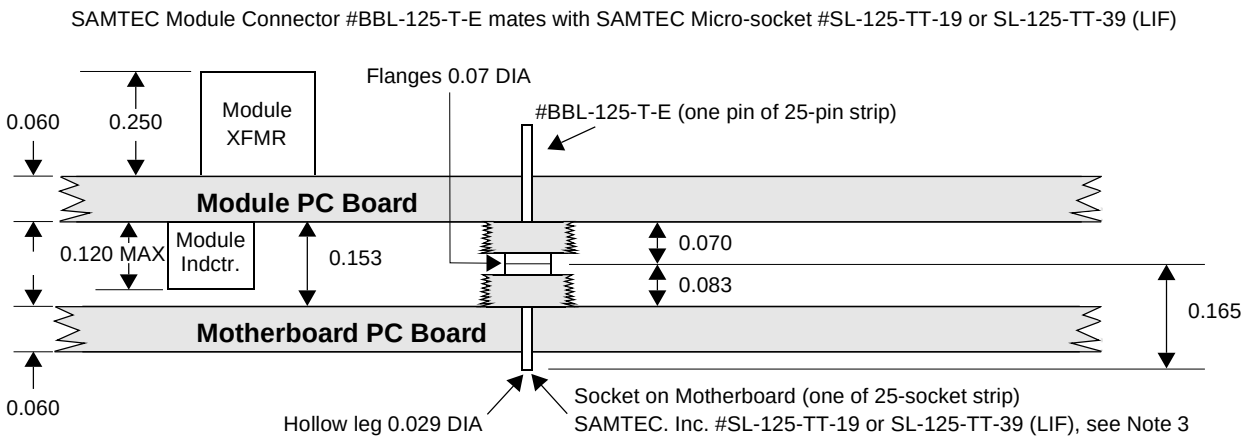


Figure 14. Installation With Motherboard Socket

Notes For Figures 13 and 14:

1. All dimensions are in inches and are nominal unless otherwise indicated.
2. Drawings not to scale.
3. SAMTEC, Inc.
   P.O. Box 1147
   New Albany, Indiana 47151-1147 USA
   Phone: 812-944-6733
   Fax: 812-948-5047
   TWX: 810-540-4095
   Telex: 333-918

ORDERING INFORMATION

Product Number: TXC-20153D
Part Number: TXC-20153-DCMM DS3/STS-1 Line Interface Module, NRZ Clock/Data Output
50-Pin Dual In-Line Package
Monitor pin provided for receive line signal input, no DCK pull-up

Product Number: TXC-20153G
Part Number: TXC-20153-GCMM DS3/STS-1 Line Interface Module, NRZ Clock/Data Output
50-Pin Dual In-Line Package
No monitor pin, pull-up provided for DCK external clock input)
Edition 1: 0 dB attenuation provided for receive line input
Edition 2: 4 dB attenuation provided for receive line input

RELATED PRODUCTS

TXC-20049D, DS3LIM Module (DS3 Line Interface Module). A complete analog to digital converter which receives and transmits B3ZS-encoded DS3 line signals and provides serial NRZ clock and data interfaces on the terminal side.

TXC-21049, DS3LIM Evaluation Board. A complete, ready-to-use test bed for the test and evaluation of the DSLIM-SN and DS3LIM Line Interface Modules. The Module plugs into a socket on the evaluation board, input and output signals are terminated via BNC connectors, and all functions of the Module are selectable via jumper insertion/extraction on the evaluation board.

TXC-20163, E3LIM Module (E3 Line Interface Module). A complete and compact full duplex analog line to digital terminal interface that converts an HDB3-encoded line signal, in E3 asynchronous format, to and from NRZ data and clock signals. The E3LIM is packaged as a 2.6 inch x 1.0 inch 50-pin Dual In-Line Package (DIP) Module.

TXC-02020, ART VLSI Device (Advanced DS3/STS-1 Receiver/Transmitter). Performs the receive and transmit line interface functions required for transmission of DS3 (44.736 Mbit/s) or STS-1 (51.840 Mbit/s) signals across a coaxial interface. The TXC-02021 ARTE device has some extended features relative to the ART and has a different package with more pins to support additional input and output signals.

TXC-03303, M13E VLSI Device. This single-chip multiplex/demultiplex device provides the complete interfacing function between a single DS3 signal and 28 independent DS1 signals.

TXC-03401B, DS3F VLSI Device (DS3 Framer). Maps broadband payloads into the DS3 frame format. Operates in either the C-bit parity or M13 operating modes.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator Receiver). Programmable multi-rate test pattern generator and receiver in a single chip with serial, nibble, or byte interface capability.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

The ATM Forum (U.S.A.):

ATM Forum World Headquarters
303 Vintage Park Drive
Foster City, CA 94404-1138

Tel: 415-578-6860
Fax: 415-525-0182

ATM Forum European Office
14 Place Marie - Jeanne Bassot
Levallois Perret Cedex
92593 Paris France

Tel: 33 1 46 39 56 26
Fax: 33 1 46 39 56 99

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

EIA - Electronic Industries Association (U.S.A.):

Global Engineering Documents
Suite 407
7730 Carondelet Avenue
Clayton, MO 63105

Tel: 800-854-7179 (In U.S.A.)
Fax: 314-726-6418

ETSI (Europe):

European Telecommunications Standards Institute
ETSI, 06921 Sophia - Antipolis
Cedex France

Tel: 33 92 94 42 00
Fax: 33 93 65 47 16

ITU-T (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (T)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

TC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated DS3LIM-SN Data Sheet that have significant differences relative to the previous and now superseded DS3LIM-SN Data Sheet:

Updated DS3LIM-SN Data Sheet: Ed. 2, August 1998

Previous DS3LIM-SN Data Sheet: Ed. 1A, November 1996

The page numbers indicated below of this updated Data Sheet include significant changes relative to the previous data sheet. Please note that repagination changes and changes of Figure numbers are not listed.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
1, 40, 42	Changed TranSwitch street address in Shelton, CT.
1	In Features list, changed features five and six.
2-3	Updated Table of Contents and List of Figures.
4	Changed third paragraph.
5	In Figure 1, added 4 dB Attenuator block after receive line input transformer. Changed second paragraph.
7	Added C25, R20 and R21 to Figure 2.
11	Added “Edition 1 and Edition 2” to Name/Function column for pin 46.
12	Changed first table and moved ambient operating temperature row from second table to first table.
14	Deleted Output Parameters For TTL2mA table (no pins of this type). Changed last table
15	Changed first table.
16	Changed first paragraph.
21	Changed Value column for Input Signal Amplitude, Cable Length and Input Jitter Tolerance in first table. Changed Maximum Tone Level column for both rows in second table.
22	Changed Values for Pulse Shape (DS3) and Pulse Shape (STS-1) in first table. Changed Parameter and Value in last row of first table.
23	Updated Bellcore Technical Reference numbers in 6 locations. Added references to Category 1 equipment and associated new Figure 7a.
24	Added Figure 7a. Changed titles of Figures 7b and 7c.
25	Changed last column of table in Figure 8.
26	Changed second and third paragraphs of Physical Design of Motherboard. Changed RGROUND and TGROUND to GROUND in Figure 9.
27	Changed 450 feet to 900 feet in “1. Equalization (pins 14,15)” subsection.

Page Number of Updated Data Sheet	Summary of the Change
29	Changed last paragraph.
30	Changed title of Figure 10.
31	Added Figure 11.
32	Changed Top View and added notes 5 and 6 of Figure 12.
34	Changed Ordering Information to describe the three versions of the DS3LIM-SN Module that can be ordered. Updated Related Products.
35	Updated Standards Documentation Sources, adding EIA.
37-38	Substituted new List of Data Sheet Changes.
41	Updated Documentation Update Registration Form.

- Notes-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