CUBIT Device
CellBus Bus Switch
TXC-05801

DATA SHEET

FEATURES

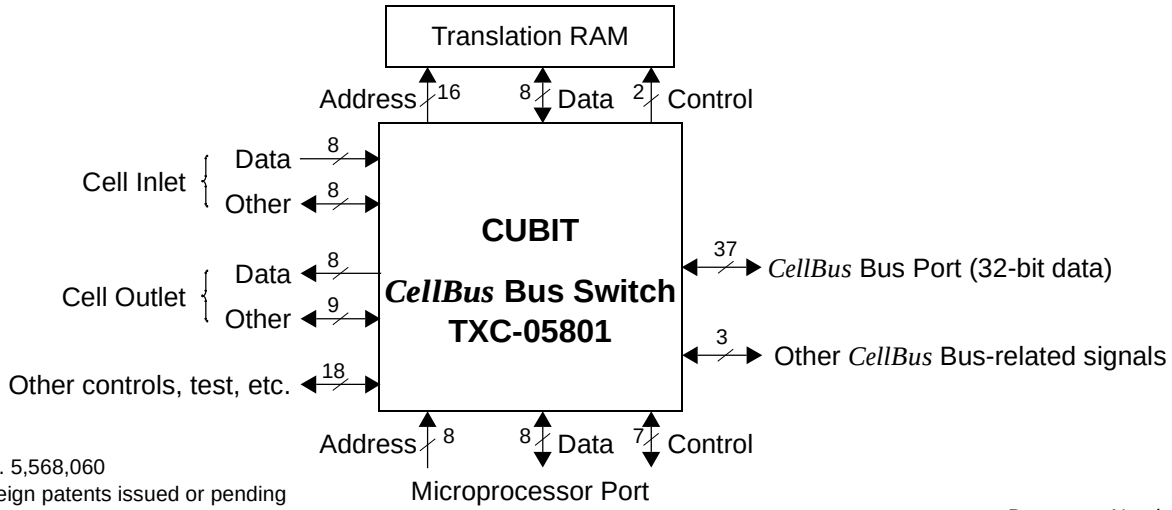
- UTOPIA or ALI-25 physical-layer cell interface
- Inlet-side address translation and routing header insertion, using external SRAM
- Programmable OAM cell routing
- *CellBus* bus access request, grant reception and bus transmission
- *CellBus* bus cell reception and address recognition
- Outlet cell queuing: various modes
- Ability to insert GFC field in real time
- Ability to insert FECN indication, under programmable conditions
- Support for ABR-type traffic with minimal cell loss
- Ability to send and receive cells for control purposes over same *CellBus* bus
- Cell insertion and extraction via microprocessor port
- Master bus arbiter included in each CUBIT
- Internal GTL transceivers for *CellBus* bus connection
- Interface port to translation table SRAM
- Microprocessor control port, selectable for Intel or Motorola interface
- 208-pin plastic quad flat package

DESCRIPTION

CUBIT is a single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* bus architecture. Such systems are constructed from a number of CUBIT devices, all interconnected by a 37-line common bus, the *CellBus* bus. When operating at a 38 MHz clock rate, a *CellBus* bus system can handle 1 Gbit/s of net ATM cell bandwidth. CUBIT supports unicast and multicast transfers, and has all necessary functions for implementing a switch: inlet queuing, cell address translation, cell routing, and outlet cell queuing.

APPLICATIONS

- ATM LAN hub
- Router Front-End
- ATM multiplexer/concentrator
- Small-stand-alone ATM switch
- Add-Drop Ring Switch
- B-ISDN access multiplexer
- Edge switching equipment
- Cable TV Distribution



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LIST OF FIGURES

BLOCK DIAGRAM

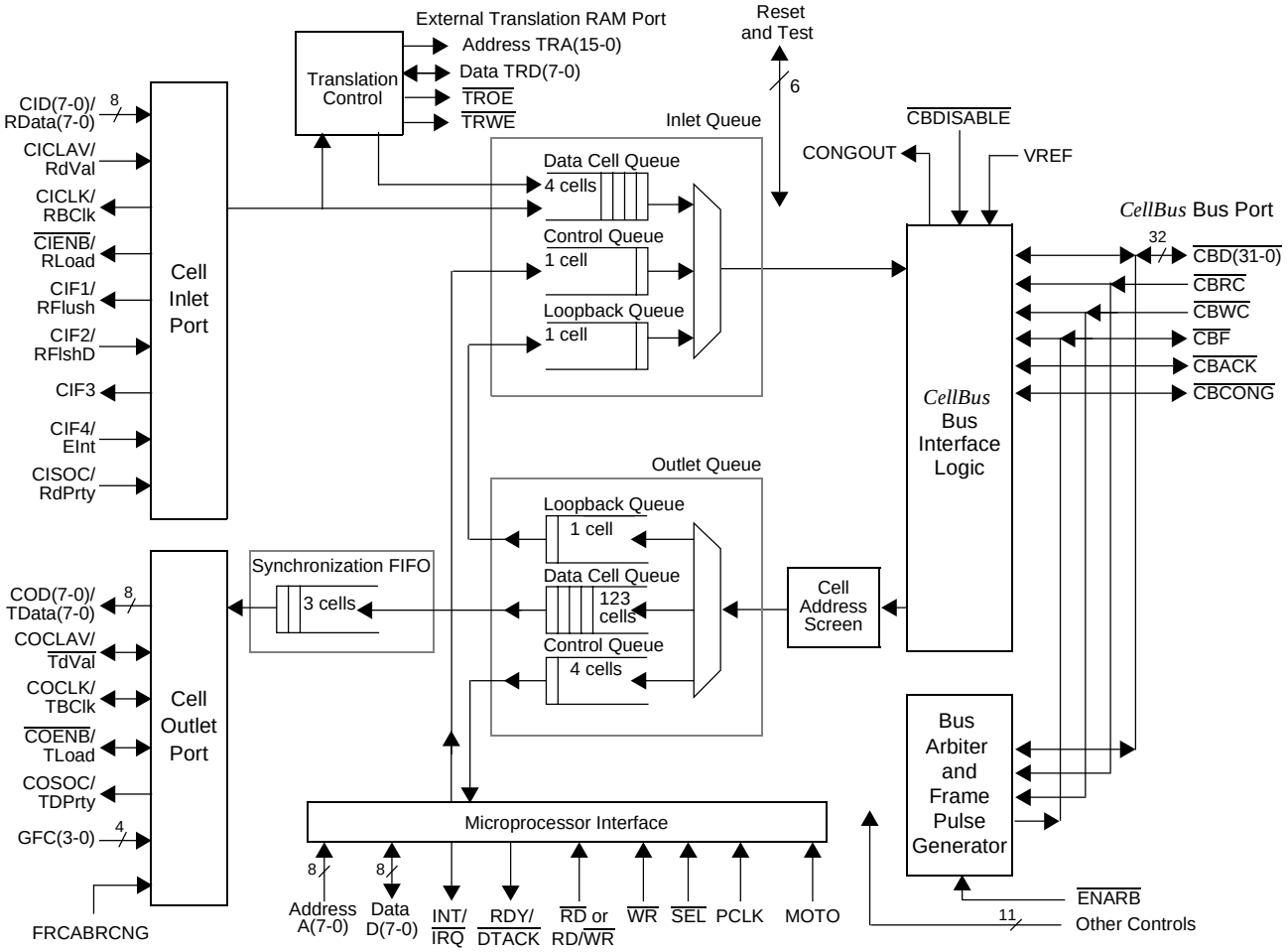


Figure 1. CUBIT TXC-05801 Block Diagram

A block diagram of the CUBIT device is shown in Figure 1. Further information on device operation and the interfaces to external circuits is provided below in the following Operation section.

On the cell inlet side of the CUBIT is circuitry associated with accepting cells from the line and passing them to the *CellBus* bus with an appropriate header. The Cell Inlet Port block is pin-selectable to be compliant with either the ATM Forum UTOPIA (Universal Test and Operations Physical Interface for ATM) interface or the TranSwitch ALI-25 device interface. Incoming cells may carry a *CellBus* Bus Routing Header and translated outgoing VPI/VCI address, the translation function having been performed externally, or this address translation and routing header insertion may be done by the CUBIT Translation Control block. Translation and routing header tables to support this function are contained in a small external static RAM (up to 64k x 8 bits). They support VPI and/or VPI/VCI address translation. The incoming cells then pass through a FIFO queue in the Inlet Queue block to the *CellBus* bus Port via the *CellBus* bus Interface Logic block. When there is a cell in this 4-cell data cell queue, the CUBIT makes a bus access request, and waits for a grant from the Bus Arbiter and Frame Pulse Generator block of the one CUBIT device attached to the bus that has been enabled to perform these two functions. When a bus access grant is received, the CUBIT sends the cell to the bus, in standard *CellBus* bus format. The cell can then be received by any connected CUBIT or CUBITs. In addition to these incoming data cells, the CUBIT can also send Control cells from the local microprocessor to the bus via the Microprocessor Interface block. Special cells of Loopback type received from the bus may also be returned to the bus, re-directed back to the CUBIT which launched the original Loopback cell. Both the Control cells and the Loopback cells have 1-cell inlet queues.

On the cell outlet side, cells of proper unicast address, broadcast address or selected multicast address, received from the bus via the *CellBus* bus Interface Logic block, are recognized by the Cell Address Screen block and routed into a FIFO structure in the Outlet Queue block. The unicast address is unique per device, set by device straps. Each CUBIT may be programmed to accept cells associated with multicast sessions. From zero up to the full 256 multicast sessions may be accepted independently by each CUBIT on the bus. Data cells from the bus go into a 123-cell outlet data cell queue structure. Control cells and Loopback cells arriving from the bus are routed to the 4-cell outlet control queue, and the 1-cell outlet loopback queue, respectively. The outlet data cell FIFO structure can be treated as a single 123-cell queue, or it can be subdivided into four individual queues for traffic of different service types. The four-queue split is typically into High-speed "control" cells, CBR cells, VBR cells, and ABR cells, in decreasing order of outlet service priority. This allows for delay minimization of critical service types, and for more efficient traffic management. At the cell outlet, provisions are made for insertion of an outgoing Generic Flow Control (GFC) field and a Forward Explicit Congestion Notification (FECN) bit.

OPERATION

INTRODUCTION TO *CellBus* Bus

CellBus Bus Operation

The CUBIT is a versatile CMOS VLSI device for implementing ATM switching functions. Various ATM cell switching or multiplexing structures can be formed by interconnection of a number of CUBIT devices over a 37-line parallel bus with 32 data bits, the *CellBus* bus. Since the interconnect structure is a bus, communications between any of the devices on the bus is possible. Each cell placed onto the *CellBus* bus by a CUBIT device can be routed either to one single CUBIT (unicast addressing), or to multiple CUBIT devices (multicast or broadcast addressing). Depending upon the needs of an application, up to 32 CUBIT devices may be interconnected on one *CellBus* bus. With a maximum bus frequency of more than 33 MHz, the raw bandwidth of the *CellBus* bus exceeds 1 Gbit/s.

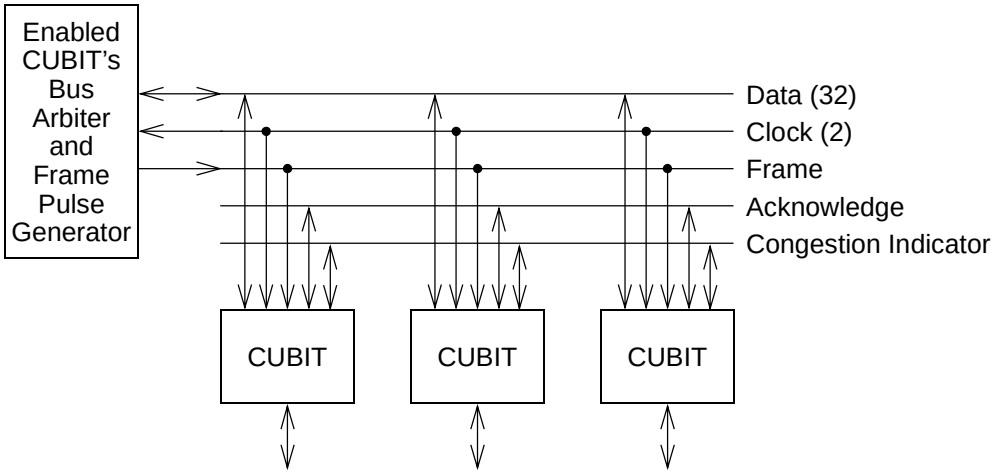


Figure 2. *CellBus* Bus Structure

CellBus bus, as shown in Figure 2, is a shared bus, and can be implemented either on a single circuit card, or in a backplane configuration among multiple circuit cards. Since multiple CUBITs share the same bus, bus access contention must be resolved. This access contention is resolved by use of a central arbitration function. CUBITs will request bus access, and the central Bus Arbiter will grant access back, in response. The circuitry for this Bus Arbiter is included inside the CUBIT device. Any one CUBIT in a system may be selected to perform the bus arbitration function.

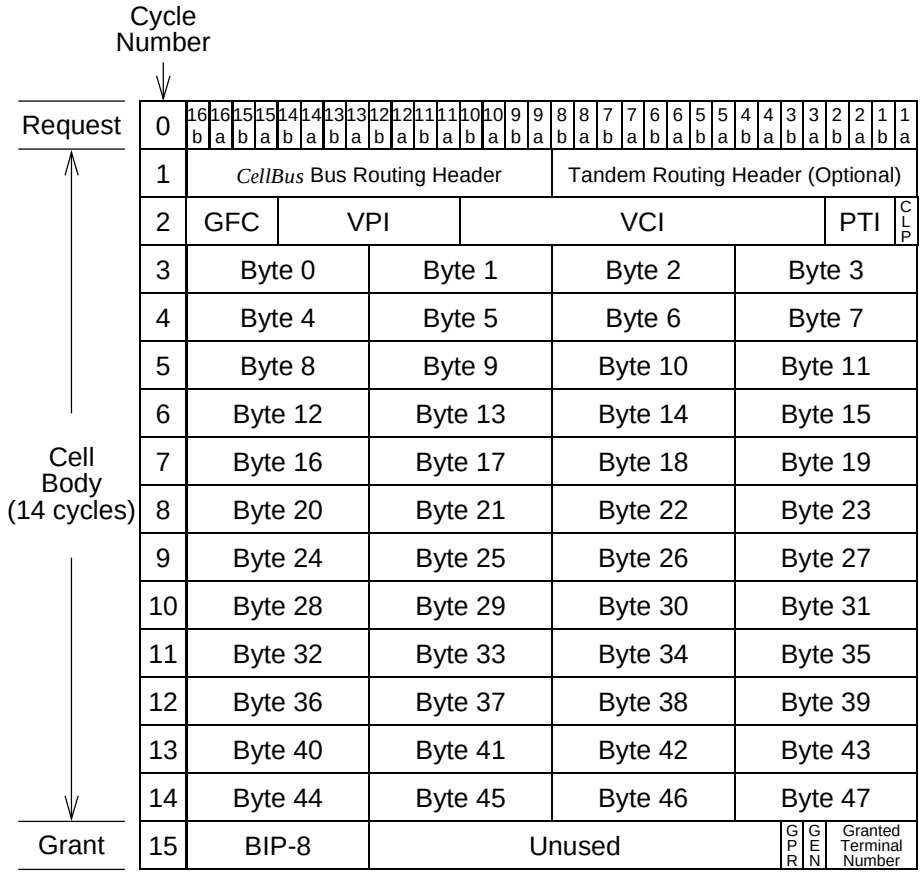


Figure 3. *CellBus* Bus Frame Format

CellBus bus has a framed format 16 clock cycles long and 32 bits wide, which is illustrated in Figure 3. The first cycle of each frame is the Request cycle (Cycle 0), during which those CUBITs which have a cell to send to the bus each make an access request by asserting one or two assigned bits on the bus. The device address assigned to each CUBIT by device straps ($\overline{UA}$(4-0) at pins 2-6) uniquely specifies which two bits it may assert during the bus Request cycle time. By asserting one of its assigned bits, or the other, or both, access requests of three different priorities may be made. A central Bus Arbiter accepts these access requests, executes an arbitration algorithm, and issues a bus access grant during the final cycle of the frame, the Grant cycle (Cycle 15). Each grant issued by the arbiter is for one CUBIT to send one cell to the bus. Whichever CUBIT is issued a grant during one cell will transmit its cell during the 14 Cell Body clock cycles of the next bus frame, and will also drive an 8-bit cell parity check during the Grant cycle of the same bus frame. Each cell sent can be of unicast, multicast, or broadcast type. CUBITs will accept single-address cells routed to an address defined by their address straps, all broadcast cells, and selected multicast cells. Thus, cells may be sent from any one CUBIT to any one CUBIT or to multiple CUBITs.

To detect *CellBus* bus errors, a BIP-8 (Bit Interleave Parity byte) is calculated over the 54-byte data field that extends from the first Tandem Routing Header byte through the final payload data byte, Byte 47. The BIP-8 is generated by the transmitting CUBIT using the following algorithm. The first byte of the Tandem Routing Header is exclusive-or gated with an all-ones byte, creating a starting seed value. This seed value is then exclusive-or gated with the second byte of the Tandem Routing Header. The result is then exclusive-or gated with the next byte in the cell. This process is repeated with every successive byte in the cell, through Byte 47 of the payload, and the final result is transmitted as the BIP-8 byte in cycle 15. The receiving CUBIT performs the same process and compares the generated BIP-8 with the received BIP-8. If no errors are detected the receiving CUBIT pulls $\overline{CBACK}$ low, acknowledging receipt of a cell. The *CellBus* Bus Routing Header has its own CRC-4 field and is not included in the BIP-8 calculation.

The only signals required to operate the bus which are not sourced by a CUBIT device are two transfer clocks: write clock ($\overline{\text{CBWC}}$), and read clock ($\overline{\text{CBRC}}$). These clock signals are of the same frequency, but may be slightly phase-offset to allow for reliable bus operation. The framing pulse used to define the bus frame cycle is sent out by one of the CUBITs, and the arbitration function is also performed by the same CUBIT. Each CUBIT contains the circuitry for both the Bus Arbiter and the Frame Pulse Generator. Only one CUBIT will have this circuitry enabled, by setting a control pin on the device.

CellBus Bus Address Coding

The encoding rules for the two-byte *CellBus* Bus Routing Header in Bits 31-16 of Cycle 1 are summarized in Figure 4.

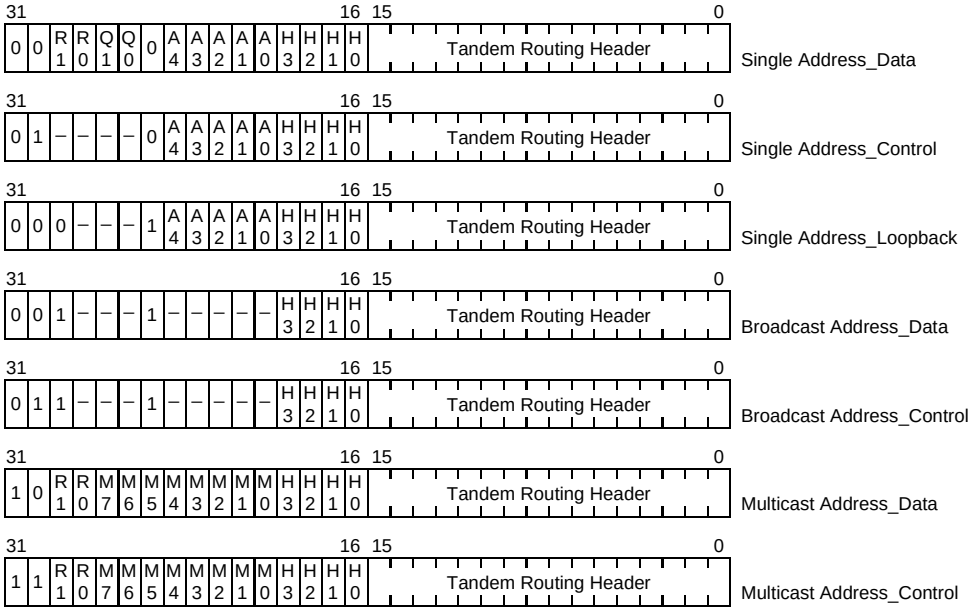


Figure 4. *CellBus* Bus Routing Header Formats

CellBus Bus Routing Header Format

The *CellBus* Bus Routing Header contains the following fields, as shown in Figure 4:

R: Multi-Phy selector field (2 bits). Not interpreted by CUBIT currently (passed through intact). This field is ignored.

Q: Queue selection field (2 bits). 00 is outlet control queue, 01 is Constant Bit Rate (CBR) queue, 10 is Variable Bit Rate (VBR) queue, 11 is Available Bit Rate (ABR) queue.

A: CUBIT single address field (5 bits, for 32 addresses). A0 is the LSB.

M: Multicast number field (8 bits, for 256 multicast sessions). M0 is the LSB.

H: CRC-4 field. This field is terminated by the CUBIT device. It is used for error protection across the *CellBus* bus. The calculation of the CRC-4 field (H3-H0) over the 12-bit word (X11-X0) in bits 31-20 must be performed external to the CUBIT using the following logic:

$$H3 = \overline{(X7 \oplus X9 \oplus X3 \oplus X10 \oplus X8 \oplus X5 \oplus X2)}$$

$$H2 = (X6 \oplus X8 \oplus X2 \oplus X9 \oplus X7 \oplus X4 \oplus X1)$$

$$H1 = \overline{(X5 \oplus X7 \oplus X1 \oplus X8 \oplus X6 \oplus X3 \oplus X0)}$$

$$H0 = (X8 \oplus X10 \oplus X11 \oplus X4 \oplus X9 \oplus X6 \oplus X3 \oplus X0)$$

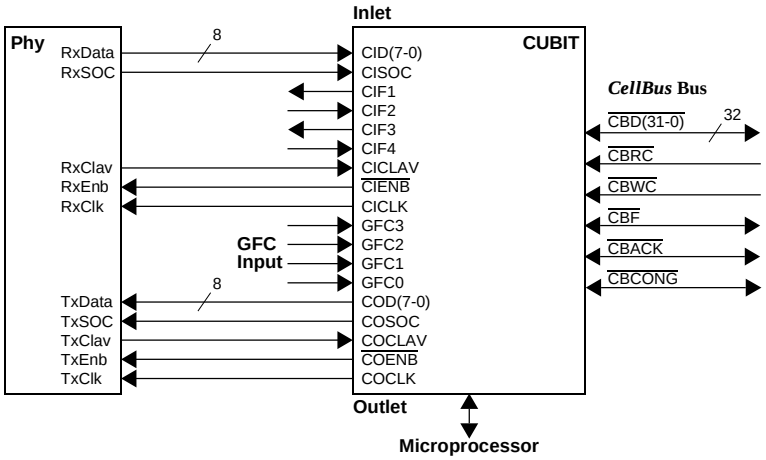
where $\oplus$ represents logical exclusive-or.

Tandem Routing Header Format

The two-byte Tandem Routing Header format in Bits 15-0 of Cycle 1 is the same as the *CellBus* Bus Routing Header format, if it is to be used by a cascaded *CellBus* bus, or may conform to a different specification if it is used by another system.

CUBIT CELL INLET AND OUTLET PORTS

UTOPIA Mode



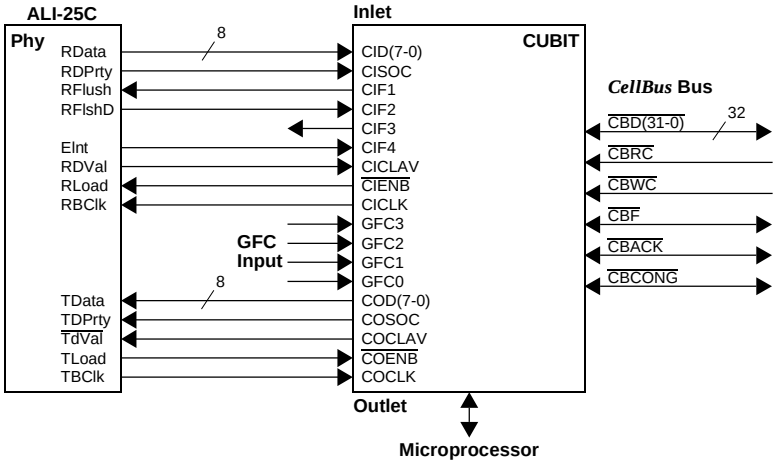
TRAN	LMODE1	LMODE0	Operating Mode: Inlet	Operating Mode: Outlet
High	X	High	UTOPIA, 57 bytes: cell plus *CellBus* Bus Routing Header plus two bytes of Tandem Routing Header	UTOPIA, 53 byte cell
High	High	Low	UTOPIA, 57 bytes: cell plus *CellBus* Bus Routing Header plus two bytes of Tandem Routing Header	UTOPIA, 55 bytes: cell plus Tandem Routing Header
Low	High	High	UTOPIA, 53 byte cell	UTOPIA, 53 byte cell
Low	High	Low	UTOPIA, 53 byte cell	UTOPIA, 55 bytes: cell plus Tandem Routing Header

Note: High = V_{DD5} = +5V; Low = V_{SS} = Ground; X = Don't Care

Figure 5. UTOPIA Mode Signal Connections and Operating Mode Selection

The CUBIT cell I/O supports the ATM Forum UTOPIA (Universal Test and Operations Physical Interface for ATM) interface standard and its extensions. Typical signal connections for the CUBIT when operating in UTOPIA mode are illustrated in Figure 5. The operating mode options for UTOPIA mode are controlled by the input pins TRAN, LMODE1 and LMODE0, as indicated in the table of Figure 5. When internal translation is used, the cell I/O is exactly that defined by UTOPIA, with 53-byte inlet cells. For applications in which the internal translation function is not used, the timing and logical flow of the cell I/O is still identical to that of UTOPIA, except that 57-byte inlet cells are used, instead of 53. The additional bytes are the Routing Header bytes which would be inserted by the CUBIT if the translation function were used, but are instead added by an external translation function. The different inlet and outlet byte counts per cell in the various modes are shown in the table of Figure 5.

ALI-25 Mode

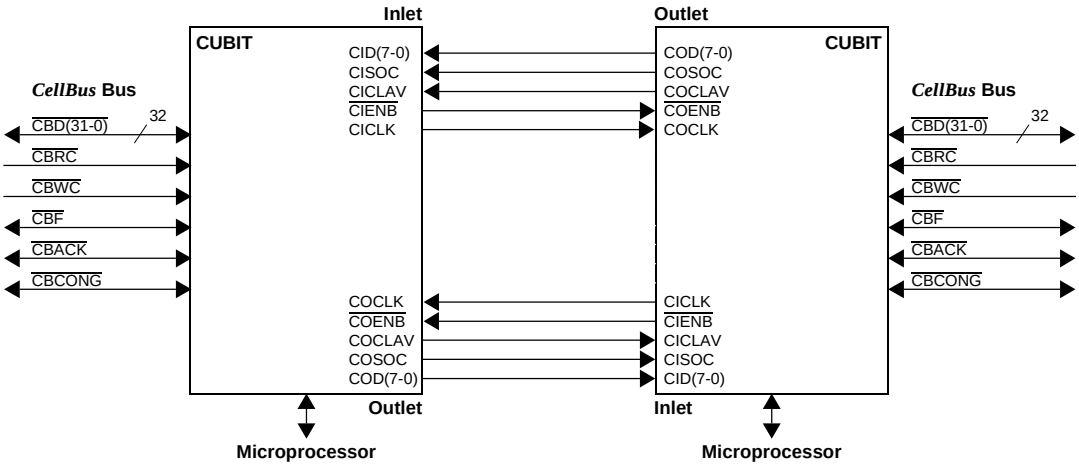


TRAN	LMODE1	LMODE0	Operating Mode: Inlet	Operating Mode: Outlet
Low	Low	High	ALI-25: 53 byte cell	ALI-25: 53 byte cell

Figure 6. ALI-25 Mode Signal Connections and Operating Mode Selection

The CUBIT supports the ALI-25 interface devices, and connects directly to the ALI-25C with no glue logic, as shown in Figure 6. In ALI-25 mode there is always translation, because the ALI-25C device cannot produce a *CellBus* Bus Routing Header or Tandem Routing Header. Two exception conditions in the ALI-25C are supported through CUBIT pins CIF1, CIF2 and CIF4. The output pin CIF1 connects directly to the RFlush input pin of the ALI-25C. If, due to an error condition in the ALI-25C, RDVal is unexpectedly de-asserted at its CICLAV input, the CUBIT will assert CIF1 to flush the ALI-25C and declare a start-of-cell (SOC) error. The ALI-25C uses its RFlshD output pin to acknowledge via the CUBIT's CIF2 input pin that the flush was completed. The second exception condition accommodated is the flagging of a HEC error by the ALI-25. If a HEC error is found, the ALI-25C asserts its EInt output pin, which drives the CIF4 input pin of the CUBIT and causes it to increment its HEC Error Counter.

Back-to-Back Mode



TRAN	LMODE1	LMODE0	Operating Mode: Inlet	Operating Mode: Outlet
High	Low	Low	Back-to-Back: 55 bytes, cell plus two bytes of *CellBus* Bus Routing Header	Back-to-Back: 55 bytes, cell plus two bytes of Tandem Routing Header
Low	Low	Low	Back-to-Back: 53 byte cell	Back-to-Back: 53 byte cell

Figure 7. Back-to-Back Mode Signal Connections and Operating Mode Selection

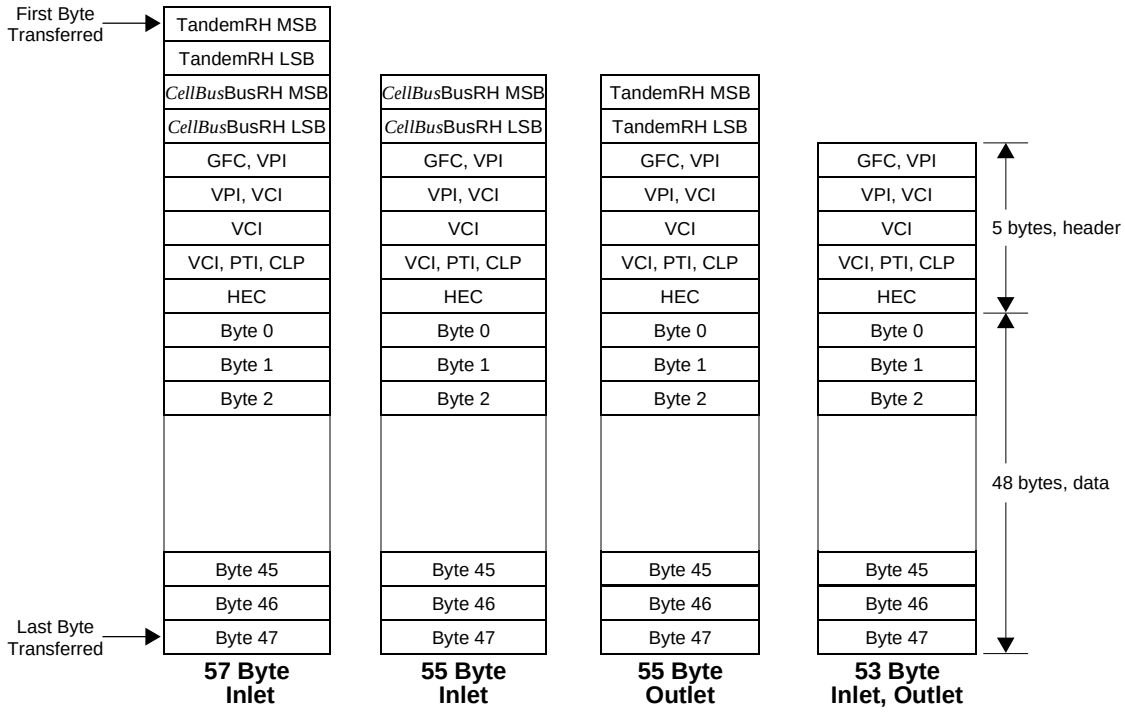
The Back-to-Back mode is used to support interconnection of two *CellBus* buses, as shown in Figure 7. If pin TRAN is low, each of the CUBITs has a translation memory connected, the cell address translation function is active, and the cells in and out are 53 bytes long. If TRAN is high, the translation function is not used. The transfers in and out will be 55 bytes long. The cell out of the outlet will carry two extra bytes which are the Tandem Routing Header from the *CellBus* bus. These two bytes are presented to the inlet port of the connected CUBIT, which uses them as a *CellBus* Bus Routing Header when it puts the cell on the bus.

In order to avoid re-transmission of multicast or broadcast cells from one *CellBus* bus to another, and back again, a CUBIT which is operating in the Back-to-Back mode will reject all incoming broadcast and multicast cells which originated from its own inlet side.

The timing of this mode is similar to UTOPIA mode, except that the directionality of the COCLAV, COENB and COCLK signals is reversed, as shown in the connections diagrams of Figures 5 and 7.

Byte Ordering for UTOPIA, ALI-25 and Back-to-Back Modes

Byte ordering for the three cell inlet and outlet alternatives described above is illustrated in Figure 8.



Note: RH = Routing Header

Figure 8. Byte Ordering on Cell Inlet and Outlet in UTOPIA, ALI-25 and Back-to-Back Modes

16-Bit Cell Interface Mode

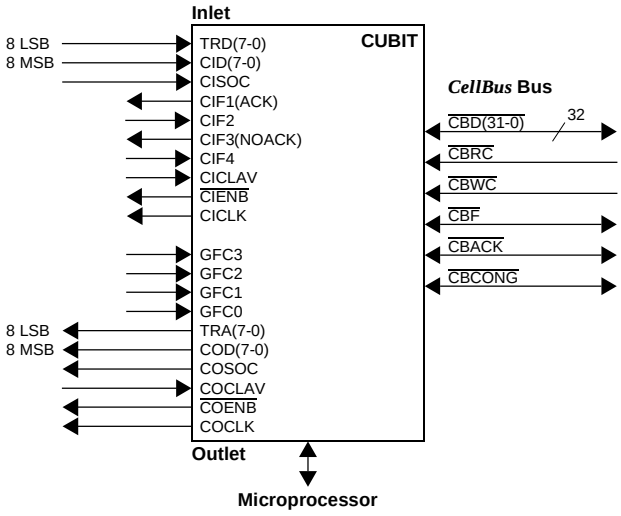


Figure 9. 16-Bit Cell Interface Mode Signal Connections

16-Bit Cell Interface mode is enabled by device strap pin $\overline{\text{ABRENA}}$, regardless of the settings of $\overline{\text{TRAN}}$, $\overline{\text{LMODE1}}$ and $\overline{\text{LMODE0}}$. The timing of this mode is identical to that of the UTOPIA mode, but the data width is expanded to a word of 16 bits in and out. The translation RAM is not used in this case. The extra 8 inlet bits are connected to the pins used for the data of the translation RAM, TRD (7-0), and the extra 8 outlet pins are the pins for the 8 LSB of the translation RAM address output, TRA (7-0). These signal connections are illustrated in Figure 9, and the 16-Bit word ordering is shown in Figure 10.

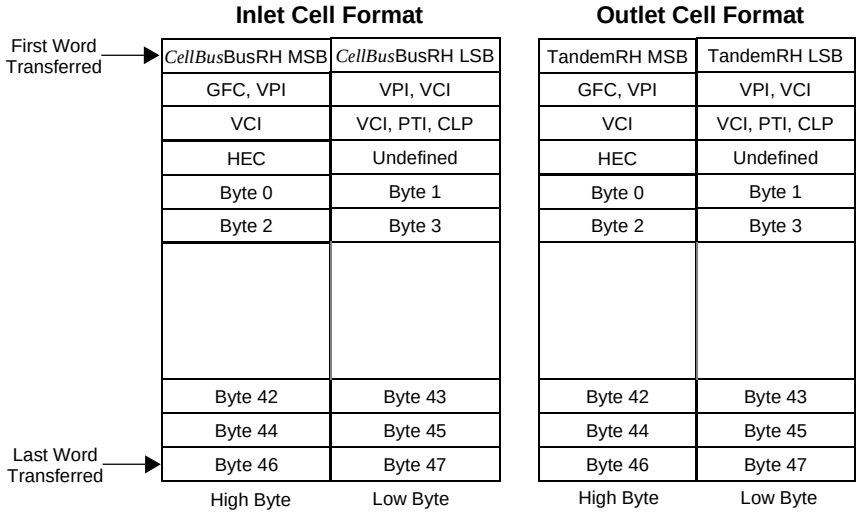


Figure 10. Word Ordering in 16-Bit Cell Interface Mode

TRAFFIC MANAGEMENT FUNCTIONS

Dynamic Generic Flow Control (GFC) Field Insertion

The CUBIT can insert the value of the first nibble of the ATM cell header in real time. The value of the GFC nibble is supplied to the CUBIT via the input pins GFC(3-0). The insertion of the GFC value is enabled via the control bit GFCENA.

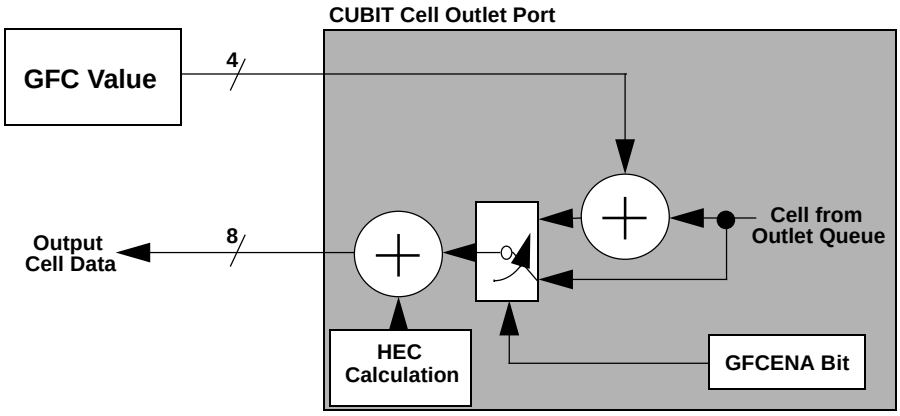


Figure 11. GFC Insertion on the Outlet Queue (GFCENA = 1)

If control bit GFCENA (Control Register Address 0CH, Bit 1) is set to one, then the state of the four Generic Flow Control input pins GFC(3-0) will be accepted during the leading rising edge of the first byte of the ATM cell header and inserted as an outgoing GFC on the following cell (see timing diagram in Figure 36 for details). Therefore the GFC value is inserted into the next outgoing cell.

Forward Explicit Congestion Notification (EFCN)

The CUBIT can notify an impending congested state by setting to one the middle bit of the Payload Type (PT) field in the ATM cell header. This sets an Explicit Forward Congestion Indication (EFCI) in the cell header which notifies the end-user of an upstream congestion situation.

The Explicit Forward Congestion Indication bit (PT middle bit in the ATM cell header) will be asserted on a cell if two conditions occur:

a) Bit 1 in register 0Ch is set to one (IFECN = 1), and

b) QM=0 and VBR Limit reached, or QM=1 and VBR Limit or CBR Limit reached.

Selective Cell Discard

In the event of congestion in the outlet queue of the CUBIT, cells marked with CLP=1 can optionally be discarded. This feature is enabled when bit 3 in address 0Ch is set to one (DISCARD=1).

If selective discarding is enabled (DISCARD=1) two scenarios may take place depending on whether single-queue, or split-queue mode is selected using bit 2 in address 0Ch (QM). In single queue mode (QM=0) the congestion size of the queue is determined by the value of VBRLIMIT. If the outlet data queue contains a number of cells equal or greater than VBRLIMIT, any cell coming from the *CellBus* bus with CLP=1 will be discarded if DISCARD=1. Discarded cells are counted in the DISCCTR counter. Cells with CLP=0 will be sent to the outlet data queue.

In split-queue mode (QM=1), only cells marked as VBR traffic (Q1-Q0 bits in the *CellBus* Bus Routing Header are equal to 10) are subject to selective discarding. Similarly, as in the single queue mode, if the VBR outlet queue is congested (i.e., the number of cells in the VBR queue is greater than or equal to the value in VBRLIMIT), VBR-marked cells with CLP=1 will be discarded and counted in DISCCTR.

Paralleling Cell Inlet/Outlet Ports for Redundancy

If the control bit ONLINE (Control Register Address 0CH, Bit 7) is set to zero, then all of the CUBIT cell outlet interface output pins will be taken to the high impedance (Hi-Z) state and the cell inlet data input pins will be disabled. Thus two CUBITs may be paralleled for redundancy, each connected to a separate *CellBus* bus. Cells will only be accepted from or sent to the line by the CUBIT in which ONLINE = 1.

INLET-SIDE TRANSLATION

Introduction

The translation function on the inlet side operates using information stored in an external static RAM, and can provide the following functions:

Virtual Path Identifier (VPI) translation or

VPI/VCI translation (where VCI is Virtual Circuit Identifier), and

CellBus Bus Routing Header insertion, and

Tandem Routing Header insertion, and

F4 flow cell routing, and

F5 flow cell routing.

All translation operations start by performing a translation table lookup based on the VPI number of the incoming cell. Within the routing table record for that VPI is control information for that VPI, indicating whether cells are to be routed based on VPI number alone or on VPI and VCI.

If VPI-only routing is selected, a translated VPI number, accompanied by *CellBus* bus and Tandem Routing Headers, is retrieved from the translation record for that VPI. In this case, the VCI number of the incoming cell is not changed. When VPI translation is selected, separate routing for F4 OAM flow cells on that VPI can be programmed, allowing selective handling of these OAM cells by a *CellBus* bus system.

If the VPI is instead programmed for VCI translation, then a two-step procedure is used to accomplish the translation. The VPI record, accessed first, indicates the size and position in memory of the VCI translation table. Using this information, and the VCI address of the cell, a VCI translation record is accessed. This translation record contains the VPI and VCI numbers to be assigned to the cell, along with the *CellBus* bus and Tandem Routing Headers. When VPI/VCI translation is selected, separate routing for F5 OAM flow cells on that VCI can be programmed, allowing selective handling of these OAM cells in a manner similar to that of F4 cells.

In both cases, the cells with the translated headers and *CellBus* bus and Tandem Routing Headers are forwarded to the bus in sequential order. Translation does not add delay to cells passing through the inlet side to the *CellBus* bus.

Translation RAM Connections

The Translation RAM (TRAM) may be a single 32k x 8 or 64k x 8 device, or two 32k x 8 Static RAMs (SRAMs) connected as shown in Figure 12. The TRAM access time requirement is dependent upon the *CellBus* bus clock speed (see Figure 26). An access time of 35 nanoseconds or less will support the maximum *CellBus* bus speed.

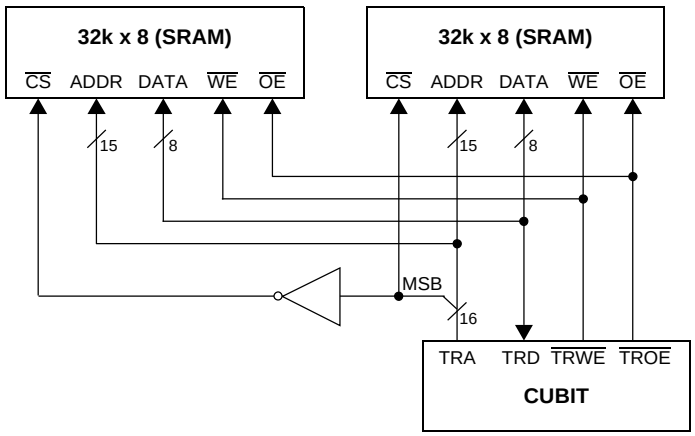


Figure 12. Translation RAM Connections

Translation RAM Control

When the CUBIT device is configured to perform translation (input pin $\overline{\text{TRAN}}$ low), it replaces received values of VPI or VPI and VCI numbers with new values, and adds Routing Headers to the cells forwarded to the *CellBus* bus. The VPI/VCI number and Routing Header information that is inserted comes from translation record entries in the TRAM. The TRAM is organized into a block of VPI records and a block of VCI records, the contents of which are established by system control.

Memory Organization

The translation RAM partitioning is shown in Figure 13.

The lower portion of the TRAM contains the translation records for VPIs. When the UNI mode is enabled (control bit UNI=1), the number of VPI entries is 256. When NNI mode is enabled (UNI=0), 4096 VPI entries are present. For each VPI number, either four or six bytes are allocated in each VPI translation record: four if the Tandem Routing Header (TRH) is not used (control bit TRHENA=0), six if the TRH is used (TRHENA=1). The size of the VPI memory space ranges from 1024 bytes (UNI mode, no TRH, 4x256) to 24576 bytes (NNI and TRH, 6x4096).

The memory space above the VPI section is the VCI translation record storage space, divided into a number of VCI pages. Each VCI page contains the translation records for 256 VCIs. Each VCI translation record is six bytes, without TRH, or eight bytes, with TRH.

The total size of the TRAM which the CUBIT can support is up to 65536 bytes (64k). Hence, the number of VCI translation table pages which can be supported is a function of memory size, and the states of control bits UNI and TRHENA. For example, the maximum number of VCI memory pages, for maximum memory size, is as follows:

if UNI=1, TRHENA = 1; VCI pages = (65536-(256*6))/(256*8)=31,

if UNI=1, TRHENA = 0; VCI pages = (65536-(256*4))/(256*6)=42.

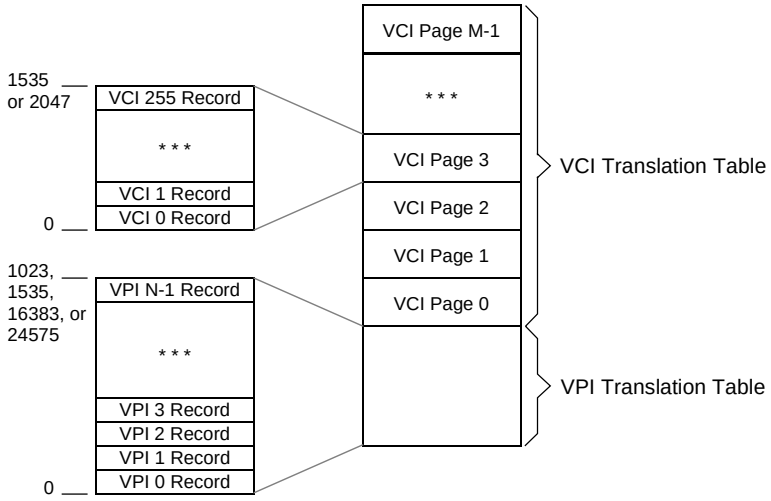


Figure 13. Translation RAM Organization

Translation Procedure

Translation is done in a two-step procedure, starting with examining the incoming VPI number. A full 8-bit (UNI=1) or 12-bit (UNI=0) VPI number may be used. The incoming VPI number is used to address a VPI translation record. If the translation is to be done on VPI only, leaving the VCI number intact, then the VPI number and routing header are contained in the VPI translation record. If VPI and VCI translation is to be done, then the VPI record contains a pointer to the location of one or more "pages" of VCI translation records. Each "page" is a set of translation records for 256 consecutive VCI numbers. Up to fifteen such VCI pages may be assigned to any VPI. The only restriction is that the VCI pages for each VPI must be assigned in consecutive VCI address space from zero upwards. Within this assigned space, the VCI number of the incoming cell is used to address a particular VCI translation record containing the new VPI and VCI numbers and the routing header.

VPI Translation Record Formats

VPI translation records are four bytes long if TRHENA=0, or six bytes long if TRHENA=1, as shown in Figure 14. Each VPI may be either idle or busy. If it is busy, then each VPI may be set for VPI-only translation, or for combined VPI/VCI translation. The control bits (A, P, E and I) and Routing Headers are described below.

VCI Translation Record Formats

VCI translation records are six bytes long if TRHENA=0, and eight bytes long if TRHENA=1, as shown in Figure 15. Each VCI may be either idle or busy. The corresponding formats for OAM translation records are shown in Figure 16.

Control Bits

Four control bits, labelled as A, P, E and I, are used in byte 0 of translation records, as described below:

Active (A) Bit:
If the A bit is set to one in a translation record, then that VPI or VCI is active. Cells received with this VPI or VCI will be translated and forwarded to the bus, unless bit I is set to one. If A=0, then cells received on this VPI or VCI will be considered misrouted, unless I=1.

VPI Translation Enable Bit (P):
If this bit is one in a VPI translation record, then a VPI-only translation is made. If it is set to zero, a combined VPI and VCI translation is made.

OAM Cell Routing Bit (E):
If bit E is set to one in a VPI record, then VCIs numbered 0 through 15 of that VPI will be routed according to OAM records contained in record numbers 0 through 15 of VCI page zero. If bit E is set to one in a VCI record, then cells of that VPI having the MSB of their PTI (Payload Type Indicator, in cell header) set to one will be routed according to a VCI translation record contained in record number 16 of VCI page zero.

Ignore Bit (I):
If a VPI is marked Active (A=1), and the Ignore bit is also set active (I=1), then incoming cells bearing this VPI number are discarded, but are not counted as misrouted cells.

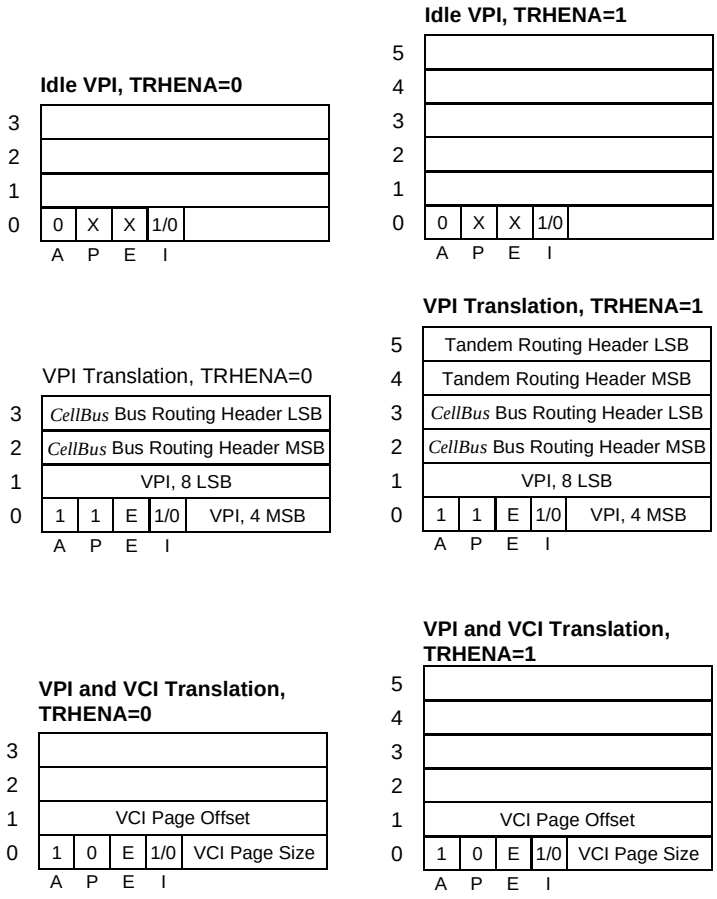
CellBus Bus Routing Header

The *CellBus* Bus Routing Header is a 16-bit structure, which is formatted as described in the *CellBus* Bus Address Coding subsection above. Additional detail is provided in Appendix A of "*CellBus* Technical Manual and Cubit Applications", TranSwitch document number TXC-05801-TM1.

Tandem Routing Header

If the Tandem Routing Header is to be used as a *CellBus* Bus Routing Header, as when passed through a CUBIT in back-to-back mode, it must follow the same construction rules as a *CellBus* Bus Routing Header. If the Tandem Routing Header is used for some proprietary purposes, its format will follow a different specification.

Figure 14. VPI Translation Record Formats

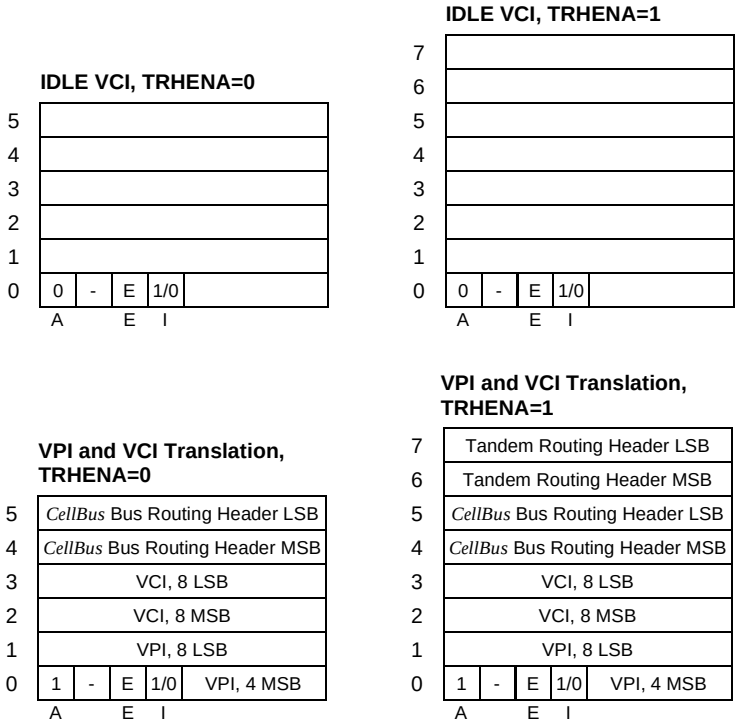


If the VPI is unused, then the MSB (Active bit, A) of relative address zero is set to zero, indicating idle. If a cell arrives with this VPI number, it is discarded and is counted as a misrouted cell.

If the VPI is busy and is to have VPI number translation only, then the A bit is set=1, and the P bit is set=1. In this case, the VPI to be inserted on the cell is contained in the 4 LSB of relative address zero (4 MSB of new VPI), and in relative address one (8 LSB of new VPI). *CellBus* Bus and Tandem Routing Headers are also contained in the next two or four bytes.

If the VPI is busy and is set for combined VPI/VCI number translation, a reference is generated to a VCI translation record. The VPI is set active (A=1), and is set for VCI translation (P=0). The 4 LSB of relative address zero contain the VCI Page Size, which is the number of assigned VCI pages, each of 256 VCI records, allocated to this VPI. Relative address one contains the VCI Page Offset, which indicates where among the VCI pages the first utilized page starts.

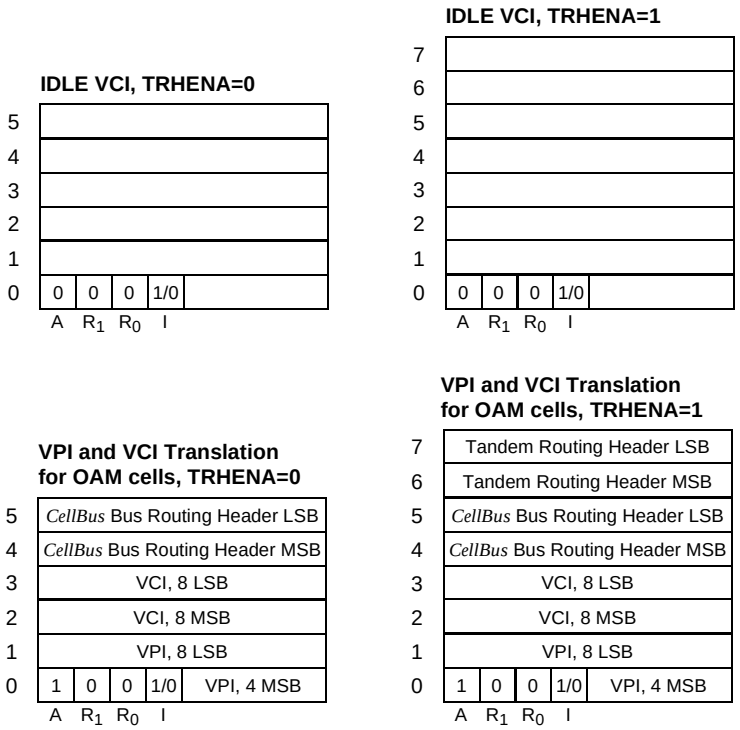
Figure 15. VCI Translation Record Formats



If the VCI is inactive (A=0) and not Ignore (I=0), then cells arriving bearing that VCI number are discarded and counted as misrouted. If I=1, they are discarded and not counted as misrouted.

If the VCI is active (A=1), then the VPI and VCI numbers to be inserted in the cell, and the *CellBus* Bus Routing Header to be used, are read from the VCI translation record at the positions indicated.

Figure 16. OAM Translation Record Formats



If the VCI is inactive (A=0) and not Ignore (I=0), then OAM cells arriving bearing that VCI number are discarded and counted as misrouted. If I=1, they are discarded and not counted as misrouted.

R_1 and R_0 are bits reserved for functions that will be implemented in the future. They must be set to "00" for correct operation.

If the VCI is active (A=1), then the VPI and VCI numbers to be inserted in the cell, and the *CellBus* Bus Routing Header to be used, are read from the OAM translation record at the positions indicated.

Note: OAM Translation Records are optional. They are located in VCI page zero.

OAM/Reserved-VC Routing

The routing scheme for special cells is algorithmically depicted in Figures 17 and 18. Figure 17 depicts the routing mechanism for cells with PTI = 1xx, which correspond to F5-flow type cells.

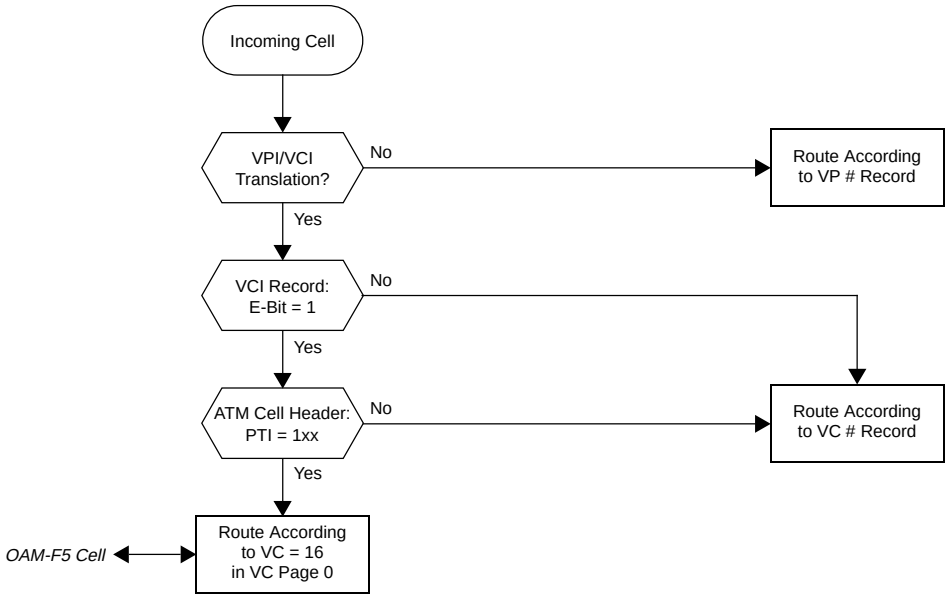


Figure 17. OAM F5 Cell Routing Mechanism

The CUBIT routes all F5-flow cells (if E-bit = 1 in the VC record) according to a single translation record located in entry 16 of VC Page 0.

In Figure 18, the routing scheme for cells with reserved VCs from 0 to 15 is presented. Cells with reserved VCs 0..15 are routed according to Records 0..15 in VC Page 0 (if E-bit = 1 in the VP record). Therefore, all VPs are routed based on the same table for that particular VP.

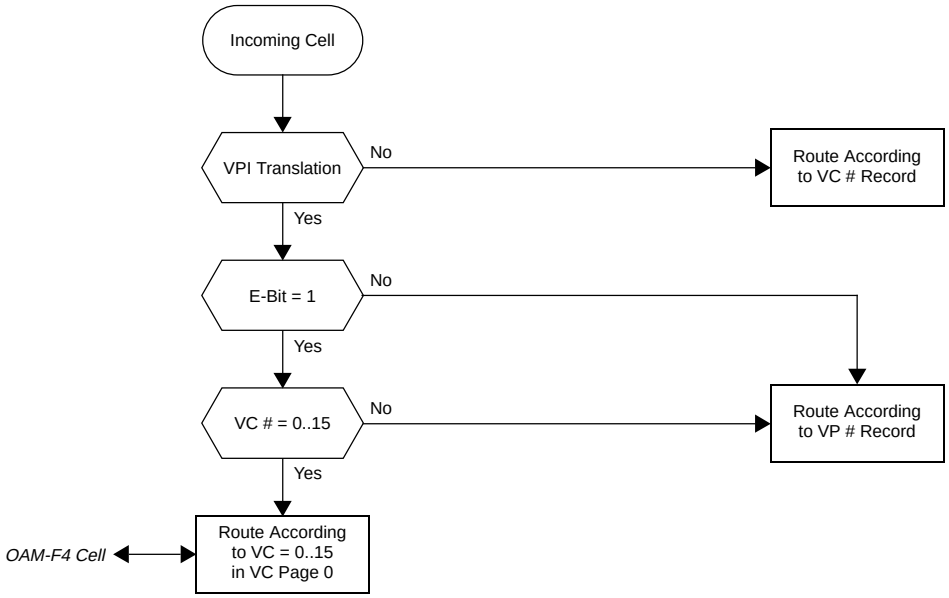


Figure 18. OAM-F4 and Reserved VCs Cell Routing Mechanism

The memory organization required with the algorithms in Figures 17 and 18 is given in Figure 19.

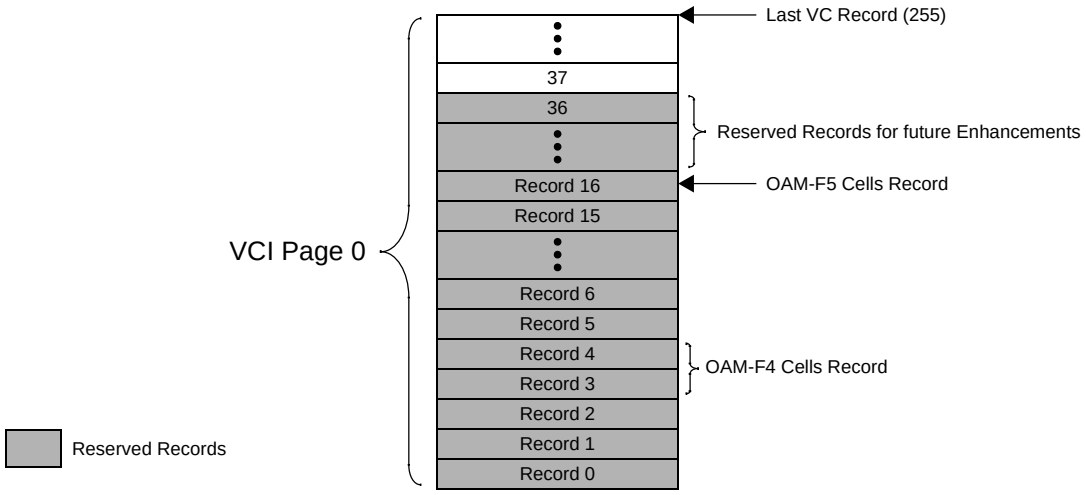
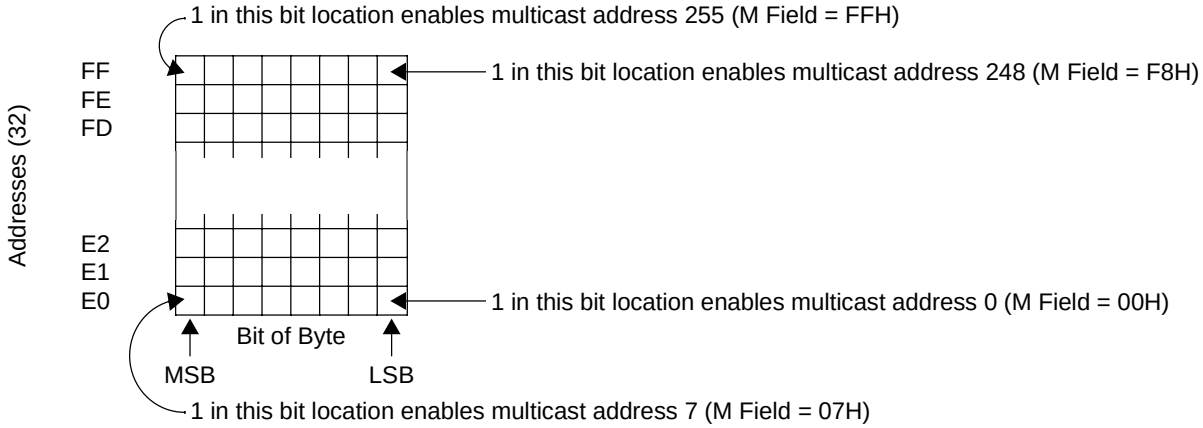


Figure 19. Memory Organization (VCI Page 0) for CUBIT

MULTICAST NUMBER MEMORY

A multicast address control cell or multicast address data cell can be sent to a number of CUBITs, and a single CUBIT can receive cells with a number of different addresses. This is controlled by the setup of the Multicast Number Memory (addresses E0H-FFH in the CUBIT memory map), which is a block of 32 bytes. Each of the 256 bits in the block maps to one multicast address, as shown in Figure 20. When a bit is set to 1, the CUBIT is enabled to receive the corresponding multicast address cell. Each CUBIT can be set to receive any or all of the 256 possible multicast addresses.



Note: The M Field refers to the *CellBus* Bus Routing Header for Multicast Address cells (see Figure 4).

Figure 20. Multicast Number Memory

THE *CellBus* Bus INTERFACE

Thirty-seven lines comprise the *CellBus* bus interface, as shown in Figure 2. There are thirty-two Data lines, with Frame, Acknowledge, and Congestion Indicator lines, all sourced by a CUBIT device, and two Clock lines sourced by external drivers.

Operation with Internal GTL Transceivers

Gunning Transceiver Logic (GTL) transceivers for *CellBus* bus Data, Frame, Acknowledge, and Congestion Indicator lines are contained internally in the CUBIT, along with two clock line GTL receivers. Each of the drivers has a maximum current sink capability of 48 mA and is capable of driving a bus on a card or on a backplane directly. Each of the GTL lines is to be pulled-up at each of its ends by a 50 ohm (+/- 5%) resistor (metal film or carbon composition) to a +1.2 V low-impedance supply. Each end of each line should have a filtering capacitor connected from the +1.2 V supply to ground, as shown in Figure 21.

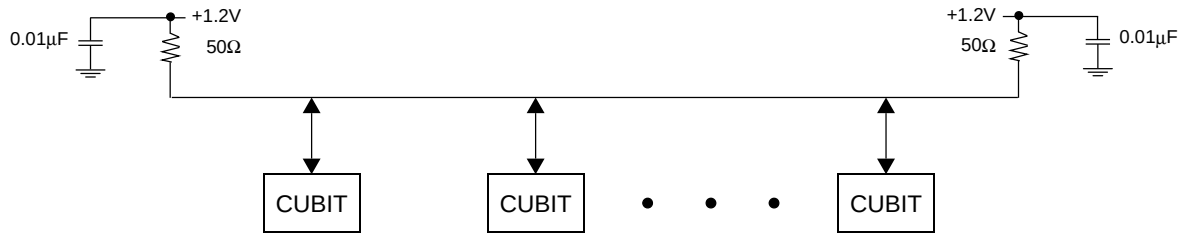


Figure 21. External Circuit Requirements for GTL Transceivers

In the CUBIT pinout, all of the pins involved with the bus interface are aligned along one side of the package between pins 50 and 112. This side of the package must be aligned toward the board connector, or toward the bus, with as little board trace length as possible between the pins and the connector or bus, to maximize operating speed.

Clock Source

Two GTL-level clock signals must be driven to the *CellBus* bus from an external source. These are the write clock, $\overline{\text{CBWC}}$, and the read clock, $\overline{\text{CBRC}}$. A phase relationship keeping the write clock between 0.5 and 4 nanoseconds behind the read clock is needed to ensure proper synchronous bus operation. When the clock driver is driven from the center of the backplane (i.e., no greater than half a backplane length from any card) a minimum phase distance of 0.5 ns or more must be maintained. When the driver is at one of the ends, a more conservative 2-4 ns minimum is required. In any *CellBus* bus implementation, on the backplane and on each card, care must be taken to ensure that these two lines are routed together. The capacitive and inductive loadings of the two lines should be as nearly equal as possible, to maintain performance. At the drive point, a delay line should be used to maintain a stable delay, and the read and write clock drivers must be units of the same integrated circuit package. All of these precautions will ensure the most stable clocks and permit the highest possible operating speed.

Bus Arbiter Selection

One copy of the *CellBus* bus Arbiter circuitry is included inside each CUBIT device. Enabling of the arbiter on a particular CUBIT is done by connecting the $\overline{\text{ENARB}}$ pin of that device to ground (V_{SS}). Normally, one arbiter is turned on and the remaining arbiters on that bus are turned off. It is the responsibility of the overall system control to decide which CUBIT will have its arbiter enabled, and to enable it. Failure of an arbiter can be detected by using the NOGRT indications. If multiple CUBITs are indicating NOGRT failures, an arbiter failure is indicated. It is again the responsibility of system control to enable another arbiter.

Upon switching from one arbiter to another, the receiving devices on the bus will automatically re-align to the new frame position within one *CellBus* bus frame.

OUTLET-SIDE QUEUE MANAGEMENT

The CUBIT contains a 123-cell queuing FIFO for data on its outlet side. This FIFO may be operated as a single 123-cell FIFO, or it may be split into four independent FIFOs.

Single Queue Operation

If control bit QM at Address 0CH, Bit 2 is zero, then the outlet has a single 123-cell FIFO. This mode is appropriate when a single type of traffic is to be switched by the system. In this case cell congestion, for purposes of causing a FECN (if enabled by control bit IFECN at Address 0CH, Bit 0), is established by the register VBRLIMIT at Address 12H.

Split-Queue Operation

If QM = 1, the outlet FIFO is split into 4 separate queues. These are, in order of service priority, Control (highest priority), CBR, VBR, and ABR. The Control cell queue is fixed in length at 2 cells, and the ABR queue at 32 cells. The congestion threshold on the ABR queue is set at 28. The size of the CBR queue is set by the contents of register CBRLEN at Address 10H, and its congestion point by CBRLIMIT at Address 11H. The remaining FIFO cells are assigned to the VBR queue. The length of the VBR queue is (123-2-32-CBRLEN = 89-CBRLEN), and its congestion limit is set by VBRLIMIT at Address 12H.

Note the differences between the control queue section of the split outlet queue, the control cell receive buffer and the control cell transmit buffer (all referred to as control queue):

1. The control queue section of the split outlet queue accepts cells from the *CellBus* bus that have a single address data routing header with the Q field set to 00 (see Figure 4).
2. The control cell receive buffer (address 60H-93H) accepts cells from the *CellBus* bus that have a single address control routing header (see Figure 4).
3. The control cell transmit buffer is loaded by the microprocessor with a cell to be sent to the *CellBus* bus. It can have any of the *CellBus* Bus Routing Header formats shown in Figure 4.

Dynamic Generic Flow Control (GFC) Field Insertion

If control bit GFCENA at Address 0CH, Bit 1 is set to 1, then the state of pins GFC(3-0) during the rising edge of COCLK is inserted into the GFC field of the next outgoing cell.

Forward Explicit Congestion Notification (FECN) Insertion

A Forward Explicit Congestion Notification bit (PTI middle bit set unconditionally to one) will be asserted on a cell if

a) IFECN = 1, and

b) QM=0 and VBR Limit reached, or QM=1 and VBR Limit or CBR Limit reached.

MICROPROCESSOR INTERFACE

General Description

The CUBIT Microprocessor Port will support an I/O interface characteristic of either Intel or Motorola microprocessors, as shown in Figure 22.

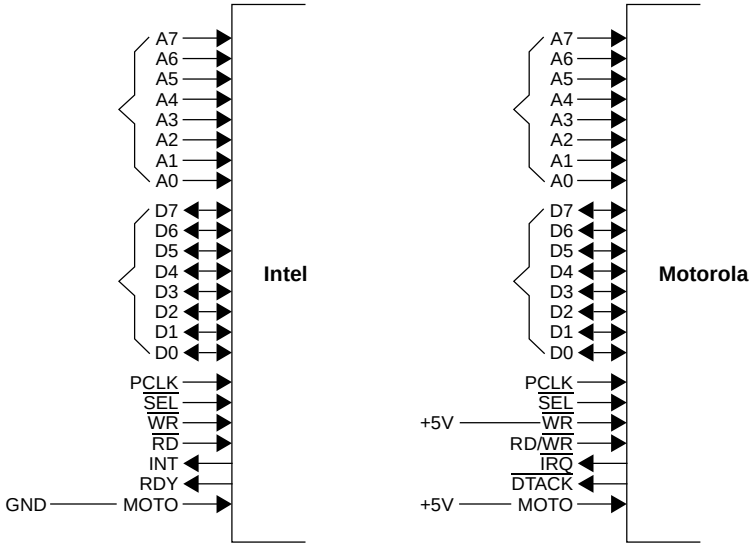


Figure 22. Microprocessor Port Interface Connections

The connections for address A(7-0), data D(7-0), select ($\overline{SEL}$) and processor clock (PCLK) are the same for both cases. Differences are listed below.

Intel Mode

Enabled when device strap MOTO is connected to V_{SS} (ground). Connections are as shown in Figure 22. The differences to support Intel mode are:

$\overline{WR}$ pin is low to execute a write command,

$\overline{RD}$ pin is low to execute a read command,

Interrupt INT is active high,

Ready RDY is active high. When set low, it requests microprocessor wait time.

Motorola Mode

Enabled when device strap MOTO is connected to V_{DD5} (+5V). Connections are as shown in Figure 22. The differences to support Motorola mode are:

$\overline{WR}$ pin is not used and must be pulled up to +5 volts,

RD/$\overline{WR}$ pin is high to execute a read command or low to execute a write command,

Interrupt $\overline{IRQ}$ is active low,

Data Transfer Acknowledge $\overline{DTACK}$ is active low. When inactive, and pulled high by an external pull-up resistor, it requests microprocessor wait time.

Interrupts

Eight events, OCOVF, OCDISC, NOGRT, CTSENT, INSOC, CRQCAV, CRQOVF, and CRCF, readable from the CUBIT status register at Address 08H, Bits 0 through 7, respectively, may cause interrupts if enabled. Each event may be enabled by setting to 1 an interrupt enable bit in Address 09H, located at the corresponding bit position. If an interrupt is not enabled, the status can still be read from the status register. When an event causes an interrupt, the INT pin will be driven to its active state. All the status bits in a register are cleared when it is read, except for any bits for which the events still persist. Some enabled interrupts may not be cleared in the absence of the *CellBus* bus clocks. Such interrupts will persist until the clocks are re-applied. It is possible, however, to mask any interrupt regardless of the absence or presence of the *CellBus* bus clocks. The events are described below, starting at bit position 0:

OCOVF Outlet Cell Overflow:

In the single queue mode an overflow will occur, and this bit will be set to 1, when more than 123 cells try to accumulate in the outlet queue.

In the split queue mode this overflow will occur if any of the following events occurs:

a. More than 32 cells try to accumulate in the ABR queue
b. More than CBRLEN (address 10H) cells try to accumulate in the CBR queue
c. More than (89 minus CBRLEN) cells try to accumulate in the VBR queue
d. More than 2 cells try to accumulate in the control queue.

OCDISC Outlet Cell Discarded:

In the single or split queue modes an outlet cell will be discarded, and this bit will be set to 1, if DISCARD (Address 0CH, Bit 3) is set to 1 and the CLP bit of the cell is 1 and more than VBRLIMIT (address 12H) cells try to accumulate in the outlet queue.

NOGRT No Grant:

If the CUBIT device has requested a *CellBus* bus grant and has not received it after the number of frames indicated by the TIME register (address 0FH), this bit will be set to 1.

CTSENT Control Cell Sent:

When the microprocessor requests that a control cell be sent to the *CellBus* bus, this bit will be set to 1 after the cell has been sent.

INSOC Inlet Start of Cell:

In the UTOPIA, 16-Bit Cell Inlet Interface, and Back-to-Back modes, if CISOC is not present in the same clock cycle that CICLAV is asserted and $\overline{\text{CIENB}}$ is asserted, or if CISOC is not present in the following cycle after $\overline{\text{CIENB}}$ is asserted (assuming that CICLAV was previously asserted when $\overline{\text{CIENB}}$ was de-asserted), or if CISOC is asserted before the end of the current cell, the INSOC bit is set to 1.

CRQCAV Control Receive Queue Cell Available:

When a control cell has been received from the *CellBus* bus and placed in the receive buffer (addresses 60H-93H) this bit will be set to 1. This bit is cleared to 0 after the microprocessor writes a 1 to CRQSENT.

CRQOVF Control Receive Queue Overflow:

An overflow will occur, and this bit will be set to 1, when more than four cells try to accumulate in the control receive queue.

CRCF CRC-4 Error:

If the CRC-4 field H(3-0) of the *CellBus* Bus Routing Header in a cell received from the *CellBus* bus does not match the calculated CRC-4, this bit is set to 1 (see Figure 4).

CONTROL CELL SEND AND RECEIVE

The formats of transmit and receive control cells are shown in Figure 23. Reference to Figure 1 will be helpful for understanding of this section.

A control cell can be sent from the microprocessor to the *CellBus* bus by using the control cell transmit buffer. This ability allows the microprocessor to send any type of data, control or loopback cell to any CUBIT on the *CellBus* bus. The microprocessor first writes a 56-byte transmit control cell with the format shown in Figure 23 to the control cell transmit buffer (Addresses A0H-D7H in the CUBIT memory map). Then a 1 is written to control bit CTRDY (Address 0AH, Bit 1). The cell will be sent to the *CellBus* bus after any pending data cells, and the CTSENT bit (Address 08H, Bit 3) will then be set to 1 and the CTRDY bit will be reset to 0. Another control cell send sequence may be started after CTSENT has been received. Note that the CRC-4 in the *CellBus* Bus Routing Header is not generated by the CUBIT and must be correctly loaded into the transmit buffer by the microprocessor.

A four-cell FIFO buffer is provided for reception of control cells from the *CellBus* bus, since control cells can arrive from several sources and may have to wait for the microprocessor to accept them from the CUBIT. The FIFO output is the 52-byte memory segment CRQ(51-0) at Addresses 93H-60H. When this segment acquires a received control cell the CUBIT sets its interrupt bit CRQCAV to 1 (Address 08H, Bit 5). This bit may be enabled to cause an interrupt to the microprocessor (by setting interrupt enable bit INTEN5 to 1 in Address 09H, Bit 5). When an interrupt or polling process causes the microprocessor to read the interrupt event register at Address 08H it will detect the CRQCAV indication that a control cell is available for reading. It must then read CRQ(51-0) and set control bit CRQSENT to 1 upon completion (Address 0AH, Bit 0). This notifies the CUBIT to reset CRQCAV to 0 and place the next control cell in CRQ(51-0), either immediately from the adjacent FIFO cell, if occupied, or whenever the next cell arrives in the FIFO from the *CellBus* bus. The CUBIT resets CRQSENT to 0.

Control cell transmission and reception may still be performed regardless of the state of control bit ONLINE (Address 0CH, Bit 7).

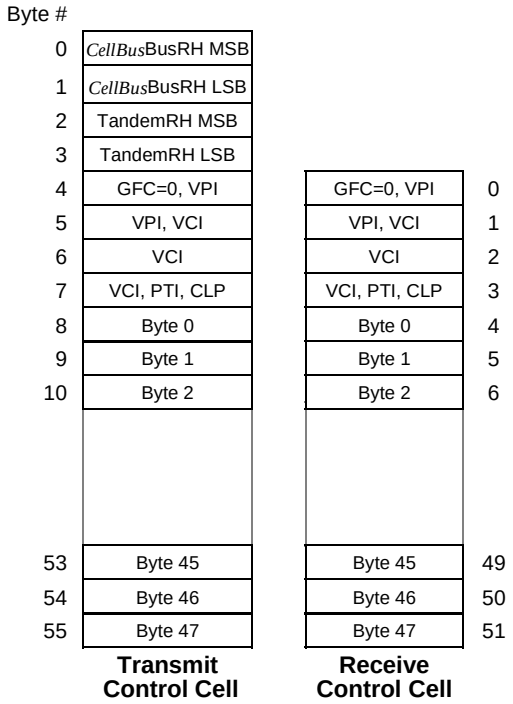
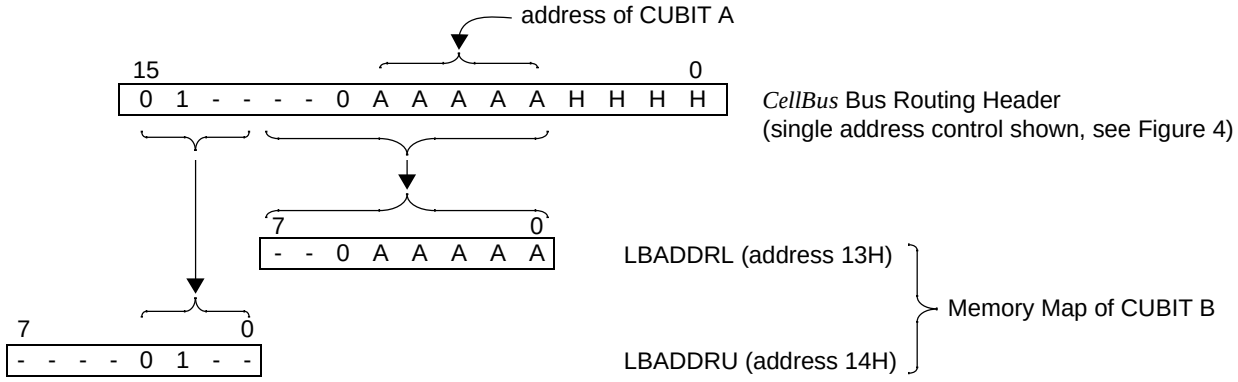


Figure 23. Transmit and Receive Control Cell Formats

LOOPBACK CELL SEND, RECEIVE AND RELAY

The loopback function is provided for diagnostic purposes. It may be used on-line (ONLINE = 1), or off-line (ONLINE = 0). A loopback path for a cell from CUBIT A to CUBIT B and back to CUBIT A can be set up by loading the LBADDR registers in Addresses 13H and 14H of CUBIT B with the single address control *CellBus* Bus Routing Header of CUBIT A, as shown in Figure 24. The microprocessor then writes a cell with a single address loopback Routing Header into the control transmit buffer (Addresses A0H-D7H) of CUBIT A and causes the cell to be sent. When CUBIT B receives the cell it will use the contents of LBADDR to form a new Routing Header for the cell and send it back to CUBIT A. CUBIT A will receive the cell and place it in the control receive buffer where it can be examined by the microprocessor.

The above description assumes that the loopback cell originates in the control transmit buffer of CUBIT A, but it could also be received from the inlet port. Also assumed is that the LBADDR registers of CUBIT B are loaded with a single address control Routing Header for CUBIT A. Any of the seven Routing Header formats shown in Figure 4 could actually be loaded, with a corresponding change in the final destination of the loopback cell.

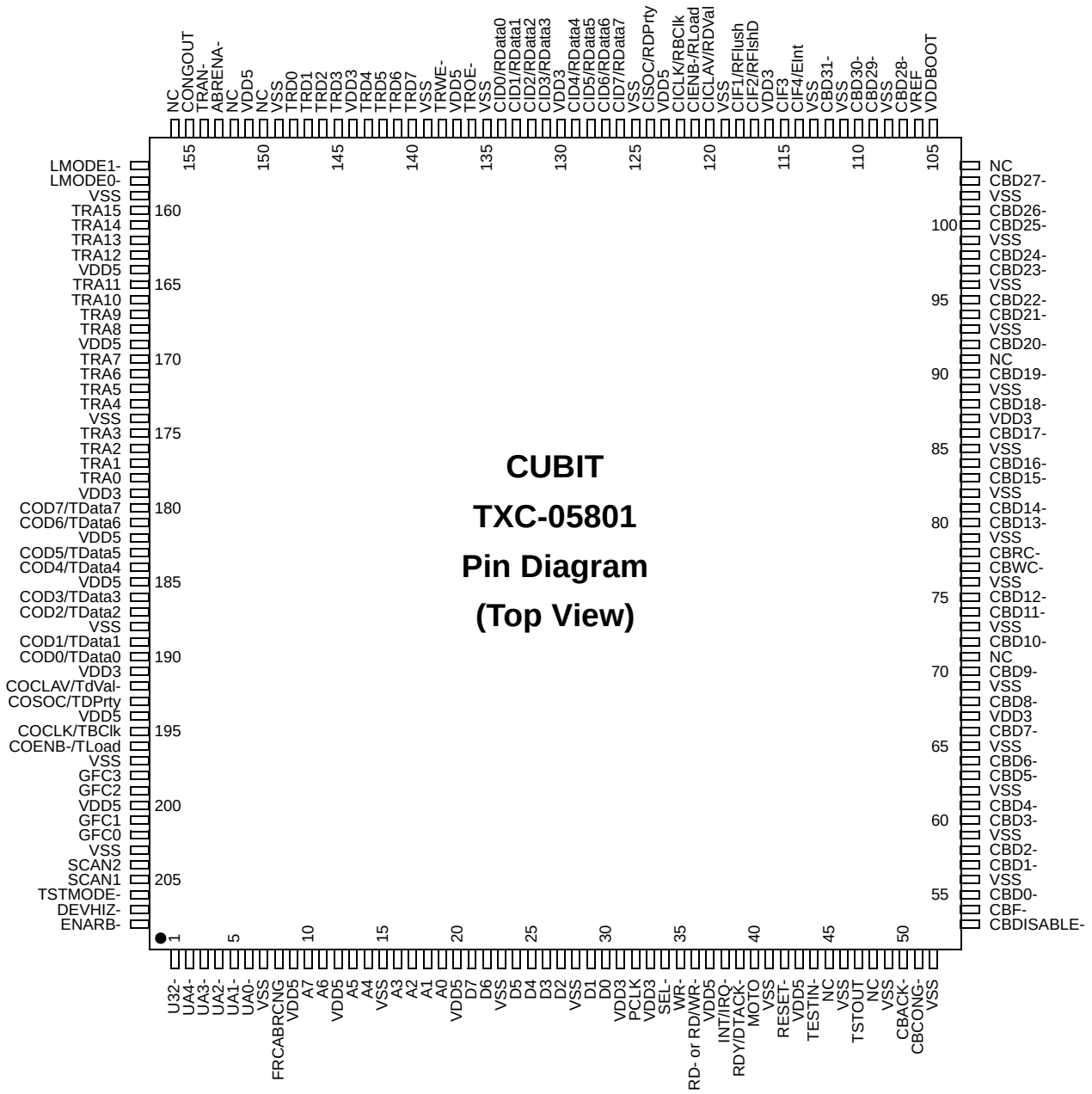


Note: - indicates don't care state

Figure 24. Loading the Loopback Registers

All aspects of system operation are the responsibility of the control system implemented for use of the CUBIT devices. Care must be taken to ensure that no more than one CUBIT is trying to set up a loopback into the same CUBIT, or mis-routing will ensue.

PIN DIAGRAM



Note: Active low (inverted) or active-on-falling-edge signals are indicated by '-' at end of symbol (e.g., LMODE1- is equivalent to $\overline{\text{LMODE1}}$).

Figure 25. CUBIT TXC-05801 Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY, GROUND AND NO CONNECT PINS

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD5	9, 12, 20, 37, 43, 123, 137, 151, 164, 169, 182, 185, 194, 200	P		**V_{DD5}**: +5 volt supply voltage, ±5%
VDD3	31, 33, 67, 87, 116, 130, 144, 179, 191	P		**V_{DD3}**: +3.3 volt supply voltage, ±5%
VSS	7, 15, 23, 28, 41, 46, 49, 52, 56, 59, 62, 65, 69, 73, 76, 79, 82, 85, 89, 93, 96, 99, 102, 108, 111, 113, 119, 125, 135, 139, 149, 159, 174, 188, 197, 203	P		**V_{SS}**: Ground, 0 volt reference.
VDDBOOT	105	P		**V_{DDBOOT}:** +5V supply voltage, ± 10%, which must be present for the *CellBus* bus disable function to work.
NC	45, 48, 71, 91, 104, 150, 152, 156	--		**No Connect**: NC pins are not to be connected, not even to another NC pin, but must be left floating. Connection of NC pins may impair performance or cause damage to the device. Some NC pins may be assigned functions in future upgrades of the device. Backwards compatibility of the upgraded device in existing applications may rely upon these pins having been left floating.

* Note: I=Input; O=Output; P=Power

CELL INLET

Symbol**	Pin No.	I/O/P	Type*	Name/Function
CICLAV/ RDVal	120	I	TTL	**Cell Inlet Cell Available:** Cell available signal from PHY device to indicate that it has a complete cell to transfer. RDVal in ALI-25 mode.
CICLK/ RBClk	122	O	6 mA	**Cell Inlet Clock:** Transfer clock. Rising edge used for data transfer. RBClk in ALI-25 mode.
CID(7-4) CID(3-0)/ RData(7-0)	126-129, 131-134	I	TTL	**Cell Inlet Data:** Byte-parallel input data. RData(7-0) in ALI-25 mode.
$\overline{\text{CIENB}}$/ RLoad	121	O	4 mA	**Cell Inlet Enable:** In UTOPIA mode, an active low signal indicating that input data and CISOC will be sampled at the end of the next cycle. RLoad in ALI-25 mode.
CIF1/ RFlush	118	O	4 mA	**Cell Inlet Flag 1:** Active high positive cell receipt acknowledge in 16-Bit Cell Interface mode. RFlush in ALI-25 mode.
CIF2/RFlshD	117	I	TTL	**Cell Inlet Flag 2:** RFlshd in ALI-25 Mode.
CIF3	115	O	4 mA	**Cell Inlet Flag 3:** Active high cell rejection indication (non-ACK) in 16-Bit Cell Interface mode.
CIF4/EInt	114	I	TTL	**Cell Inlet Flag 4:** EInt in ALI-25 mode.
CISOC/ RDPrty	124	I	TTL	**Cell Inlet Start of Cell:** Start-of-Cell indication for UTOPIA mode. RDPrty parity in ALI-25 mode. (Note: Parity output of ALI-25 device is ignored by the CUBIT).

* See Input, Output and I/O Parameters section for Type definitions.
** Signals which are active when low or upon their falling edges are shown as negated (overlined).

CELL OUTLET

Symbol	Pin No.	I/O/P	Type	Name/Function
COCLAV/ $\overline{\text{TdVal}}$	192	I/O, see Note 1.	TTL/4 mA	**Cell Outlet Cell Available:** COCLAV input is asserted by PHY device to indicate that it can accept the transfer of a complete cell in UTOPIA mode and 16-Bit Cell Interface mode. COCLAV output is asserted by CUBIT to indicate that an outlet cell is available in Back-to-Back mode. $\overline{\text{TdVal}}$ output in ALI-25 mode.
COCLK/ TBClk	195	O/I, see Note 2.	TTL/6 mA	**Cell Outlet Clock:** Transfer clock. Rising edge used for data transfer. TBClk input in ALI-25 mode.
COD(7-6) COD(5-4) COD(3-2) COD(1-0)/ TData(7-0)	180, 181, 183, 184, 186, 187, 189, 190	O	4 mA	**Cell Outlet Data:** Byte-parallel output data. TData(7-0) output in ALI-25 mode.
$\overline{\text{COENB}}$/ TLoad	196	O/I, see Note 2.	TTL/4 mA	**Cell Outlet Enable:** An active low enable signal which occurs during clock cycles when COD(7-0) data and/or COSOC are active. TLoad input in ALI-25 mode.
COSOC/ TDPrty	193	O	4 mA	**Cell Outlet Start of Cell:** Start-of-Cell for UTOPIA mode. TDPrty parity output in ALI-25 mode.
GFC(3-2) GFC(1-0)	198, 199, 201, 202	I	TTL(PU)	**Generic Flow Control:** Inlet for GFC nibble to be inserted at cell outlet.
FRCABRCNG	8	I	TTL(PU)	**Force ABR Congestion:** Active high signal to force a congestion indication for any ABR cells received.

Note 1: I for UTOPIA and 16-bit cell interface modes, O for Back-to-Back and ALI-25 modes.
Note 2: O for UTOPIA and 16-bit cell interface modes, I for Back-to-Back and ALI-25 modes.

***CellBus* Bus PORT**

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{CBACK}}$	50	I/O	GTL	***CellBus* Bus Acknowledge:** Active low acknowledge.
$\overline{\text{CBCONG}}$	51	I/O	GTL	***CellBus* Bus Congestion Indicator:** Active low congestion indicator.
$\overline{\text{CBD(31-24)}}$	112, 110, 109, 107, 103, 101, 100, 98	I/O	GTL	***CellBus* Bus Data:** Active low 32-bit parallel data input/output bus.
$\overline{\text{CBD(23-16)}}$	97, 95, 94, 92, 90, 88, 86, 84	I/O	GTL	
$\overline{\text{CBD(15-8)}}$	83, 81, 80, 75, 74, 72, 70, 68	I/O	GTL	
$\overline{\text{CBD(7-0)}}$	66, 64, 63, 61, 60, 58, 57, 55	I/O	GTL	
$\overline{\text{CBF}}$	54	I/O	GTL	***CellBus* Bus Frame:** 16-clock cycle structure.
$\overline{\text{CBRC}}$	78	I	GTL	***CellBus* Bus Read Clock:** Accepts data from bus. Falling edge used for data transfer.
$\overline{\text{CBWC}}$	77	I	GTL	***CellBus* Bus Write Clock:** Puts data on the bus. Falling edge used for data transfer.
CONGOUT	155	O	4 mA	***CellBus* Bus Congestion:** Active high GTL-to-CMOS level conversion of $\overline{\text{CBCONG}}$ signal. (This signal is not part of the *CellBus* bus.)
$\overline{\text{CBDISABLE}}$	53	I	CMOS	***CellBus* Bus Disable:** Active low signal to tristate the entire *CellBus* bus regardless of the state of the V_{DD3} and V_{DD5} power supplies. (This signal is not part of the *CellBus* bus.)
VREF	106	I	Reference Voltage	**VREF:** Reference voltage for GTL receivers. VREF is approximately 2/3 V_{tt}, where V_{tt} is the backplane termination voltage (nominally Vtt = +1.2V). The input connection to this pin is not part of the *CellBus* bus.

MICROPROCESSOR PORT

Symbol	Pin No.	I/O/P	Type	Name/Function
A(7-6) A(5-4) A(3-0)	10, 11, 13, 14, 16-19	I	TTL	**Address Bus:** 8-bit address lines from microprocessor, used to address CUBIT register memory. A0 is LSB. High is logic 1.
D(7-6) D(5-2) D(1-0)	21, 22, 24-27, 29, 30	I/O	TTL/8 mA	**Data Bus:** Bidirectional 8-bit data lines used for transferring data to and from microprocessor. D0 is LSB. High is logic 1.
INT/$\overline{\text{IRQ}}$	38	O	4 mA	**Interrupt:** Active high for Intel, active low for Motorola.
MOTO	40	I	TTL	**Motorola Mode:** Select Motorola operation if high, Intel if low.
PCLK	32	I	TTL	**Processor Clock:** Rising edge used for data transfer.
$\overline{\text{RD}}$ or RD/$\overline{\text{WR}}$	36	I	TTL	**Read/Write:** Data transfer command for CUBIT memory. Read (low) for Intel. Read (high) / Write (low) for Motorola.
RDY/$\overline{\text{DTACK}}$	39	O	OD 4 mA	**Ready or Data Transfer Acknowledge:** Active high Ready for Intel, active low Data Transfer Acknowledge for Motorola.
$\overline{\text{SEL}}$	34	I	TTL	**Select:** Active low signal to enable data transfer.
$\overline{\text{WR}}$	35	I	TTL	**Write:** Active low write command for transferring data to CUBIT memory in Intel mode. This input must be held high in Motorola mode.

TRANSLATION RAM ACCESS PORT

Symbol	Pin No.	I/O/P	Type	Name/Function
TRA(15-12) TRA(11-8) TRA(7-4) TRA(3-0)	160-163, 165-168, 170-173, 175-178	O	4 mA	**Translation RAM Address Bus:** 16-bit address output to 64k byte Translation RAM. TRA(7-0) are cell data outlet 8 LSB if $\overline{\text{ABRENA}}$ is enabled. TRA0 is LSB. High is logic 1.
TRD (7-4) TRD (3-0)	140-143, 145-148	I/O	TTL/4 mA	**Translation RAM Data Bus:** Bidirectional 8-bit data bus. TRD(7-0) are cell data inlet 8 LSB if $\overline{\text{ABRENA}}$ is enabled. TRD0 is LSB. High is logic 1.
$\overline{\text{TROE}}$	136	O	4 mA	**Translation RAM Output Enable:** Active low output enable.
$\overline{\text{TRWE}}$	138	O	4 mA	**Translation RAM Write Enable:** Active low write enable.

CONTROL STRAPS

Symbol*	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{ABRENA}}$	153	I	TTL (PU)	**16-Bit Cell Interface Mode Enable:** Active low signal to select 16-bit data I/O. The additional 8 data bits are carried by TRD(7-0) acting as the 8 LSB for cell data inlet and by TRA(7-0) acting as the 8 LSB for cell data outlet. This pin enables the 16-Bit Cell Interface operating mode.
$\overline{\text{DEVHIZ}}$	207	I	TTL (PU)	**Device High Impedance:** Active low signal to set all outputs to high-impedance (Hi-Z) state.
$\overline{\text{ENARB}}$	208	I	TTL (PU)	**Enable Arbiter:** Active low signal to enable internal copy of Bus Arbiter and Frame Pulse Generator.
$\overline{\text{LMODE1}}$ $\overline{\text{LMODE0}}$	157, 158	I	TTL (PU)	**Operating Mode:** Two active low signals for selection of CUBIT operating mode.
$\overline{\text{TRAN}}$	154	I	TTL (PU)	**Translation Enable:** An active low signal to enable header translation by the CUBIT.
$\overline{\text{UA(4-0)}}$	2-6	I	TTL (PU)	**Unit Address:** Five active low device identity straps, used to identify each CUBIT device in a system containing up to 32 devices.
$\overline{\text{U32}}$	1	I	TTL (PU)	**Unit 32:** Control strap for setting maximum number of CUBITs that can be connected to the *CellBus* bus. Set low for 32 CUBITs, high (or floating) for 16.

* Note: All control straps are active low inputs. They are pulled up internally and will be inactive if left unconnected. They must be set low to enable the associated function.

RESET AND TEST PINS

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{RESET}}$	42	I	TTL	**Reset:** Active low device reset (minimum duration 300 nanoseconds).
$\overline{\text{TSTMODE}}$	206	I	--	**Test Mode:** Active low signal to enable device test by manufacturer. Tie to V_{DD5}.
SCAN1	205	I	--	**Scan 1:** Internal test function. Tie to V_{SS}.
SCAN2	204	I	--	**Scan 2:** Internal test function. Tie to V_{SS}.
TSTOUT	47	O	--	**Internal Test Pin:** Leave floating.
$\overline{\text{TESTIN}}$	44	I	--	**Internal Test Mode Input:** Tie to V_{DD5}.

BSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage, +5V	V_{DD5}	-0.3	7.0	V	Note 1
Supply voltage, +3.3V	V_{DD3}	-0.3	6.0	V	Note 1
DC input voltage	V_{IN}	-0.3	V_{DD5} +0.3	V	Note 1
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient operating temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Component Temperature x Time	TI		270 x 5	^oC x s	Note 1
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD		$\pm$2000	V	per MIL-STD-833D Method 3015.7

Notes:
1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		36.6		$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD5}	4.75	5.0	5.25	V	
I_{DD5}		20	48	mA	
P_{DD5}		100	250	mW	
V_{DD3}	3.14	3.30	3.46	V	
I_{DD3}		150	289	mA	
P_{DD3}		500	1000	mW	
V_{DDBOOT}	4.75	5.00	5.25	V	
I_{DDBOOT}		10	100	μA	
P_{DDBOOT}		500	525	μW	
P_{TOTAL}		600	1250	mW	

INPUT, OUTPUT AND I/O PARAMETERS

INPUT PARAMETERS FOR CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	$0.7 * V_{DD5}$			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			$0.2 * V_{DD5}$	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current	-10	1	10	µA	
Input capacitance		5		pF	

INPUT PARAMETERS FOR GTL (GUNNING TRANSCEIVER LOGIC)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	0.86			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.66	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		7		pF	

INPUT PARAMETERS FOR TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	
Input capacitance		5		pF	

INPUT PARAMETERS FOR TTL (PU)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input current	-35	-115	-214	µA	$V_{IN}=V_{SS}$
Input leakage current			10	µA	$V_{IN}=V_{DD5}$
Input capacitance		5		pF	

OUTPUT PARAMETERS FOR 4 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -4.0 mA
V_{OL}		0.2	0.4	V	I_{OL} = 4.0 mA
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	

OUTPUT PARAMETERS FOR 6 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -6.0 mA
V_{OL}		0.2	0.4	V	I_{OL} = 6.0 mA
I_{OL}			6.0	mA	
I_{OH}			-6.0	mA	

OUTPUT PARAMETERS FOR OD 4 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}			0.4	V	V_{DD}=4.75; I_{OL}= 4.0
I_{OL}			4.0	mA	

Note: Open Drain requires use of a 4.7 kΩ external pull-up resistor to V_{DD5}. If this resistor is not provided the output behaves as tri-state.

INPUT/OUTPUT PARAMETERS FOR GTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	0.86				$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.66	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		7		pF	
V_{OL}	0.2		0.4	V	
I_{OL}		33	48	mA	

INPUT/OUTPUT PARAMETERS FOR TTL/4 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		7		pF	
V_{OH}	2.4			V	$V_{DD} = 4.75$; $I_{OH} = -4.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 4.0$
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	

INPUT/OUTPUT PARAMETERS FOR TTL/8 mA

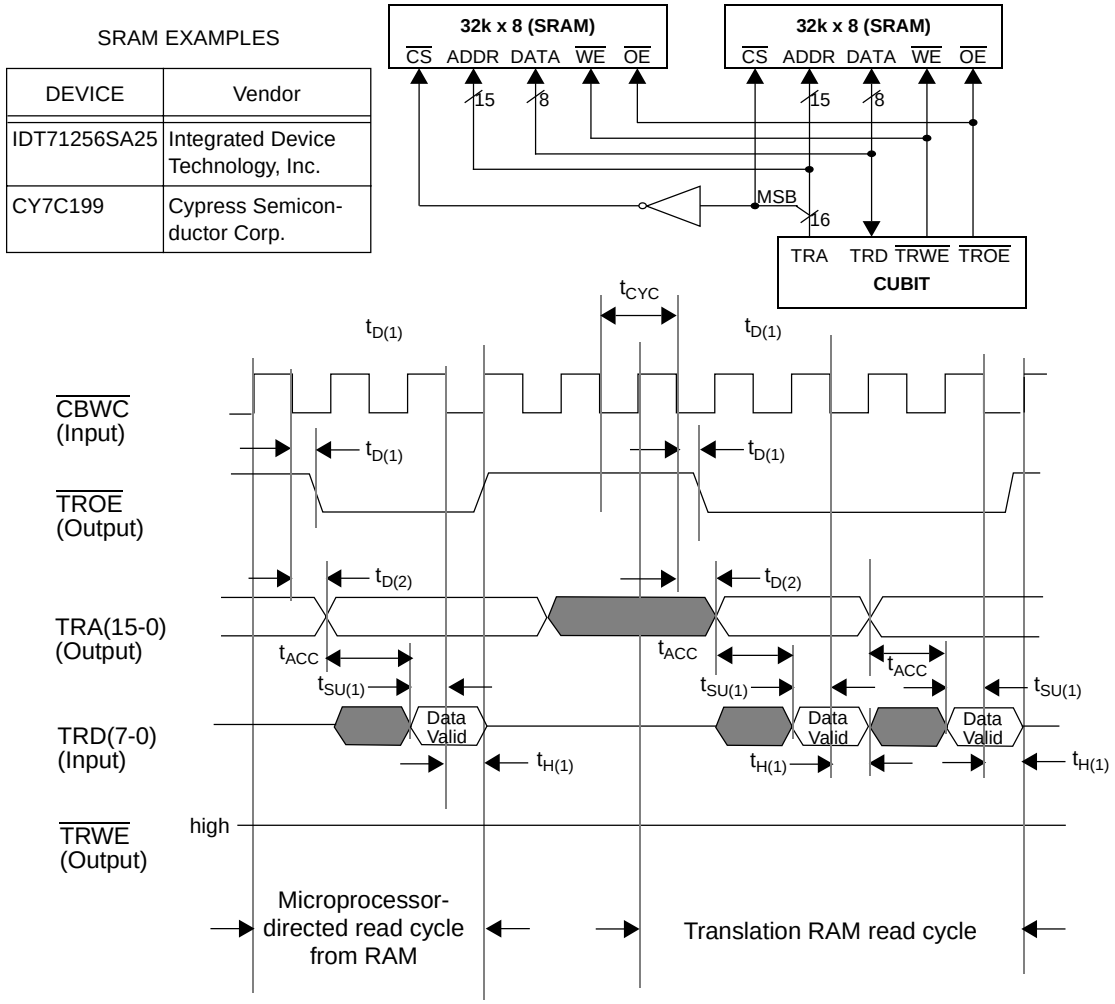
Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		7		pF	
V_{OH}	2.4			V	$V_{DD} = 4.75$; $I_{OH} = -8.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 8.0$
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	

TIMING CHARACTERISTICS

Detailed timing diagrams for the CUBIT device are provided in Figures 26 through 43, with values for the timing intervals given in tables below the waveform drawings. All output times are measured with a maximum load capacitance of 25 pF unless otherwise indicated. Timing parameters are measured at voltage levels of $(V_{IH}+V_{IL})/2$ for input signals or $(V_{OH}+V_{OL})/2$ for output signals.

CONTROL/TRANSLATION RAM INTERFACE

Figure 26. Translation RAM Timing - Read from RAM



Parameter	Symbol	Min	Typ	Max	Unit
$\overline{TROE}$ output delay after $\overline{CBWC}\downarrow$	$t_{D(1)}$	4		18	ns
TRA(15-0) output delay after $\overline{CBWC}\downarrow$	$t_{D(2)}$	4		20	ns
TRD(7-0) setup time before $\overline{CBWC}\downarrow$	$t_{SU(1)}$	3			ns
TRD(7-0) hold time after $\overline{CBWC}\downarrow$	$t_{H(1)}$	6			ns
$\overline{CBWC}$ cycle time; see note 1	t_{CYC}		30		ns
SRAM Read Cycle Access; see note 1	t_{ACC}			35	ns

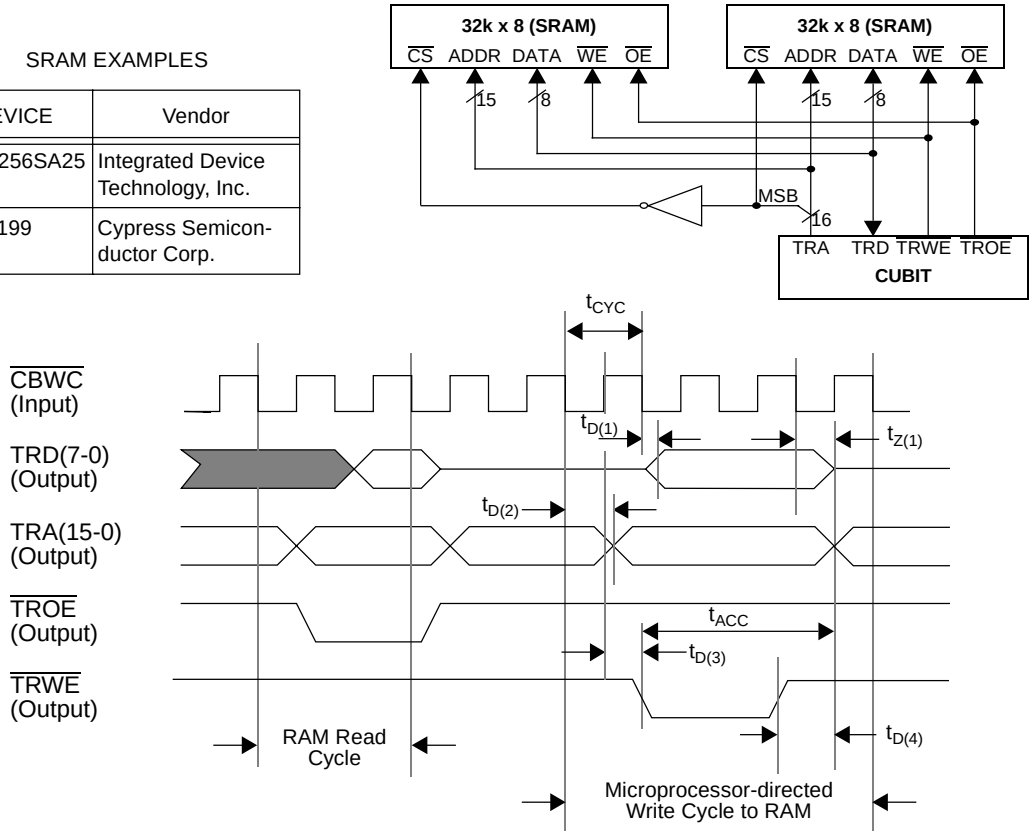
Control	Addr	Bit	Pin	Value
$\overline{ABRENA}$			153	High
$\overline{TRAN}$			154	Low
ONLINE	0C	7		1

Note 1: *CellBus* bus timing varies with application. The data shown is for the maximum speed deemed practical for a typical backplane design of 33 MHz. A faster Cell Bus will require an SRAM with less than a 35 nsec. read access time.

Figure 27. Translation RAM Timing - Write to RAM

SRAM EXAMPLES

DEVICE	Vendor
IDT71256SA25	Integrated Device Technology, Inc.
CY7C199	Cypress Semiconductor Corp.



Parameter	Symbol	Min	Typ	Max	Unit
TRD(7-0) delay from tristate after CBWC↓	$t_{D(1)}$			19	ns
TRD(7-0) delay to tri-state after CBWC↓	$t_{Z(1)}$			19	ns
TRA(15-0) delay after CBWC↓	$t_{D(2)}$			17	ns
TRWE delay after CBWC↓	$t_{D(3)}$			17	ns
TRWE↑ before TRA(15-0) goes tristate	$t_{D(4)}$	0			ns
CBWC cycle time; see note 1	t_{CYC}		30		ns
SRAM Write Cycle Access; see note 1	t_{ACC}			54	ns

Control	Addr	Bit	Pin	Value
ABRENA			153	High
TRAN			154	Low
ONLINE	0C	7		1

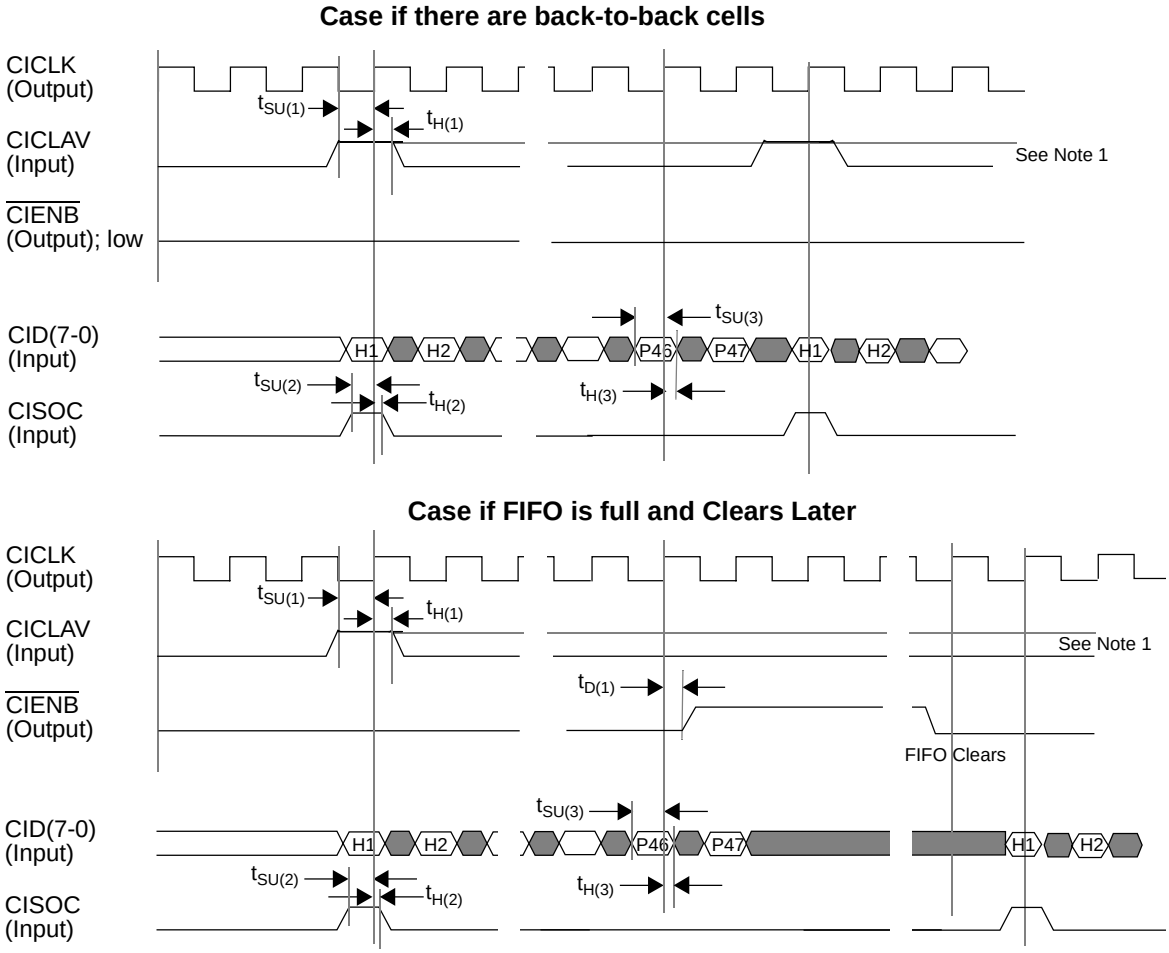
Note 1: *CellBus* bus timing varies with application. The data shown is for the maximum speed deemed practical for a typical backplane design of 33 MHz. A faster Cell Bus will require an SRAM with less than a 54 nsec. write access time.

CELL INTERFACE

Note: For all cell interface timing diagrams, the 48 payload bytes of the cell are labelled as P0 through P47. This is consistent with Figures 8 and 10, which describe the byte/word ordering of the four cell interface modes.

Cell Input/Output, UTOPIA Mode

Figure 28. Timing of UTOPIA Cell Receive Interface



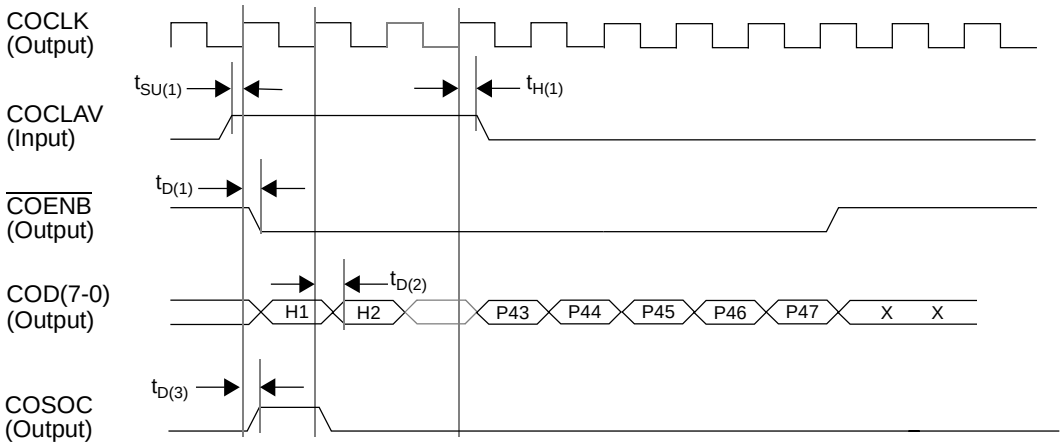
Parameter	Symbol	Min	Typ	Max	Unit
CICLAV setup time before CICLK↑	$t_{SU(1)}$	13			ns
CICLAV hold time after CICLK↑	$t_{H(1)}$	0			ns
$\overline{\text{CIENB}}$ delay (rise/fall) after CICLK↑	$t_{D(1)}$			9	ns
CISOC setup time before CICLK↑	$t_{SU(2)}$	13			ns
CISOC hold time after CICLK↑	$t_{H(2)}$	0			ns
CID(7-0) setup time before CICLK↑	$t_{SU(3)}$	16			ns
CID(7-0) hold time after CICLK↑	$t_{H(3)}$	0			ns

Control	Addr	Bit	Pin	Value
$\overline{\text{ABRENA}}$			153	High
$\overline{\text{LMODE1}}$			157	See Fig. 5
$\overline{\text{LMODE0}}$			158	
$\overline{\text{TRAN}}$			154	
ONLINE	0C	7		1

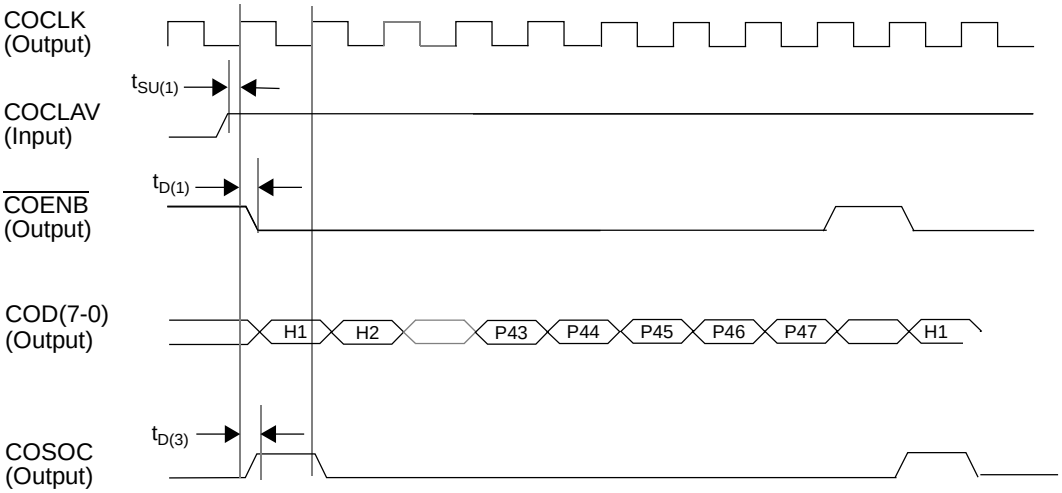
Note 1: CICLAV may be de-asserted after the first byte (H1) is read in by the CUBIT.

Figure 29. Timing of UTOPIA Cell Transmit Interface

Case if COCLAV is one cell



Case if COCLAV is two consecutive cells



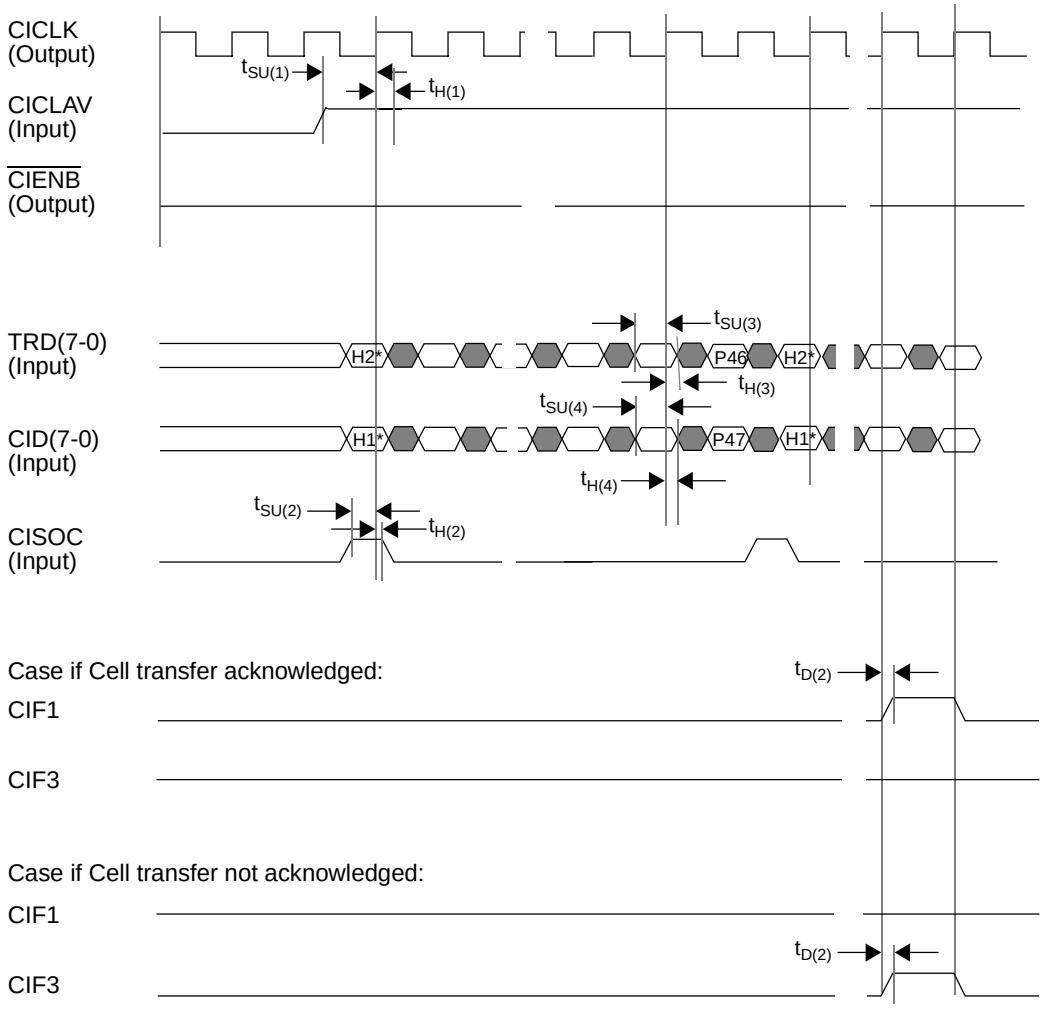
Parameter	Symbol	Min	Typ	Max	Unit
COCLAV setup time before COCLK↑	$t_{SU(1)}$	6			ns
COCLAV hold time after COCLK↑	$t_{H(1)}$	0			ns
$\overline{\text{COENB}}$ delay after COCLK↑	$t_{D(1)}$			6	ns
COD(7-0) delay after COCLK↑	$t_{D(2)}$			6	ns
COSOC delay after COCLK↑	$t_{D(3)}$			7	ns

Control	Addr	Bit	Pin	Value
$\overline{\text{ABRENA}}$			153	High
$\overline{\text{LMODE1}}$			157	See Fig. 5
$\overline{\text{LMODE0}}$			158	
$\overline{\text{TRAN}}$			154	
ONLINE	0C	7		1

Cell Input/Output, 16-Bit Cell Interface Mode

Figure 30. Timing of 16-Bit Cell Receive Interface

Case if there are back-to-back cells

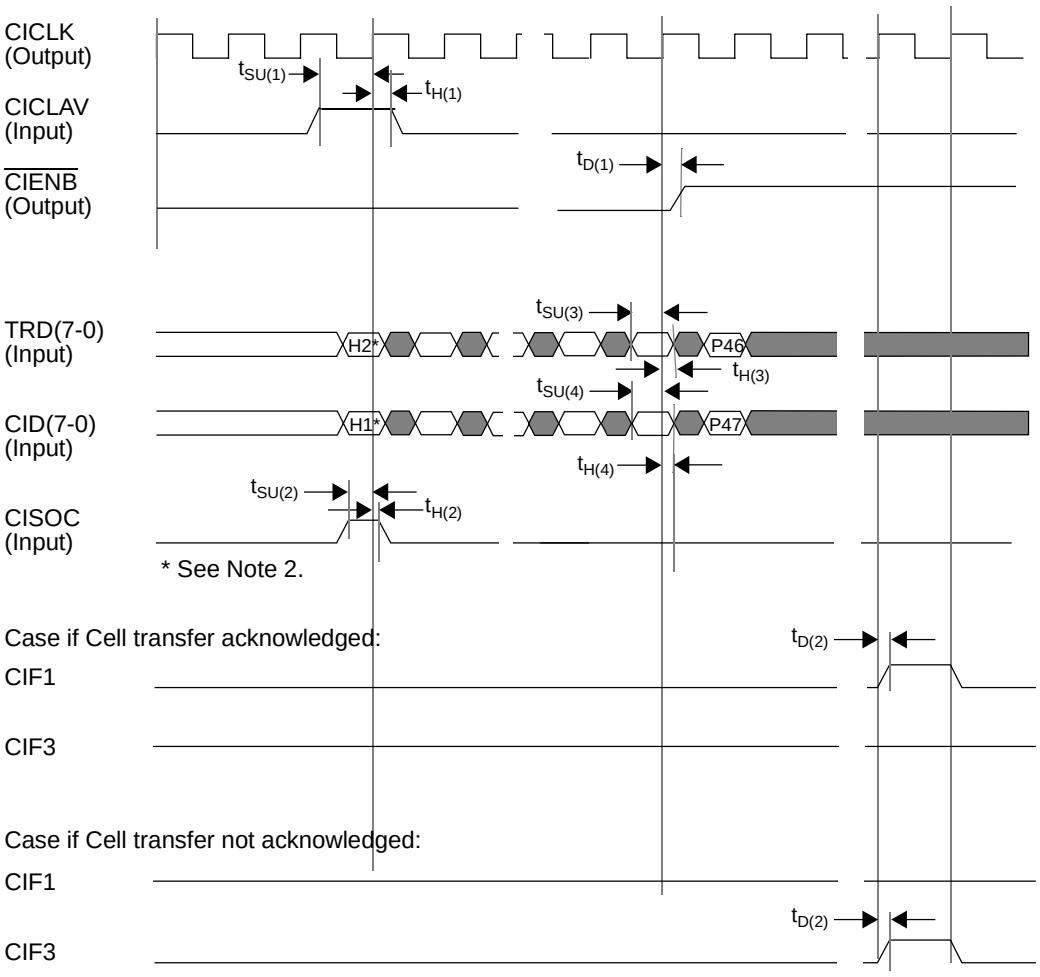


Notes:

1. ACK (CIF1) and NOACK (CIF3) are synchronous with CICLK but there is no fixed relationship to events occurring at the cell inlet.
2. Word ordering for 16-bit cell interface mode is detailed in Figure 10.

Figure 30 (continued). Timing of 16-Bit Cell Receive Interface

Case if FIFO is full



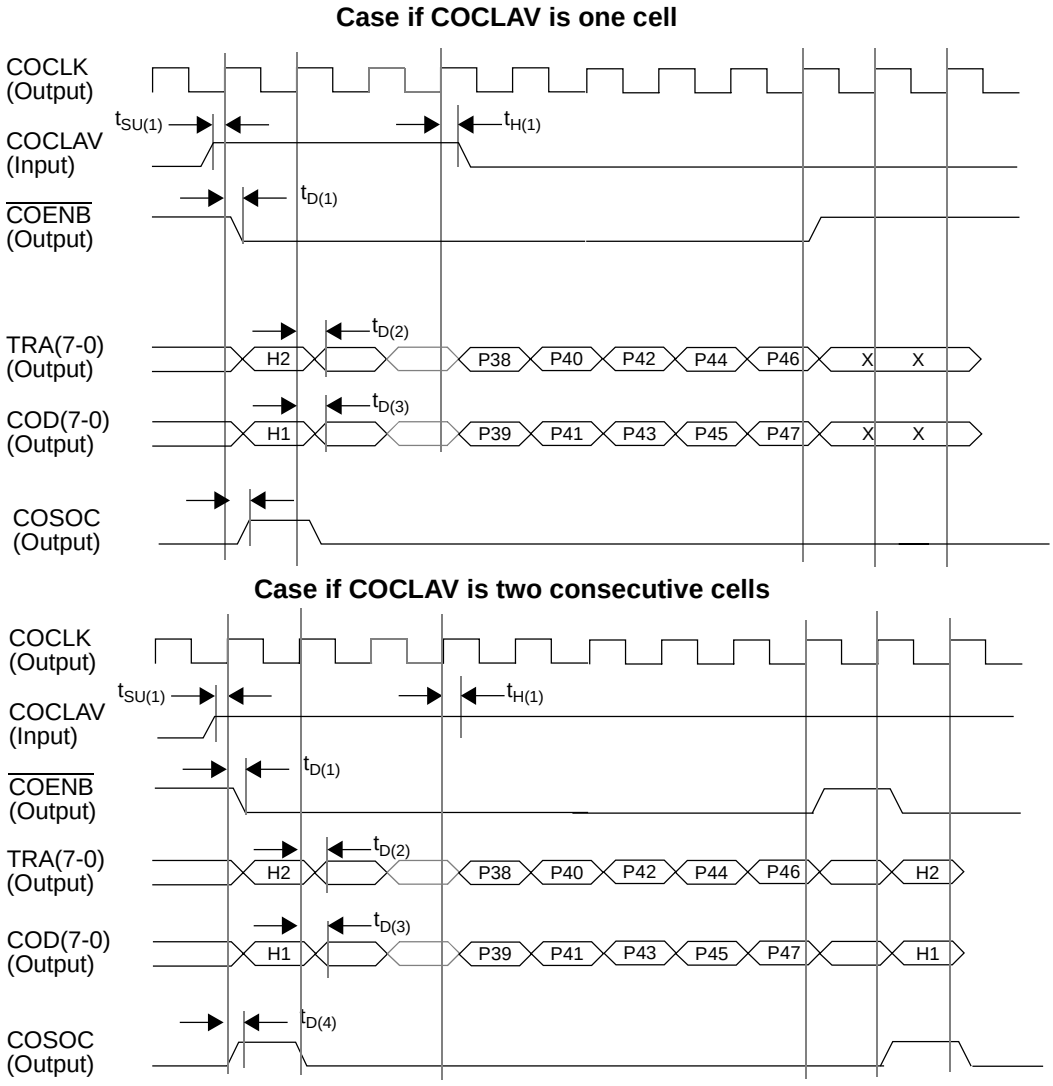
Notes:

1. ACK (CIF1) and NOACK (CIF3) are synchronous with CICLK but there is no fixed relationship to events occurring at the cell inlet.
2. Word ordering for 16-bit cell interface mode is detailed in Figure 10.

Parameter	Symbol	Min	Typ	Max	Unit
CICLAV setup time before CICLK↑	$t_{SU(1)}$	13			ns
CICLAV hold time after CICLK↑	$t_{H(1)}$	0			ns
$\overline{\text{CIENB}}$ delay (rise/fall) after CICLK↑	$t_{D(1)}$	0		9	ns
CISOC setup time before CICLK↑	$t_{SU(2)}$	13			ns
CISOC hold time after CICLK↑	$t_{H(2)}$	0			ns
CID(7-0) setup time before CICLK↑	$t_{SU(3)}$	16			ns
CID(7-0) hold time after CICLK↑	$t_{H(3)}$	0			ns
TRD(7-0) setup time before CICLK↑	$t_{SU(4)}$	14			ns
TRD(7-0) hold time after CICLK↑	$t_{H(4}$	0			ns
CIF1 and CIF3 delay after CICLK↑	$t_{D(2)}$		0		ns

Control	Addr	Bit	Pin	Value
$\overline{\text{ABRENA}}$			153	Low
ONLINE	0C	7		1

Figure 31. Timing of 16-Bit Cell Transmit Interface

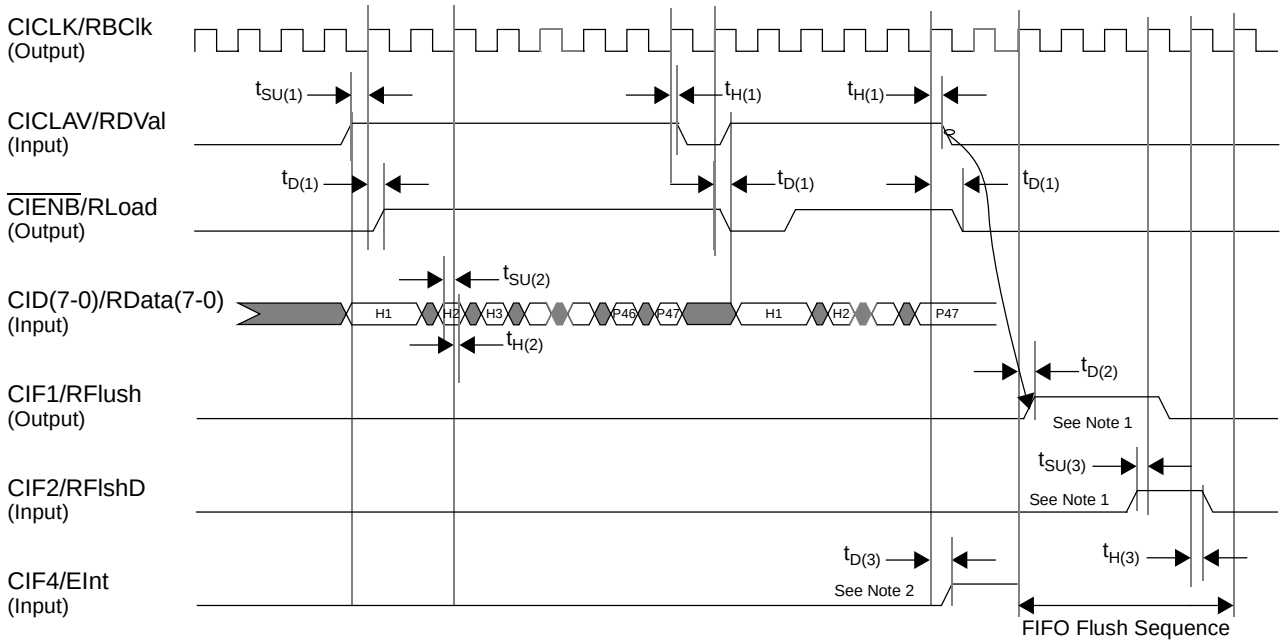


Parameter	Symbol	Min	Typ	Max	Unit
COCLAV setup time before COCLK↑	$t_{SU(1)}$	6			ns
COCLAV hold time after COCLK↑	$t_{H(1)}$			0	ns
COENB delay after COCLK↑	$t_{D(1)}$			6	ns
COD(7-0) delay after COCLK↑	$t_{D(2)}$			6	ns
TRA(7-0) delay after COCLK↑	$t_{D(3)}$			7	ns
COSOC delay after COCLK↑	$t_{D(4)}$			7	ns

Control	Addr	Bit	Pin	Value
$\overline{\text{ABRENA}}$			153	Low
ONLINE	0C	7		1

Cell Input/Output, ALI-25 Mode

Figure 32. Timing of ALI-25 Cell Receive Interface



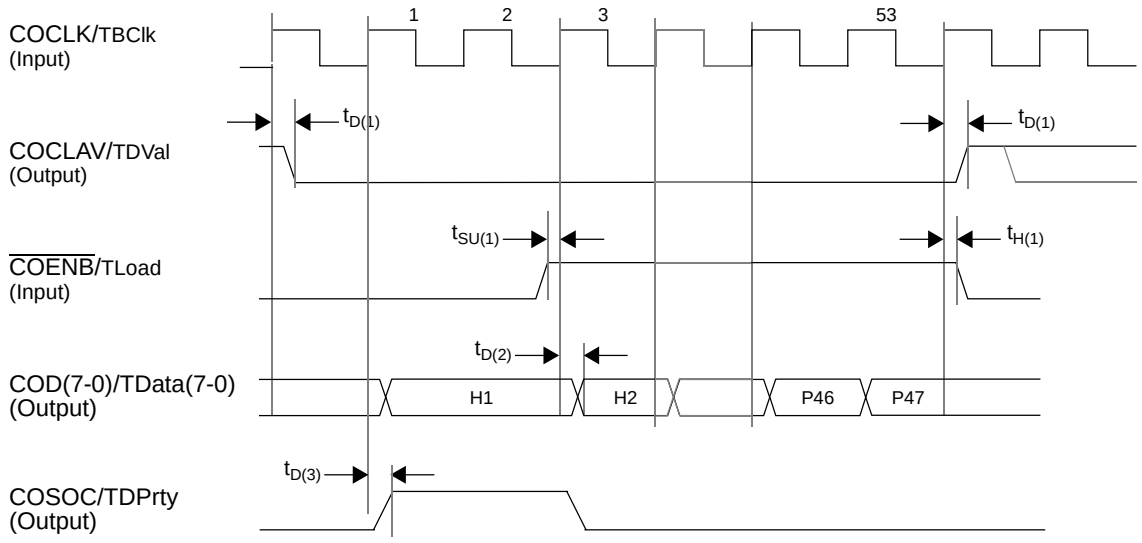
Parameter	Symbol	Min	Typ	Max	Unit
CICLAV setup time before CICLK↑	$t_{SU(1)}$	16			ns
CICLAV hold time after CICLK↑	$t_{H(1)}$	0			ns
$\overline{\text{CIENB}}$ delay after CICLK↑	$t_{D(1)}$			9	ns
CID(7-0) setup time before CICLK↑	$t_{SU(2)}$	6			ns
CID(7-0) hold time after CICLK↑	$t_{H(2)}$	0			ns
CIF1 delay after CICLK↑	$t_{D(2)}$			21	ns
CIF2 setup time before CICLK↑	$t_{(SU)3}$	8			ns
CIF2 hold time after CICLK↑	$t_{H(3)}$	0			ns
CIF4 delay time after CICLK↑	$t_{D(3)}$			21	ns

Control	Addr	Bit	Pin	Value
$\overline{\text{ABRENA}}$			153	High
$\overline{\text{LMODE0}}$			158	High
$\overline{\text{LMODE1}}$			157	Low
ONLINE	0C	7		1
TRAN			154	Low

Notes:

1. If, due to an error condition in the ALI-25C, RDVal is unexpectedly de-asserted at its CICLAV input, the CUBIT will assert CIF1 to flush the ALI-25C and declare a start-of-cell (SOC) error. The ALI-25C uses its RFlshD output pin to acknowledge via the CUBIT's CIF2 input pin that the flush was completed.
2. The second exception condition accommodated is the flagging of a HEC error by the ALI-25. If a HEC error is found, the ALI-25C asserts its EInt output pin, which drives the CIF4 input pin of the CUBIT and causes it to increment its HEC Error Counter.

Figure 33. Timing of ALI-25 Cell Transmit Interface

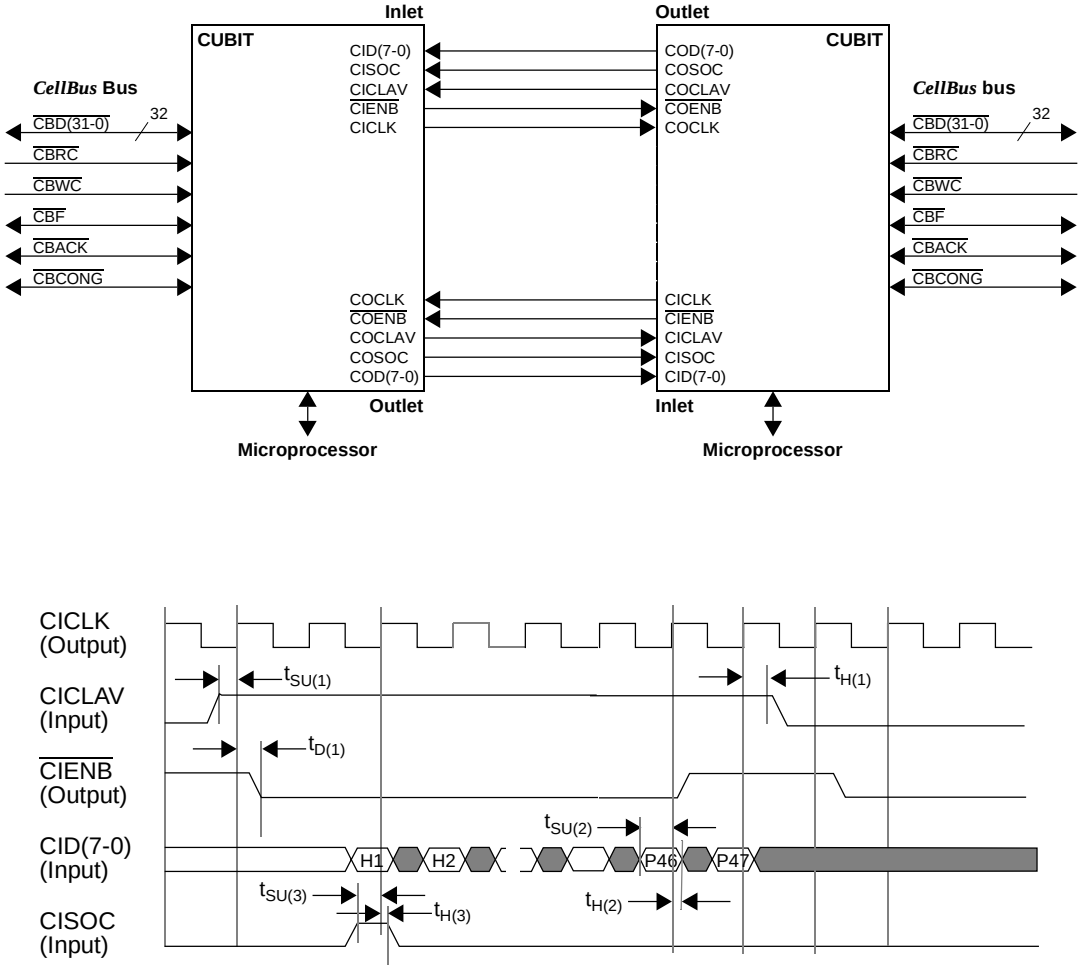


Parameter	Symbol	Min	Typ	Max	Unit
COCLAV delay after COCLK↑	$t_{D(1)}$			16	ns
$\overline{\text{COENB}}$ setup time before COCLK↑	$t_{SU(1)}$	18			ns
$\overline{\text{COENB}}$ hold time after COCLK↑	$t_{H(1)}$			0	ns
COD(7-0) delay after COCLK↑	$t_{D(2)}$			15	ns
COSOC delay after COCLK↑	$t_{D(3)}$			15	ns

Control	Addr	Bit	Pin	Value
$\overline{\text{ABRENA}}$			153	High
$\overline{\text{LMODE0}}$			158	High
$\overline{\text{LMODE1}}$			157	Low
ONLINE	0C	7		1
TRAN			154	Low

Cell Input/Output, Back-to-Back Mode

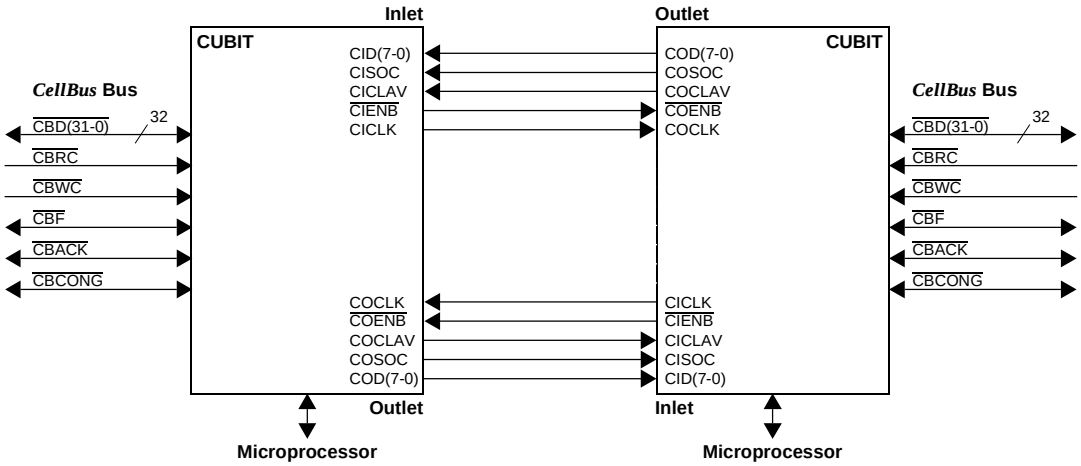
Figure 34. Timing of Back-to-Back Cell Receive Interface

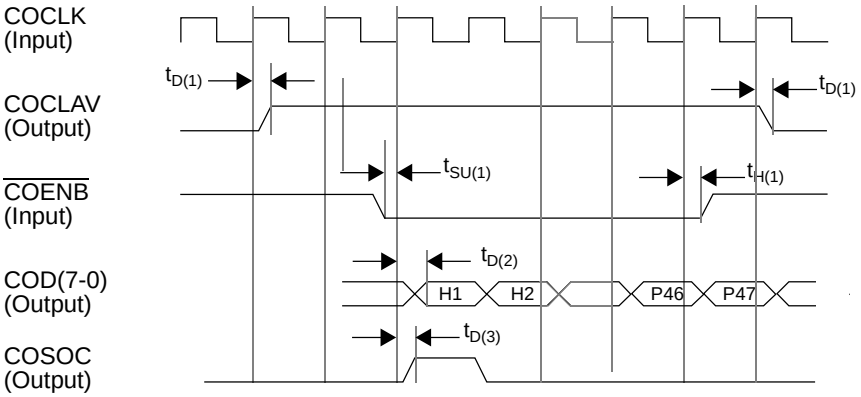


Parameter	Symbol	Min	Typ	Max	Unit
CICLAV setup time before CICLK↑	$t_{SU(1)}$	13			ns
CICLAV hold time after CICLK↑	$t_{H(1)}$	0			ns
CIENB delay after CICLK↑	$t_{D(1)}$	0		9	ns
CID(7-0) setup time before CICLK↑	$t_{SU(2)}$	16			ns
CID(7-0) hold time after CICLK↑	$t_{H(2)}$	0			ns
CISOC setup time before CICLK↑	$t_{SU(3)}$	13			ns
CISOC hold time after CICLK↑	$t_{H(3)}$	0			ns

Control	Addr	Bit	Pin	Value
$\overline{\text{ABRENA}}$			153	High
$\overline{\text{LMODE0}}$			158	Low
$\overline{\text{LMODE1}}$			157	Low
LINEDIV	0B	3-0		0[H]
ONLINE	0C	7		1
$\overline{\text{TRAN}}$			154	any

Figure 35. Timing of Back-to-Back Cell Transmit Interface



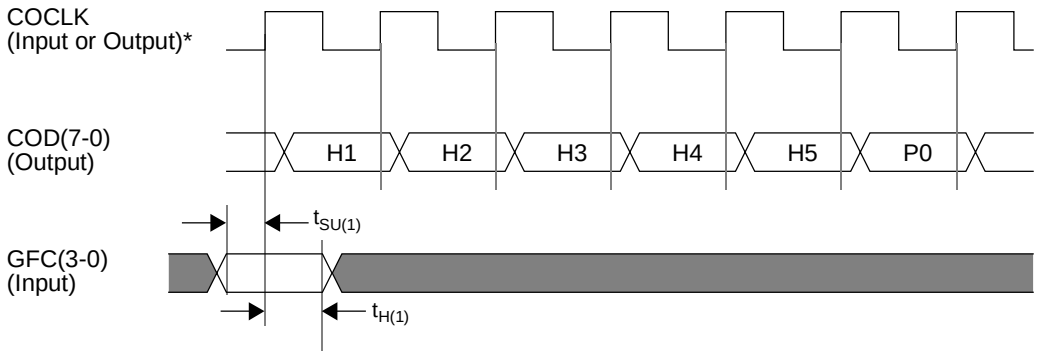


Parameter	Symbol	Min	Typ	Max	Unit
COCLAV delay after COCLK↑	$t_{D(1)}$			16	ns
$\overline{\text{COENB}}$ setup time before COCLK↑	$t_{SU(1)}$	18			ns
$\overline{\text{COENB}}$ hold time after COCLK↑	$t_{H(1)}$	0			ns
COD(7-0) delay after COCLK↑	$t_{D(2)}$			15	ns
COSOC delay after COCLK↑	$t_{D(3)}$			15	ns

Control	Addr	Bit	Pin	Value
$\overline{\text{ABRENA}}$			153	High
$\overline{\text{LMODE0}}$			158	Low
$\overline{\text{LMODE1}}$			157	Low
LINEDIV	0B	3-0		0[H]
ONLINE	0C	7		1
$\overline{\text{TRAN}}$			154	any

GFC Field Insertion

Figure 36. GFC Field Insertion Timing



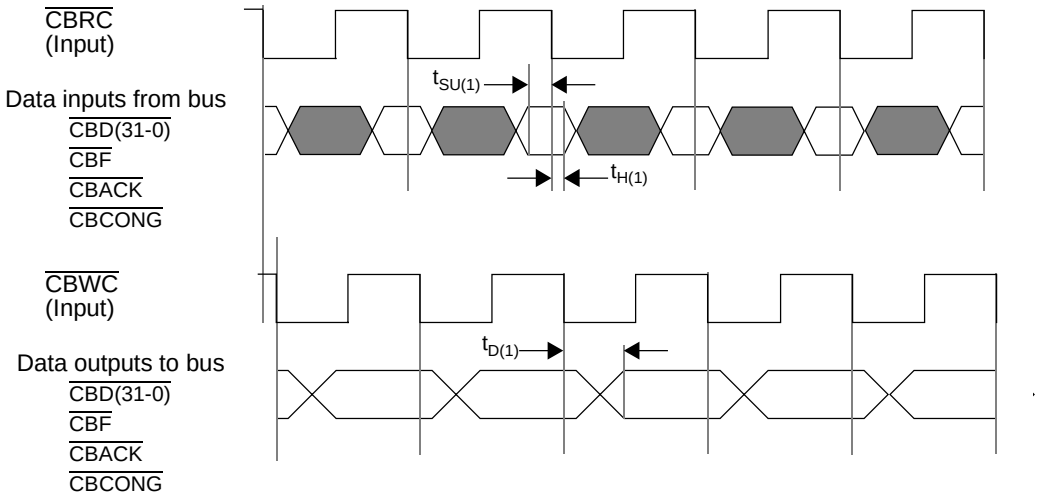
* Note: Output signal for UTOPIA and 16-bit cell interface modes.
Input signal for Back-to-Back and ALI-25 modes.

Parameter	Symbol	Min	Typ	Max	Unit
GFC(3-0) setup time before COCLK↑	$t_{SU(1)}$	4			ns
GFC(3-0) hold time after COCLK↑	$t_{H(1)}$	0			ns

CellBus Bus Port

Note: The *CellBus* Bus Port is characterized for an output load capacitance of 100 pF.

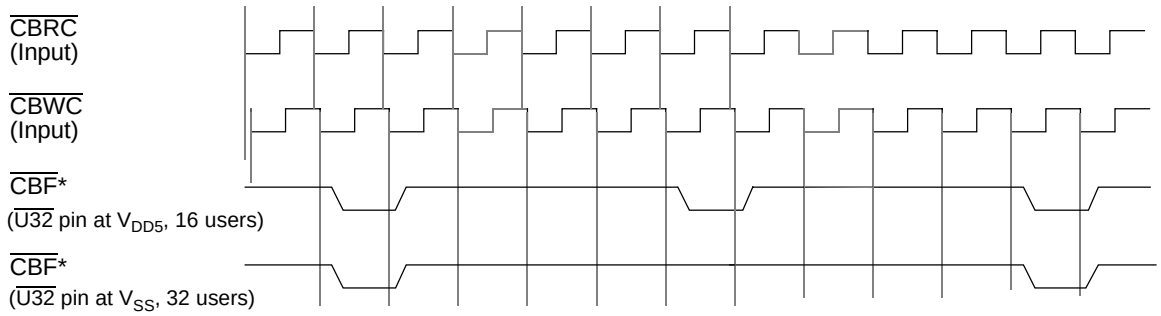
Figure 37. *CellBus* Bus Timing



Parameter	Symbol	Min	Typ	Max	Unit
CellBus bus inputs setup time before $\overline{\text{CBRC}}\downarrow$	$t_{SU(1)}$	0			ns
CellBus bus inputs hold time after $\overline{\text{CBRC}}\downarrow$	$t_{H(1)}$	6			ns
CellBus bus outputs delay after $\overline{\text{CBWC}}\downarrow$	$t_{D(1)}$	6		23.5	ns
$\overline{\text{CBWC}}$ and $\overline{\text{CBRC}}$ Frequency	f_{CB}		33.0	38.0	MHz
$\overline{\text{CBWC}}$ and $\overline{\text{CBRC}}$ Duty Cycle	dc	40		60	%

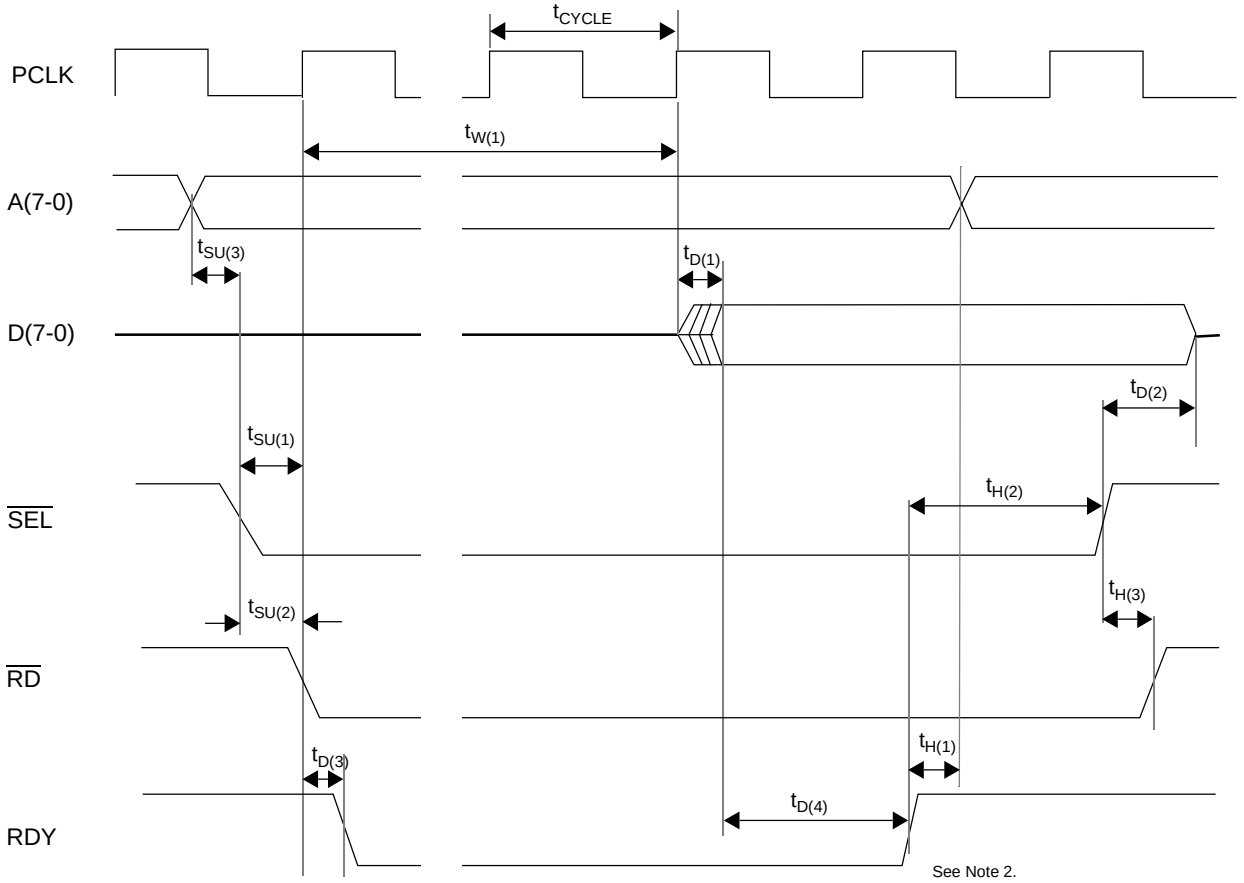
Note: See "*CellBus* Technical Manual and CUBIT Application", TXC-05801-TM1 (Ed. 3B) for additional timing details.

Figure 38. *CellBus* Bus Frame Position, 16-User and 32-User Applications



*Note: Output from the CUBIT that is selected to perform the bus arbitration function.
Input to all other CUBITs on the *CellBus* bus.

Figure 39. Intel Microprocessor Read Cycle Timing

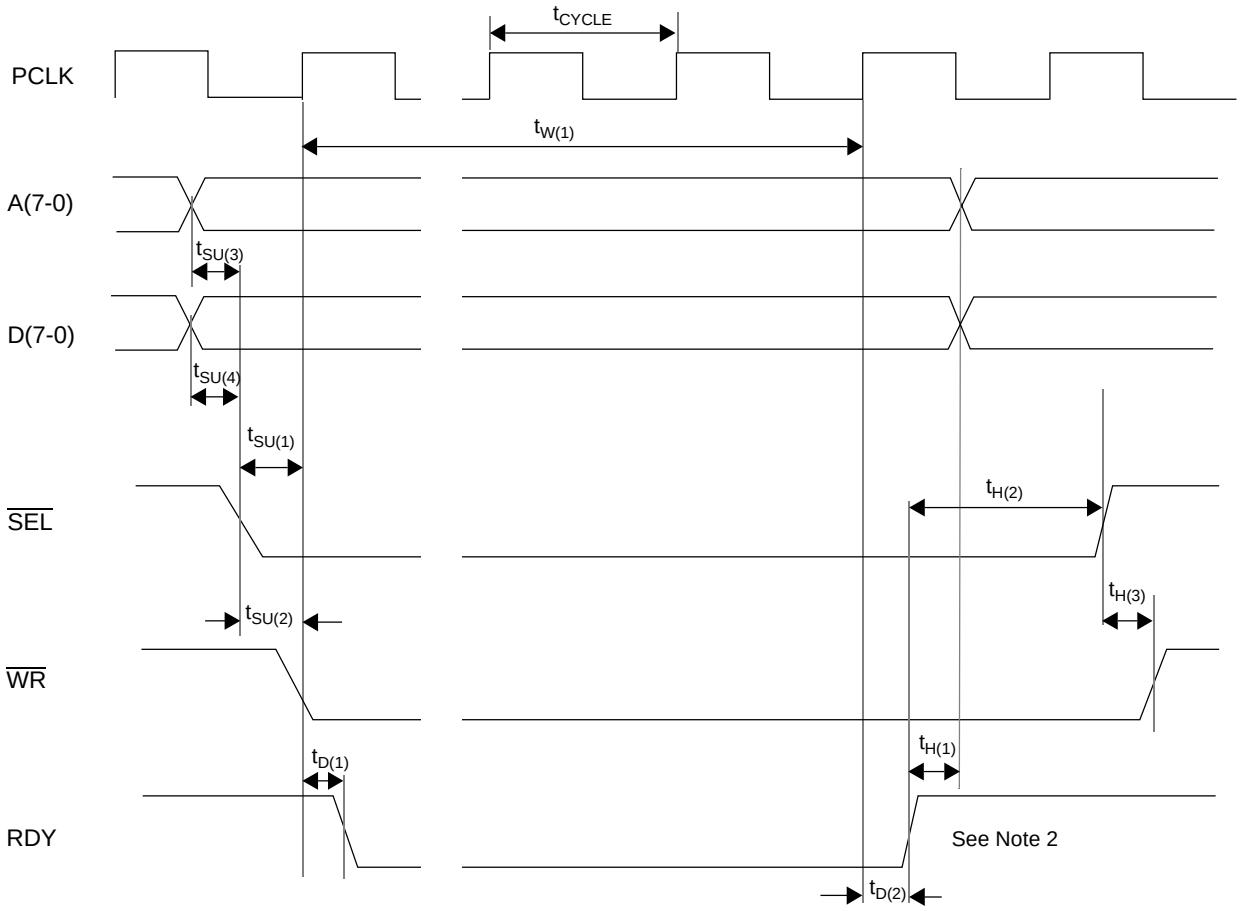


Parameter	Symbol	Min	Typ	Max	Unit
$\overline{SEL}$ set-up time to PCLK↑	$t_{SU(1)}$	3			ns
$\overline{SEL}$ set-up time to $\overline{RD}$↓	$t_{SU(2)}$	0			ns
A(7-0) set-up time to $\overline{SEL}$↓	$t_{SU(3)}$	0			ns
A(7-0) hold time after RDY↑	$t_{H(1)}$	0			ns
$\overline{SEL}$ hold time after RDY↑	$t_{H(2)}$	0			ns
$\overline{RD}$ hold time after $\overline{SEL}$↑	$t_{H(3)}$	0			ns
D(7-0) delay after PCLK↑	$t_{D(1)}$			18	ns
D(7-0) return to Z delay after $\overline{SEL}$↑	$t_{D(2)}$			16	ns
RDY delay after $\overline{RD}$↓	$t_{D(3)}$			21	ns
RDY delay after Data Valid	$t_{D(4)}$			t_{CYCLE} -3	ns
Bus cycle time (see note 1)	$t_{W(1)}$	3 x t_{CYCLE}		20 x t_{CYCLE}	ns
PCLK Period	t_{CYCLE}			30	ns
PCLK Duty Cycle	dc	40		60	%

Notes:

1. The CUBIT will hold off the microprocessor for a period of up to 20 *CellBus* bus clocks. This occurs only during accesses to the external Translation RAM.
2. RDY line should be pulled-up externally by a resistor connected to V_{DD}.

Figure 40. Intel Microprocessor Write Cycle Timing

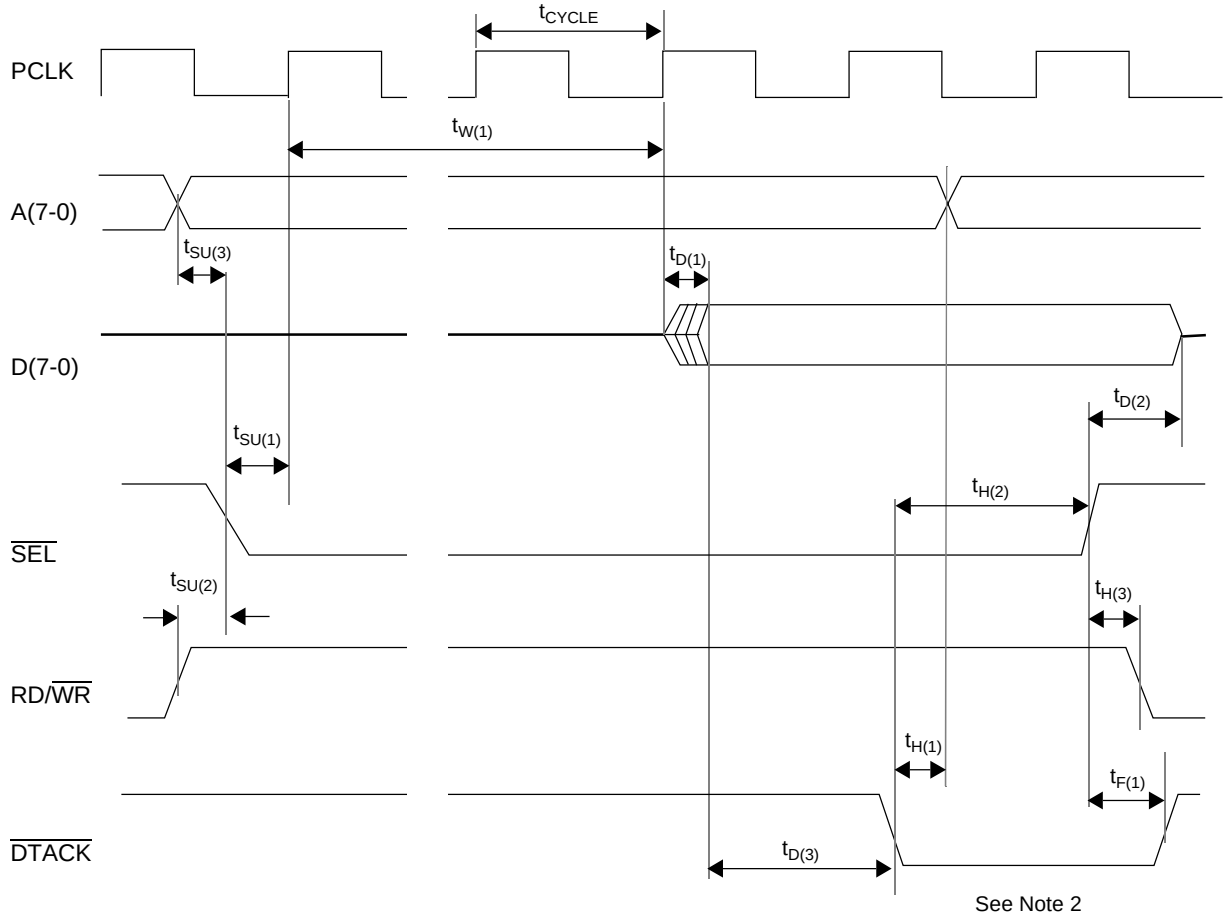


Parameter	Symbol	Min	Typ	Max	Unit
$\overline{SEL}$ set-up time to PCLK↑	$t_{SU(1)}$	3			ns
$\overline{SEL}$ set-up time to $\overline{WR}$↓	$t_{SU(2)}$	0			ns
A(7-0) set-up time to $\overline{SEL}$↓	$t_{SU(3)}$	0			ns
D(7-0) set-up time to $\overline{SEL}$↓	$t_{SU(4)}$	0			ns
A(7-0) & D(7-0) hold time after $\overline{SEL}$↑	$t_{H(1)}$	0			ns
$\overline{SEL}$ hold time after RDY↑	$t_{H(2)}$	0			ns
$\overline{WR}$ hold time after $\overline{SEL}$↑	$t_{H(3)}$	0			ns
RDY delay after $\overline{WR}$↓	$t_{D(1)}$			21	ns
RDY delay after PCLK↑	$t_{D(2)}$			15	ns
Bus cycle time (see note 1)	$t_{W(1)}$	3 x t_{CYCLE}		20 x t_{CYCLE}	ns
PCLK Period	t_{CYCLE}			30	ns
PCLK Duty Cycle	dc	40		60	%

Notes:

1. The CUBIT will hold off the microprocessor for a period of up to 20 *CellBus* bus clocks. This occurs only during accesses to the external Translation RAM.
2. RDY line should be pulled-up externally by a resistor connected to V_{DD}.

Figure 41. Motorola Microprocessor Read Cycle Timing

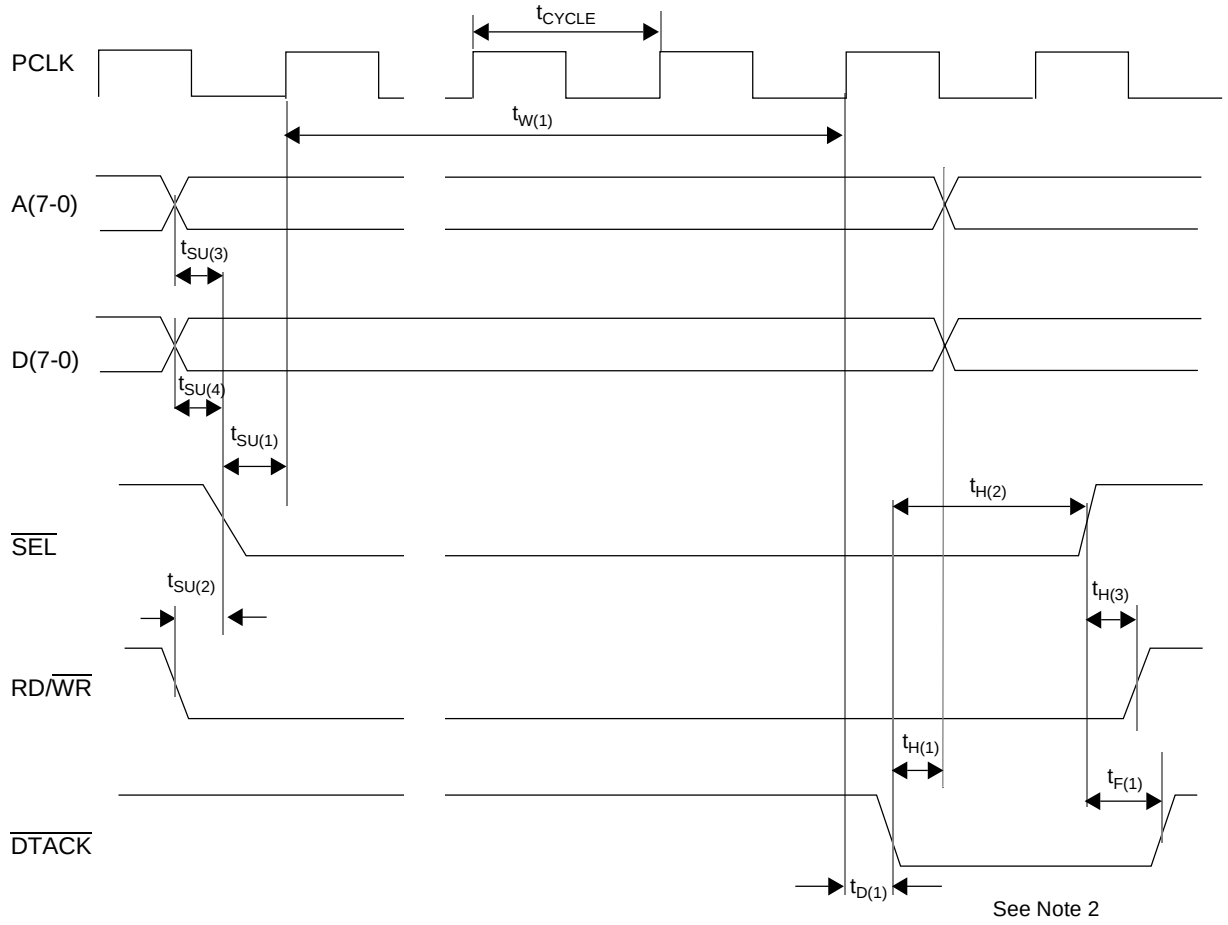


Parameter	Symbol	Min	Typ	Max	Unit
$\overline{SEL}\downarrow$ valid set-up time to PCLK$\uparrow$	$t_{SU(1)}$	4			ns
RD/$\overline{WR}$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	0			ns
A(7-0) set-up time to $\overline{SEL}\downarrow$	$t_{SU(3)}$	0			ns
A(7-0) hold time to $\overline{SEL}\downarrow$	$t_{H(1)}$	0			ns
$\overline{SEL}$ hold time after $\overline{DTACK}\downarrow$	$t_{H(2)}$	0			ns
RD/$\overline{WR}$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0			ns
D(7-0) output delay after PCLK$\uparrow$	$t_{D(1)}$			18	ns
D(7-0) float time after $\overline{SEL}\uparrow$	$t_{D(2)}$			17	ns
$\overline{DTACK}$ asserted after data valid	$t_{D(3)}$			t_{CYCLE} - 1	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	$t_{F(1)}$			12	ns
Bus cycle duration	$t_{W(1)}$	4 x t_{CYCLE}		20 x t_{CYCLE}	ns
PCLK Period	t_{CYCLE}			30	ns
PCLK Duty Cycle	dc	40		60	%

Notes:

1. The CUBIT will hold off the microprocessor for a period of up to 20 *CellBus* bus clocks. This occurs only during accesses to the external Translation RAM.
2. $\overline{DTACK}$ line should be pulled-up externally by a resistor connected to V_{DD}.

Figure 42. Motorola Microprocessor Write Cycle Timing

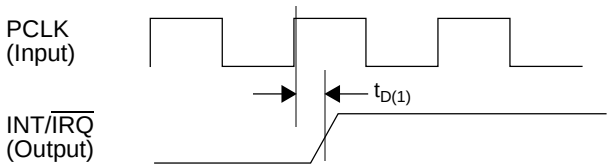


Parameter	Symbol	Min	Typ	Max	Unit
$\overline{SEL}\downarrow$ valid set-up time to PCLK$\uparrow$	$t_{SU(1)}$	4			ns
RD/$\overline{WR}$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	0			ns
A(7-0) set-up time to $\overline{SEL}\downarrow$	$t_{SU(3)}$	0			ns
D(7-0) set-up time to $\overline{SEL}\downarrow$	$t_{SU(4)}$	0			ns
A(7-0) & D(7-0) hold time after $\overline{DTACK}\downarrow$	$t_{H(1)}$	4			ns
$\overline{SEL}$ hold time after $\overline{DTACK}\downarrow$	$t_{H(2)}$	0			ns
RD/$\overline{WR}$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0			ns
$\overline{DTACK}$ delay after P-CLK$\uparrow$	$t_{D(1)}$			17	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	$t_{F(1)}$			13	ns
Bus cycle duration (see note 1)	$t_{W(1)}$	4 x t_{CYCLE}		20 x t_{CYCLE}	ns
PCLK Period	t_{CYCLE}			30	ns
PCLK Duty Cycle	dc	40		60	%

Notes:

1. The CUBIT will hold off the microprocessor for a period of up to 20 *CellBus* bus clocks. This occurs only during accesses to the external Translation RAM.
2. $\overline{DTACK}$ line should be pulled-up externally by a resistor connected to V_{DD}.

Figure 43. Microprocessor Interrupt Timing



Parameter	Symbol	Min	Typ	Max	Unit
INT/$\overline{IRQ}$ delay after PCLK↑	$t_{D(1)}$	0		23	ns

MEMORY MAP

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	RO	1	1	0	1	0	1	1	1
01	RO	1	1	0	0	0	0	0	0
02	RO	0	1	0	0	0	0	1	1
03	RO	Version	Version	Version	Version	0	0	0	1
04	RO	Mask Rev	Mask Rev	Mask Rev	Mask Rev	Reserved**			
05		Reserved**							
06		Reserved**							
07	WO	Reserved**							RESET
08	RC	CRCF	CRQOVF	CRQCAV	INSOC	CTSENT	NOGRT	OCDISC	OCOVF
09	R/W	INTEN7	INTEN6	INTEN5	INTEN4	INTEN3	INTEN2	INTEN1	INTEN0
0A	R/W	P1	P0	UNI	TRHENA	Reserved**		CTRDY	CRQSENT
0B	R/W	Reserved**				LINEDIV			
0C	R/W	ONLINE	Reserved**			DISCARD	QM	GFCENA	IFECN
0D	R/W	Reserved**							MRCIN
0E	R/W	Reserved**							
0F	R/W	TIME(7-0)							
10	R/W	CBRLEN(7-0)							
11	R/W	CBRLIMIT(7-0)							
12	R/W	VBRLIMIT(7-0)							
13	R/W	LBADDRL(7-0)							
14	R/W	Reserved**				LBADDRU(3-0)			
15	R/W	TRAL(7-0)							
16	R/W	TRAU(7-0)							
17	R/W	TRADATA(7-0)							

* RO = Read-Only; WO = Write-Only; RC = Read and Clear (bits remain set to 1 if causative condition persists); R/W = Read/Write; R = Register

** Note: Reserved addresses should not be accessed by the microprocessor. Reserved bit positions within used addresses may contain random values; in writable addresses, these bits should be set to 0.

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18	R	DISCCTR(7-0)							
19	R	MRCCTR(7-0)							
1A	R	HECERCTR(7-0)							
1B	R	INCELLL(7-0) (Lower Byte)							
1C	R	INCELLM(7-0) (Middle Byte)							
1D	R	INCELLU(7-0) (Upper Byte)							
1E	R	Reserved**							
1F	R	Reserved**							
20	RO	MRCHEAD0(7-0)							
21	RO	MRCHEAD1(7-0)							
22	RO	MRCHEAD2(7-0)							
23	RO	MRCHEAD3(7-0)							
24		Reserved**							
25-5F		Reserved**							
60	RO	CRQ0(7-0)							
61-92	RO	CRQ1(7-0) (61H) through CRQ50(7-0) (92H)							
93	RO	CRQ51(7-0)							
94-9F		Reserved**							
A0	R/W	CTQ0(7-0)							
A1-D6	R/W	CTQ1(7-0) (A1H) through CTQ54(7-0) (D6H)							
D7	R/W	CTQ55(7-0)							
D8-DF		Reserved**							
E0	R/W	MCASTN00(7-0)							
E1-FE	R/W	MCASTN01(7-0) (E1H) through MCASTN1E(7-0) (FEH)							
FF	R/W	MCASTN1F(7-0)							

MEMORY MAP DESCRIPTIONS

CONTROL BIT AND REGISTER DESCRIPTIONS

Address *	Bit	Symbol	Description
00-02 03	7-0 3-0	DEVID	Device identification code (28 bits).
03	7-4		Version number.
04	7-4		Mask revision level.
07	0	RESET	When set to 1, this bit clears the counters DISCCTR, MRCCTR, HECERCTR and INCELL (L, M and U) in addresses 18H thru 1DH.

* All addresses in memory map description tables are hexadecimal. Reserved addresses and bit positions are not listed.

INTERRUPT AND INTERRUPT-ENABLE BITS

Address	Bit	Symbol	Description
08	7	CRCF	Indication if CRC check error on cell from *CellBus* bus.
	6	CRQOVF	Indication of loss of an incoming control cell, due to overflow of the internal 4-cell control cell receive queue.
	5	CRQCAV	Indication that a control cell is present in the control cell receive queue, CRQ.
	4	INSOC	Indication of a cell inlet Start-of-Cell error occurrence.
	3	CTSENT	Indication that a control cell has been sent to the *CellBus* bus from the control cell transmit buffer.
	2	NOGRT	No bus access grant has been received by the inlet side, after a bus access request, within a time established by register TIME.
	1	OCDISC	Cell discarded due to FIFO length greater than VBRLIMIT, and DISCARD = 1, and CLP of the incoming cell = 1.
	0	OCOVF	Cell discarded due to overflow of outlet FIFO.
09	7	INTEN7	Interrupt enabled for CRCF, if = 1.
	6	INTEN6	Interrupt enabled for CRQOVF, if = 1.
	5	INTEN5	Interrupt enabled for CRQCAV, if = 1.
	4	INTEN4	Interrupt enabled for INSOC, if = 1.
	3	INTEN3	Interrupt enabled for CTSENT, if = 1.
	2	INTEN2	Interrupt enabled for NOGRT, if = 1.
	1	INTEN1	Interrupt enabled for OCDISC, if = 1.
	0	INTEN0	Interrupt enabled for OCOVF, if = 1.

DEVICE MODE CONTROL BITS

Address	Bit	Symbol	Description
0A	7, 6	P1, P0	Set bus access priority of this CUBIT device. Possible values are: high-priority, P1=1, P0=1; medium-priority, P1=1, P0=0; low-priority, P1=0, P0=1; no request, P1=0, P0=0.
	5	UNI	If = 1, UNI operation, VPI filled width = 8 bits. If = 0, NNI operation, VPI filled width = 12 bits.
	4	TRHENA	If THRENA = 1, enable insertion of Tandem Routing Header during address translation.
	1	CTRDY	Set to 1 by microprocessor to indicate that a control cell is ready to be sent. Cleared by CUBIT when done.
	0	CRQSENT	Set to 1 by the microprocessor to indicate that a control cell has been read from the CUBIT's control cell receive buffer. Cleared to 0 automatically by CUBIT.
0B	3-0	LINEDIV	Cell outlet and cell inlet clock frequency control. Frequency will be equal to *CellBus* bus read or write clock ($\overline{\text{CBRC}}$ and $\overline{\text{CBWC}}$) frequency divided by 2-to-the-power-LINEDIV, for the cell outlet and inlet, respectively.
0C	7	ONLINE	Operational status. If = 1, the CUBIT is on-line and all functions are operating. If = 0, the CUBIT is off-line. In off-line condition, no cells are accepted from the cell inlet, and only control and loopback cells are accepted from the bus. In the off-line condition, the cell interface outputs are in tri-state. After hardware reset, the ONLINE bit is set to 0.
	3	DISCARD	Allow cell discard. If = 1 and VBR queue size > VBRLIMIT, and if cell CLP = 1, then discard the cell, and index DISCCTR.
	2	QM	Outlet cell queue structure. One single 123-cell queue if QM=0. Split queue (Control, CBR, VBR, ABR) if QM = 1.
	1	GFCENA	Enable insertion of the state of pins GFC(3-0) into the GFC field of outgoing cells if = 1. State of GFC(3-0) is sampled on the rising edge of COCLK that precedes the first byte of the ATM cell header (see Figure 36).
	0	IFECN	Enable insertion of FECN if = 1. FECN (middle bit of PTI field) will be set =1 if the CBR or VBR FIFO length exceeds the congestion limits, and IFECN = 1.
0D	0	MRCIN	Indication that a misrouted cell has been received. Cleared by a write operation.
0F	7-0	TIME	Time-out counter preset value for bus access watchdog timer. If timer expires after a request is made, and before a grant is received, alarm bit NOGRT is set. Units are bus frame cycles.

OUTLET CELL FIFO SIZE AND LIMIT CONTROLS

Address	Bit	Symbol	Description
10	7-0	CBRLEN	Length (in cells) of the CBR section of the cell outlet FIFO. Valid values are zero through 89.
11	7-0	CBRLIMIT	Congestion size (in cells) for CBR FIFO. FECN may be set if CBR FIFO length is greater than this value and IFECN = 1.
12	7-0	VBRLIMIT	Congestion size (in cells) for VBR FIFO. FECN may be set if VBR FIFO length is greater than this value and IFECN = 1. Cells may be discarded if length greater than this value and DISCARD = 1, and the arriving cell has CLP = 1.

LOOPBACK CONTROL ADDRESS

Address	Bit	Symbol	Description
13	7-0	LBADDRL	8 LSB of Loopback Routing Header, bits 11-4 of *CellBus* Bus Routing Header (see Figure 24).
14	3-0	LBADDRU	4 MSB of Loopback Routing Header, bits 15-12 of *CellBus* Bus Routing Header (see Figure 24).

TRANSLATION RAM READ/WRITE CONTROL

Address	Bit	Symbol	Description
15	7-0	TRAL	8 LSB of the translation RAM address.
16	7-0	TRAU	8 MSB of the translation RAM address.
17	7-0	TRADATA	Data read from, or to be written into, the translation RAM at the above address.

COUNTERS AND MISROUTED CELL HEADER

Address	Bit	Symbol	Description
18	7-0	DISCCTR	Count of cells discarded at input to outlet-side FIFO.
19	7-0	MRCCTR	Count of cell inlet mis-routed cells received.
1A	7-0	HECERCTR	Count of cells at cell inlet having a HEC error indication.
1B	7-0	INCELLL	Bits 7-0 (8 LSB) of count of incoming cells.
1C	7-0	INCELLM	Bits 15-8 of count of incoming cells.
1D	7-0	INCELLU	Bits 23-16 (8 MSB) of count of incoming cells.
20	7-0	MRCHEAD0	First (least significant) byte of the header of the first misrouted cell received after this buffer was last cleared.
21	7-0	MRCHEAD1	Second byte of above header.
22	7-0	MRCHEAD2	Third byte of above header.
23	7-0	MRCHEAD3	Fourth (most significant) byte of above header.

CONTROL CELL SEND AND RECEIVE QUEUES

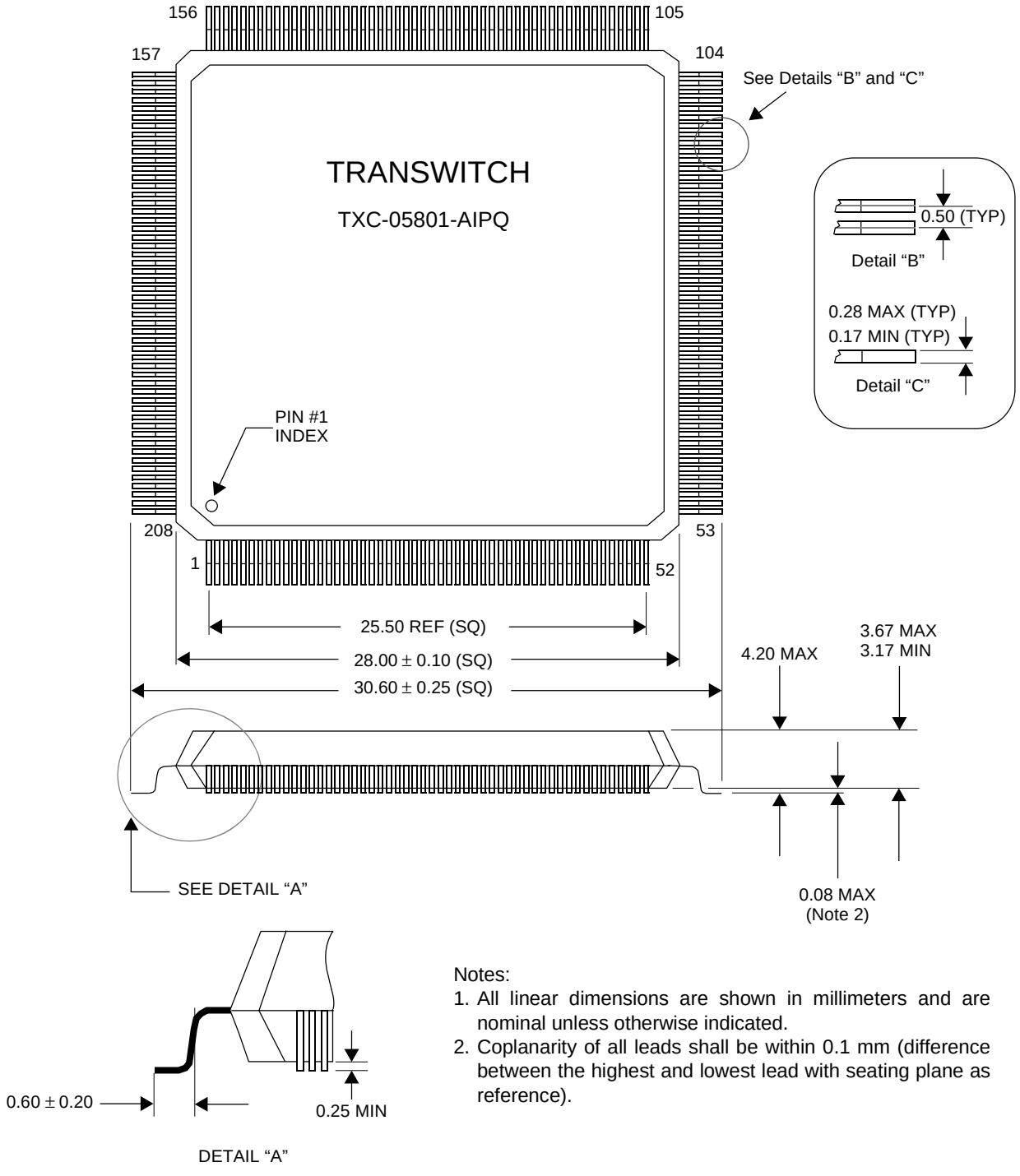
Address	Bit	Symbol	Description
60-93	7-0	CRQi	Control cell receive buffer, 52 bytes (i = 0 - 51).
A0-D7	7-0	CTQi	Control cell transmit buffer, 56 bytes (i = 0 - 55).

MULTICAST NUMBER MEMORY

Address	Bit	Symbol	Description
E0	7-0	MCASTN00	Multicast session RX enable bits, channels 7-0, (relative address zero decimal, bits 7-0).
E1-FE	7-0	MCASTN01-MCASTN1E	Multicast session RX enable bits for channels 15-8, 23-16, . . . , 247-240, relative addresses 1 to 30 decimal.
FF	7-0	MCASTN1F	Multicast session RX enable bits, channels 255-248 (relative address 31 decimal, bits 7-0).

PACKAGE INFORMATION

The CUBIT device is available in a 208-pin plastic quad flat package (PQFP) suitable for surface mounting, as shown in Figure 44.



Notes:
1. All linear dimensions are shown in millimeters and are nominal unless otherwise indicated.
2. Coplanarity of all leads shall be within 0.1 mm (difference between the highest and lowest lead with seating plane as reference).

Figure 44. CUBIT TXC-05801 208-Pin Plastic Quad Flat Package

ORDERING INFORMATION

Part Number: TXC-05801-AIPQ 208-pin Plastic Quad Flat Package (PQFP)

RELATED PRODUCTS

Figure 45 illustrates typical applications of the CUBIT *CellBus* Bus Switch device in a generic architecture for ATM access switching. The other TranSwitch devices included in this diagram are briefly described below:

TXC-03003B, SOT-3 VLSI Device (STM-1, STS-3, STS-3c Overhead Terminator). This device performs all the functions for section, line and path overhead processing of STM-1, STS-3 or STS-3c signals, providing access to all overhead bytes. It performs pointer justification and payload tracking, alarm detection and generation, and performance monitoring.

TXC-03102, QDS1F VLSI Device (Quad DS1 Framer). A 4-channel DS1 (1.544 Mbit/s) framer for voice and data applications. This device handles all logical interfacing functionality to a T1 line. This device is not recommended for use in new designs, which should use QT1F-*Plus*.

TXC-03103, QT1F-*Plus* VLSI Device (Quad T1 Framer-*Plus*). A 4-channel DS1 (1.544 Mbit/s) framer designed with extended features for voice and data applications.

TXC-05150, CDB VLSI Device (Cell Delineation Block). Extracts/inserts ATM cells from/to DS1, DS3, E1, STS-1, STS-3c or STM-1 line interface signals. Serial, byte and nibble interfaces operate from 1.544 to 155.52 Mbit/s.

TXC-05501 and TXC-05601, SARA-S and SARA-R VLSI Devices (Segmentation and Reassembly). A two-chip set for implementation of the ATM Adaptation Layers (AAL) 3, 4, and 5 at line rates from DS1 (1.544 Mbit/s) up to STS-3c/STM-1 (155.52 Mbit/s).

TXC-05551, SARA-2 ATM Cell Processing IC Device. Used with application-specific microcode to perform complete segmentation and reassembly (SAR) for implementing ATM adapter cards, legacy LAN to ATM hubs, and routers. PCI-based host interface. Supports CBR, VBR and UBR services. Integrated SONET/SDH framer.

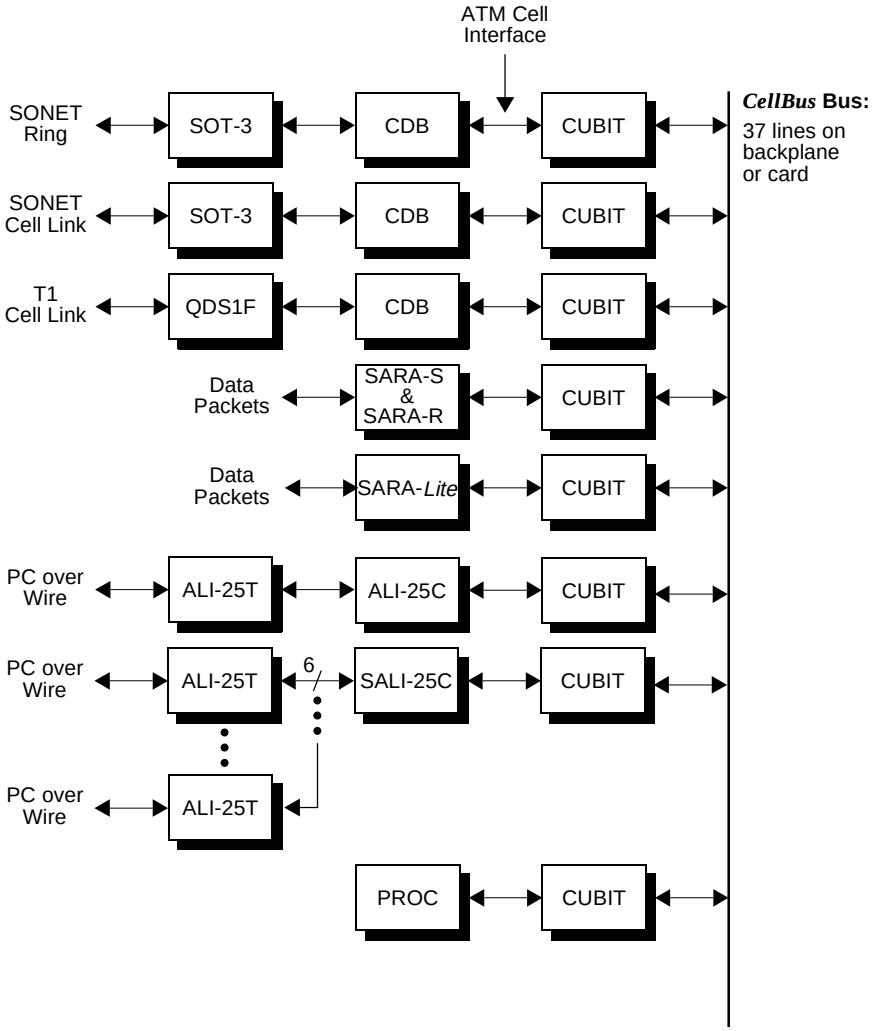
TXC-05551/L, SARA-*Lite* ATM AAL0/5 Segmentation and Reassembly Product (combination of SARA-2 device and microcode that provides it with SARA-Lite functionality)

TXC-05802, CUBIT-*Pro* VLSI Device (*CellBus* Bus Switch). This is the next generation device that provides more features than the CUBIT, which is no longer recommended for use in new designs.

TXC-07025, ALI-25 VLSI Chip Set (ATM Line Interface). Controller and Transceiver devices together provide the complete ATM 25 Mbit/s physical layer function (TC, PMD) and operate over existing STP or UTP-3, 4, 5 cable plant.

TXC-07625, SALI-25C VLSI Device (Six ATM Line Interface at 25 Mbit/s). Six channel 25.6 Mbit/s ATM transmission convergence function for twisted pair cable. Supports UTOPIA Level 1 and 2. Provides multicasting capability and 4 level priority queuing.

Figure 45. CUBIT and Related Product Applications in ATM Access Switching



STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

The ATM Forum:

ATM Forum World Headquarters
303 Vintage Park Drive
Foster City, CA 94404-1138

Tel: 415-578-6860
Fax: 415-525-0182

ATM Forum European Office
14 Place Marie - Jeanne Bassot
Levallois Perret Cedex
92593 Paris France

Tel: 33 1 46 39 56 26
Fax: 33 1 46 39 56 99

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

EIA - Electronic Industries Association (U.S.A.):

Global Engineering Documents
Suite 407
7730 Carondelet Avenue
Clayton, MO 63105

Tel: 800-854-7179 (In U.S.A.)
Fax: 314-726-6418

ITU-T (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (T)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

MIL-STD Military Standard (U.S.A.):

Standardization Documents Order Desk
700 Robbins Avenue
Building 4D
Philadelphia, PA 19111-5094

Tel: 212-697-1187
Fax: 215-697-2978

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated CUBIT Data Sheet that have significant differences relative to the previous and now superseded CUBIT Data Sheet:

Updated CUBIT Data Sheet:	Edition 5, June 1998
Previous CUBIT Data Sheet:	Edition 4, August 1996

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
1, 72, 74	Changed TranSwitch street address in Shelton, CT.
3-4	Updated Table of Contents and added note. Updated List of Figures.
25	Modified first paragraph of Interrupts subsection.
32	Changed pin 8 $\overline{\text{FRCABRCNG}}$ Symbol to FRCABRCNG and changed Description to active high.
36	Added last column, last five rows and second note to first (renamed Absolute Maximum Ratings and Environmental Limitations) table. Deleted its operating junction temperature row. Moved ambient operating temperature row of last (renamed) table to be above the five added rows in the first table. Added first row to last table.
40-42	Modified waveform diagrams and tables. Added Note 1.
43-46, 49-50, 54-57	Modified waveform diagrams and tables. Added connection diagrams on pages 49 and 50.
47	Modified waveform diagrams and tables. Added Notes 1 and 2.
48	Modified table.
52	Modified table and added note.
65	Added part number to top view of device in figure.
66-67	Updated Related Products section.
68-69	Added EIA and MIL-STD.
70	Replaced List of Data Sheet Changes.
73	Updated Documentation Update Registration Form.

- NOTES -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