ADMA-T1 Device
DS1 to VT1.5 Async Mapper-Desync
TXC-04001

DATA SHEET

FEATURES

- Add/drop two DS1s from SONET bus through asynchronous VT1.5 mapping
- Handles both STS and VT pointer tracking
- Monitors bus parity, SONET loss of pointer, and VT loss of pointer
- Records VT pointer increment and decrement counts, FEBE counts, BIP-2 error counts, yellow, VTAIS, and signal label of the selected VT1.5
- Selectable AMI, B8ZS or NRZ DS1 interface
- Reports received AMI or B8ZS coding error count
- Microprocessor programmable DS1 loopback, send VT yellow, send VTAIS, transmit VT label and generate timed BIP-2 errors
- Contains digital desynchronizers which assure Bellcore Category I jitter performance

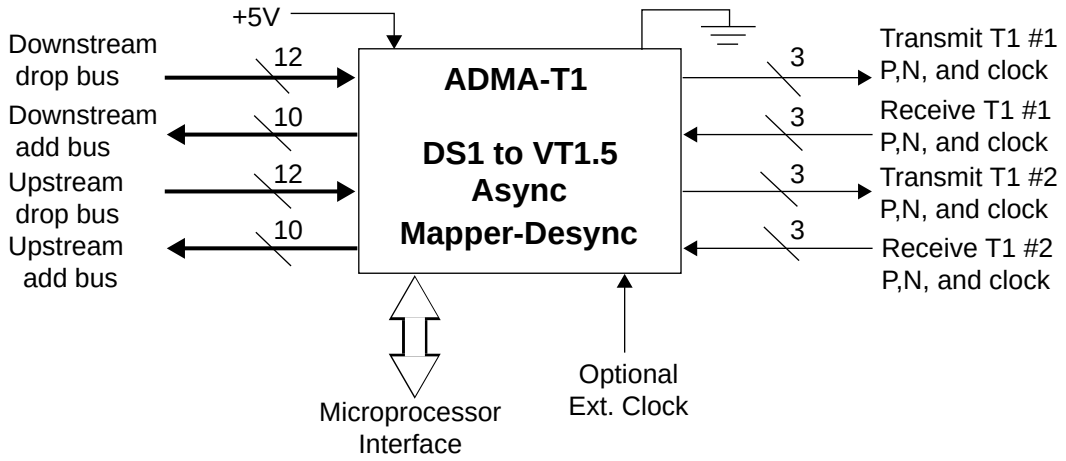
DESCRIPTION

Under software control, TranSwitch's ADMA-T1 interconnects two DS1 signals with any two asynchronous mode VT1.5 virtual tributaries carried in STS-1 rate SPE (SONET Payload Envelope). The bus interface facilitates a convenient modular growth of terminal or add/drop applications. In addition to providing on-board codecs for AMI and B8ZS, the device includes digital circuits that minimize the effects of pointer movement and jitter. The DS1 interface consists of clock and P and N rail signals compatible with many commercially available DS1 interface devices.

The STS-1 inputs to the ADMA-T1 contain full SONET overheads, as well as VT1.5 payloads. The bus output of the ADMA is two VT1.5 signals. SONET overheads are added by other SONET devices, such as the TXC-03001, SOT-1, as required.

APPLICATIONS

- SONET add/drop multiplexer
- SONET terminations
- SONET/DS1 RSU or DLC
- Wideband DCS, EDX
- SONET test equipment



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TranSwitch Corporation • 8 Progress Drive • Shelton, CT 06484 • USA • Tel: 203-929-8810 • Fax: 203-926-9453

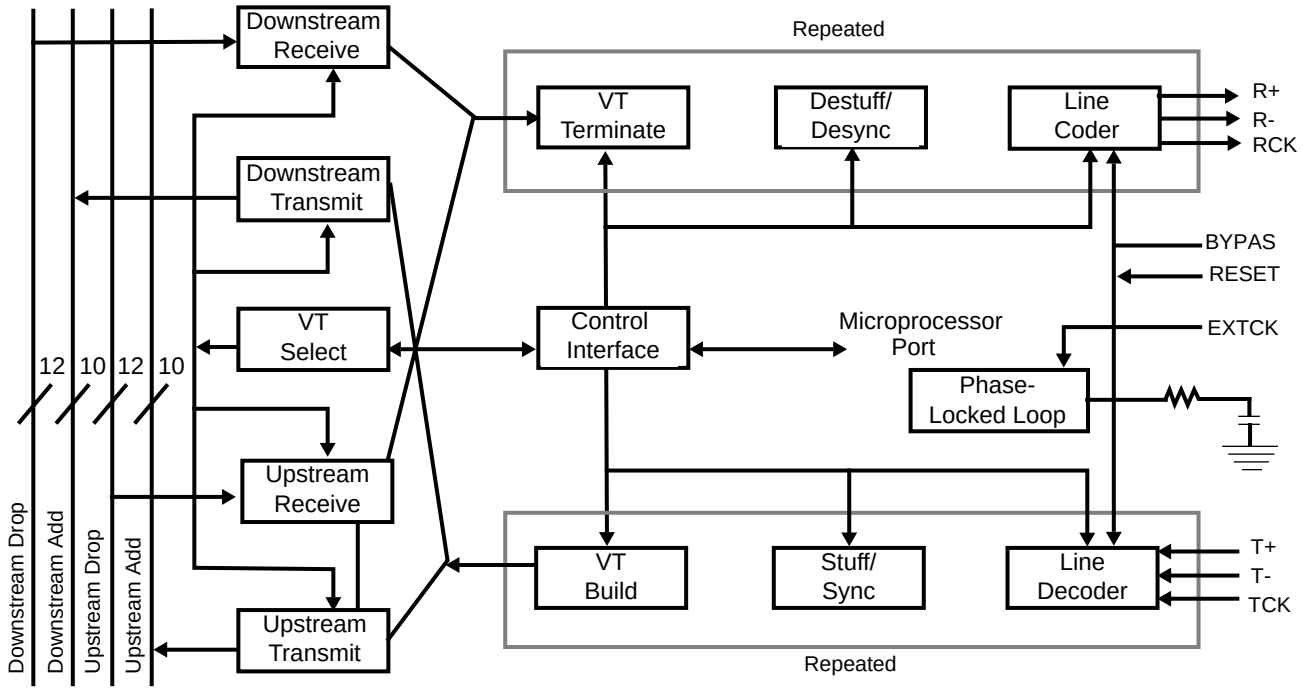


Figure 1. ADMA-T1 Block Diagram

BLOCK DIAGRAM DESCRIPTION

The block diagram for the ADMA-T1 is shown in Figure 1. The ADMA-T1 connections to the four drop and add bus segments are also shown. The ADMA-T1 supports a SONET bidirectional add/drop multiplexer architecture in which up to two DS1 channels may be dropped from either bus or from one bus. In a typical add/drop multiplexer application, a DS1 channel is dropped from a downstream drop bus, and added to the upstream add bus. Likewise, a DS1 channel dropped from the upstream drop bus is added to the downstream add bus. Timing for an add bus is derived from the like named drop bus, e.g., timing for the downstream add bus is derived from the downstream drop bus.

Receive SONET to DS1

The Downstream Receive and Upstream Receive Blocks are identical. The VT selection from the STS-1 payload is determined by the Control Interface Block with an instruction written by the microprocessor. Twelve leads connect a drop bus to a receive block: byte-wide data at 6.48 Mbytes per second, a clock signal, a payload present indicator signal, a C1/J1 indicator signal, and odd parity. A receive block performs STS pointer tracking, SPE extraction, and VT channel selection. The output of a receiver block is connected to the VT Terminate Block.

The VT Terminate Block extracts the VT and performs the following functions: VT pointer processing, valid pointer detection with positive and negative stuff occurrences, BIP-2 parity calculation and error counting, FEBE counting, and VT yellow alarm detection. In addition, the signal label contained in the V5 byte is provided in the memory map.

In the Destuff/Desync Block, the DS1 signal is extracted from the VT SPE. A pointer leak FIFO is provided to absorb the effects of VT pointer movements. A phase-locked loop (PLL) is used to track the frequency of the received DS1 signal and to remove transmission and stuffing jitter. The PLL uses a 6.48 MHz drop clock and an external RC for operation. An option is provided to select an external 51.84 MHz clock, which is connected to the signal lead EXTCK.

The Line Coder Block formats the DS1 serial bit stream into either an AMI or B8ZS signal. Positive and negative rail signals are provided with a clock signal. The Line Coder Block can also be bypassed, with the NRZ signal provided on the positive rail lead.

Transmit DS1 to SONET

In the transmit direction, toward an add bus, the Line Decoder Block regenerates a DS1 NRZ serial bit stream from either an AMI or a B8ZS line coded signal. An option is provided for bypassing the Decoder Block for NRZ operation.

The Stuff/Sync Block buffers the incoming DS1 signal using a FIFO which is used to bit stuff the data into the SPE of an asynchronous VT. The ADMA-T1 accepts a 1.544 Mbit/s +/- 130 ppm DS1 signal having an input jitter tolerance that satisfies the Category 1 standard (+/- 5 UI of peak jitter) specified in Bellcore's TR-TSY-000499, Issue 3, December 3, 1989 document. This block operates in conjunction with the VT Build Block.

Figure 2. ADMA-T1 Output Byte Order

V1
V5
R R R R R R I R
BYTE 1
*
*
BYTE 24
V2
R R R R R R R R
C1 C2 O O O O I R
BYTE 1
*
*
BYTE 24
V3
R R R R R R R R
C1 C2 O O O O I R
BYTE 1
*
*
BYTE 24
V4
R R R R R R R R
C1 C2 O O O S1 S2 R
BYTE 1
*
*
BYTE 24

The VT Build Block forms the asynchronous VT to be transmitted. This block requests DS1 bits from the Stuff/Sync Block along with timing information to indicate the number of bits in the FIFO for stuffing. The VT is generated with a pointer value fixed at a decimal value of 78. The format of the VT1.5 is shown in Figure 2.

The VT Build Block accepts timing information from either the downstream or upstream drop bus for transmit timing, and accepts control information from the Control Interface Block for the VT selection. The VT overhead byte is shown in Figure 3. The VT Build Block calculates the BIP-2 parity, and formats the information into the V5 byte.

Figure 3. Byte V5 Structure

BIP-2		FEBE	X	SIGNAL LABEL			YELLOW
				L_1	L_2	L_3	
1	2	3	4	5	6	7	8

Bit Numbers

The Upstream and Downstream Transmit Blocks place the formatted signals onto an add bus. A tristate interface is used. Data is present only for the VT time slots that are to be added to the bus. In addition, odd parity and add pulses are generated which correspond to the VT time slots.

PIN DIAGRAM

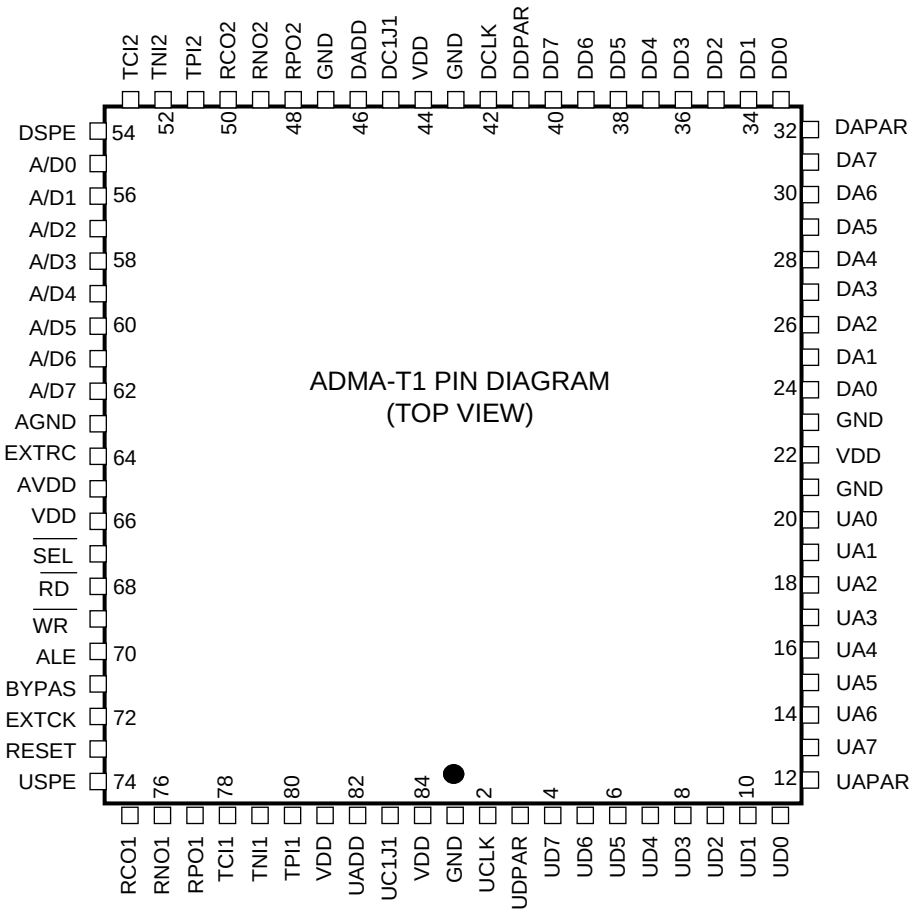


Figure 4. ADMA-T1 Pin Diagram With Numbers and Names

PIN DESCRIPTIONS

Power Supply and Ground:

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	22,44,66,81,84	P		**VDD:** 5-volt supply voltage, ±5%.
GND	1,21,23,43,47	P		**Ground:** 0 volts reference
AVDD	65	P	Analog	**Analog VDD:** 5-volt power supply for the PLL
AGND	63	P	Analog	**Analog Ground:** Ground for the PLL

*Note: I = Input; O = Output; P = Power

PIN DESCRIPTIONS (continued)

Upstream Bus I/O:

Symbol	Pin No.	I/O/P	Type	Name/Function
UCLK	2	I	TTL	**Upstream Drop Clock:** This 6.48 MHz input clock samples UDn, UDPAR, USPE and UC1J1 signals on the falling edge. UAn, UADD, and UAPAR are clocked out on the rising edge of UCLK during the time slot corresponding to the appropriate VT which is selected by software.
UDPAR	3	I	TTLp	**Upstream Drop Parity Bit:** The ADMA-T1 expects an odd parity signal representing a parity calculation over UDn.
UD(7-0)	4-11	I	TTLp	**Upstream Drop Data Byte:** Byte-wide input data corresponding to the STS-1 signal. The MSB is bit 7 (pin 4).
USPE	74	I	TTLp	**Upstream Drop Payload Present Indicator:** This input is high following the last line or section overhead byte in a subframe row and remains high for all SONET Payload Envelope (SPE) bytes. During stuffing, it will be high during negative stuff bytes and low during positive stuff bytes.
UC1J1	83	I	TTLp	**Upstream Drop C1/J1 Byte Indicators:** This input indicates the location of the C1 and the J1 overhead bytes in the STS-1 signal.
UAPAR	12	O (tristate)	CMOS4mA	**Upstream Add Parity Bit:** An odd-parity output signal calculated over the UAn data. This tristate output is only active when VT data is being output.
UA(7-0)	13-20	O (tristate)	CMOS4mA	**Upstream Add Data Byte:** Byte-wide output data corresponding to the selected VT1.5 STS-1 signal. These tristate outputs are only active when VT data is being output. Up to 14 ADMAs may be wire-ored together.
UADD	82	O	TTL4mA	**Upstream Add Data Present Indicator:** This signal is high whenever upstream add data is being clocked out from the ADMA-T1.

PIN DESCRIPTIONS (continued)

Downstream Bus I/O:

Symbol	Pin No.	I/O/P	Type	Name/Function
DCLK	42	I	TTL	**Downstream Drop Clock:** This 6.48 MHz input clock samples DDn, DDPAR, DSPE and DC1J1 signals on the falling edge. DAn, DADD, and DAPAR are clocked out on the rising edge of DCLK during the time slot corresponding to the appropriate VT which is selected by software.
DDPAR	41	I	TTLp	**Downstream Drop Parity Bit:** The ADMA-T1 expects an odd-parity signal representing a parity calculation over DDn.
DD(0-7)	33-40	I	TTLp	**Downstream Drop Data Byte**: Byte-wide input data corresponding to the STS-1 signal. The MSB is bit 7.
DSPE	54	I	TTLp	**Downstream Drop Payload Present Indicator:** This input is high following the last line or section overhead byte in a subframe row, or remains high for all SPE bytes. During stuffing, it will be high during negative stuff bytes and low during positive stuff bytes.
DC1J1	45	I	TTLp	**Downstream Drop C1/J1 Byte Indicators:** This input must go high during the time of C1 and J1 overhead bytes.
DAPAR	32	O (tristate)	CMOS4mA	**Downstream Add Parity Bit:** An odd-parity output signal calculated over the UAn data. This tristate output is active only when VT data is being output.
DA(0-7)	24-31	O (tristate)	CMOS4mA	**Downstream Add Data Byte:** Byte-wide output data corresponding to the selected VT1.5 of the STS-1 signal. These tristate outputs are active only when VT data is being output. Up to 14 ADMAs may be wire-ored together.
DADD	46	O	TTL4mA	**Downstream Add Data Present Indicator:** This signal is high whenever upstream add data is being clocked out from the ADMA.

PIN DESCRIPTIONS (continued)

DS1 Port 1 I/O:

Symbol	Pin No.	I/O/P	Type	Name/Function
RCO1	75	O	TTL4mA	**DS1 Output Clock, Port 1:** A clock output of 1.544 MHz. Data is clocked out of the ADMA-T1 on the rising edge of RCO1.
RPO1	77	O	TTL4mA	**DS1 Positive Output Pulse, Port 1:** When the ADMA-T1 is operating in the P&N rail mode, the P rail information appears on this pin. When operating in the bypass mode, the non-coded NRZ data appears here.
RNO1	76	O	TTL4mA	**DS1 Negative Output Pulse, Port 1:** When the ADMA-T1 is operating in the P&N rail mode, the N rail information appears on this pin. When operating in the bypass mode, this pin is not used.
TCI1	78	I	TTLp	**DS1 Input Clock, Port 1:** A clock input of 1.544 MHz is required. Data is clocked into the ADMA-T1 on the falling edge of TCI1.
TPI1	80	I	TTLp	**DS1 Positive Input Pulse, Port 1:** When the ADMA-T1 is operating in the P&N rail mode, the P rail information appears on this pin. When operating in the bypass mode, this pin provides non-coded NRZ data.
TNI1	79	I	TTLp	**DS1 Negative Input Pulse, Port 1:** When the ADMA-T1 is operating in the P&N rail mode, the N rail information appears on this pin. When operating in the bypass mode, this pin is not used and should be connected to ground.

PIN DESCRIPTIONS (continued)

DS1 Port 2 I/O:

Symbol	Pin No.	I/O/P	Type	Name/Function
RCO2	50	O	TTL4mA	**DS1 Output Clock, Port 2:** A clock output of 1.544 MHz. Data is clocked out of the ADMA-T1 on the rising edge of RCO2.
RPO2	48	O	TTL4mA	**DS1 Positive Output Pulse, Port 2:** When the ADMA-T1 is operating in the P&N rail mode, the P rail information appears on this pin. When operating in the bypass mode, the non-coded NRZ data appears here.
RNO2	49	O	TTL4mA	**DS1 Negative Output Pulse, Port 2:** When the ADMA-T1 is operating in the P&N rail mode, the N rail information appears on this pin. When operating in the bypass mode, this pin is not used.
TCI2	53	I	TTLp	**DS1 Input Clock, Port 2:** A clock input of 1.544 MHz is required. Data is clocked into the ADMA-T1 on the falling edge of TCI2.
TPI2	51	I	TTLp	**DS1 Positive Input Pulse, Port 2:** When the ADMA-T1 is operating in the P&N rail mode, the P rail information appears on this pin. When operating in the bypass mode, this pin provides non-coded NRZ data.
TNI2	52	I	TTLp	**DS1 Negative Input Pulse, Port 2:** When the ADMA-T1 is operating in the P&N rail mode, the N rail information appears on this pin. When operating in the bypass mode, this pin is not used and should be connected to ground.

PIN DESCRIPTIONS (continued)

Microprocessor Bus:

Symbol	Pin No.	I/O/P	Type	Name/Function
A/D(0-7)	55-62	I/O	TTL8mA	**Address/Data Bus:** An 8-bit, time-multiplexed address and data bus.
$\overline{SEL}$	67	I	TTLp	**Select Lead:** A logic low signal on this pin indicates that the ADMA-T1 has been selected for a read/write operation.
$\overline{RD}$	68	I	TTLp	**Microprocessor Read Control:** This signal represents a microprocessor read operation (active low). When the ADMA-T1 is selected via the $\overline{SEL}$ pin, the $\overline{RD}$ signal enables the ADMA-T1 to place data from the selected register on the A/D bus.
$\overline{WR}$	69	I	TTLp	**Microprocessor Write Control:** This signal represents a microprocessor write operation (active low). When the ADMA-T1 is selected via the $\overline{SEL}$ pin, the $\overline{WR}$ signal causes the ADMA-T1 to load data on the A/D bus into the selected register.
ALE	70	I	TTLp	**Microprocessor Address Latch Enable:** A logic high on this line indicates that the information present on the A/D bus represents an address. The ADMA-T1 latches the address information with the falling edge of ALE.

Controls:

Symbol	Pin No.	I/O/P	Type	Name/Function
BYPAS	71	I	TTLp	**Bypass Pin:** If this lead is high and the value 04(HEX) is written to register 1E(HEX), the ADMA-T1 bypasses the internal codecs. NRZ DS1 data is provided on the TP/RP pins. When held low (grounded), a positive/negative rail AMI/B8ZS DS1 signal is provided.
EXTCK	72	I	TTL	**External Reference Clock**: A 51.84 MHz clock that has a duty cycle of 50% ±10% is applied to this pin when the external clock reference is selected by software. Otherwise, this pin is grounded.
RESET	73	I	TTLp	**Reset**: The RESET pin must be pulsed high for a minimum of 150 nanoseconds after power becomes stable. This clears all internal registers and initializes the internal FIFOs.
EXTRC	64	--	Analog	**External Series RC Network** (R=1.2K Ohms/ C=1000 picofarads): These external components are required when the internal PLL is used. The resistor is connected to pin 64 and the capacitor to ground.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	7	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Continuous power dissipation	P_C	225	300	mW
Ambient operating temperature	T_A	-40	85	^oC
Operating junction temperature	T_J		150	^oC
Storage temperature range	T_S	-55	150	^oC

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal res - junc to ambient	--	32	34	$^oC/W$	

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5	5.25	V	
V_{ANALOG}	4.75	5	5.25	V	
I_{DD}		45	57	mA	
I_{ANALOG}		2	5	mA	
P_{DD}		225	300	mW	Inputs switching
P_{ANALOG}		10	27	mW	

INPUT, OUTPUT, AND I/O PARAMETERS

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Input Parameters For TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		0.5	1.4	mA	$V_{DD} = 5.25$; Input = 0 volts
Input capacitance		5.5		pF	

Note: Input has a 9K (nominal) internal pull-up resistor.

Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -2mA$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 4mA$
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.8	6.5	9.2	ns	$C_{LOAD} = 15pF$
t_{FALL}	1.3	2.3	3.4	ns	$C_{LOAD} = 15pF$

Output Parameters For CMOS4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -4mA$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 4mA$
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	1.4	2.9	4.2	ns	$C_{LOAD} = 15pF$
t_{FALL}	1.3	2.3	3.4	ns	$C_{LOAD} = 15pF$

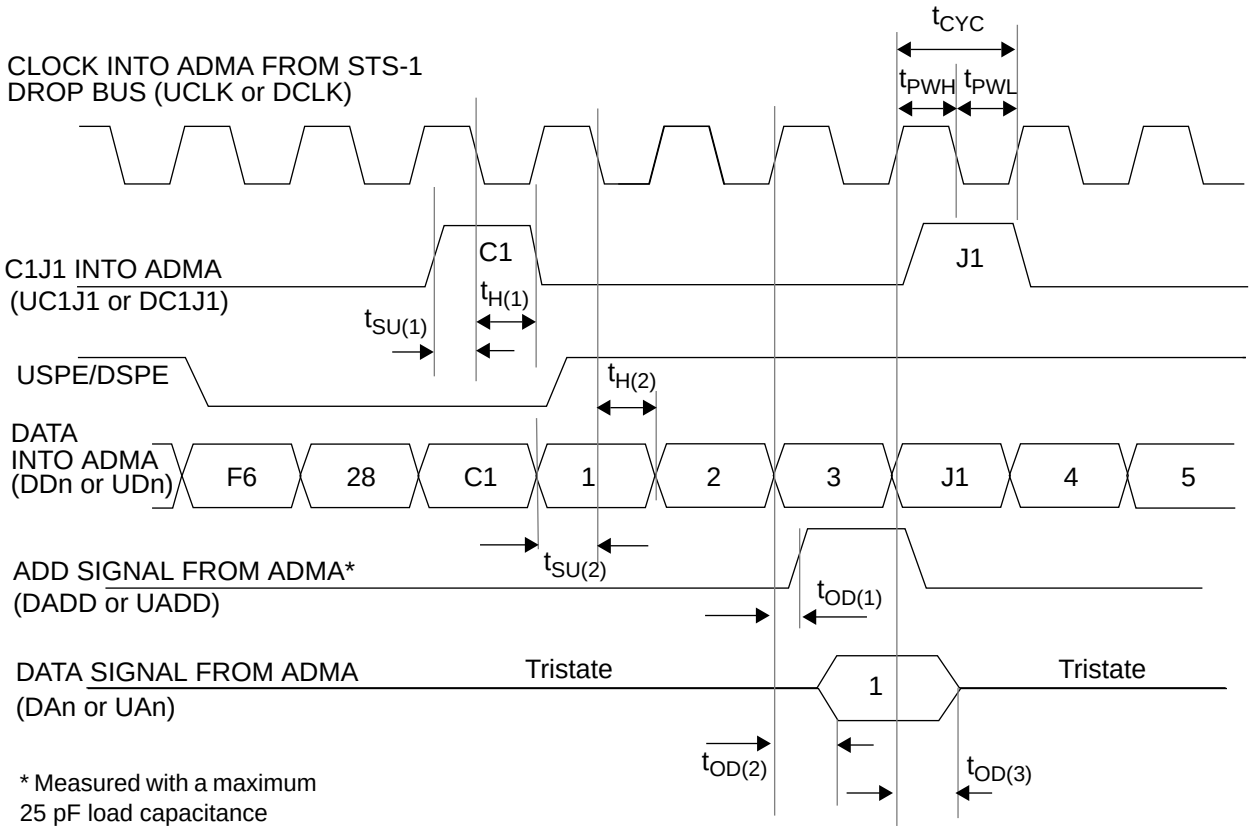
Input/Output Parameters For TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -4mA$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 8mA$
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	2.4	4.9	7.0	ns	$C_{LOAD} = 25pF$
t_{FALL}	1.1	1.8	2.5	ns	$C_{LOAD} = 25pF$

TIMING CHARACTERISTICS

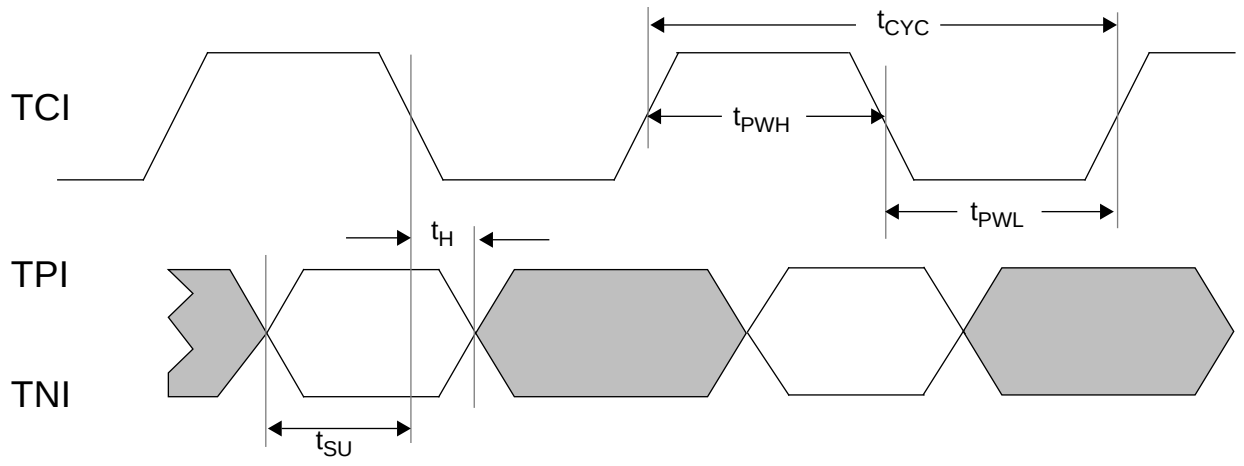
Detailed timing diagrams for the ADMA-T1 are illustrated in Figures 5 through 9, with values of the timing intervals following each figure. All output times are measured with a maximum 75 pF load capacitance. Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

Figure 5. STS-1 I/O Timing



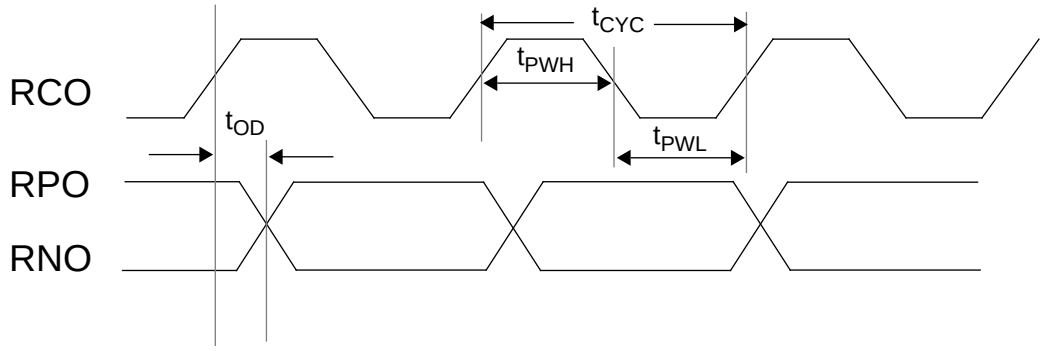
Parameter	Symbol	Min	Typ	Max	Unit
SPE and C1J1 set-up time to CLK ↓	$t_{SU(1)}$	12			ns
SPE and C1J1 hold time after CLK ↓	$t_{H(1)}$	5			ns
UD or DD data set-up time to CLK ↓	$t_{SU(2)}$	-5	0		ns
UD or DD data hold time after CLK ↓	$t_{H(2)}$	10			ns
ADD pulse output delay after CLK ↑	$t_{OD(1)}$	18.5	20.5	31.3	ns
ADD data output delay (tristate to data valid) after CLK ↑	$t_{OD(2)}$	21.5	23.5	36	ns
ADD data output delay (data valid to tristate) after CLK ↑	$t_{OD(3)}$	20.5	23	36	ns
CLK period	t_{CYC}		154.32		ns
CLK high time	t_{PWH}	20	77	92	ns
CLK low time	t_{PWL}	62			ns

Figure 6. DS1 Input Timing



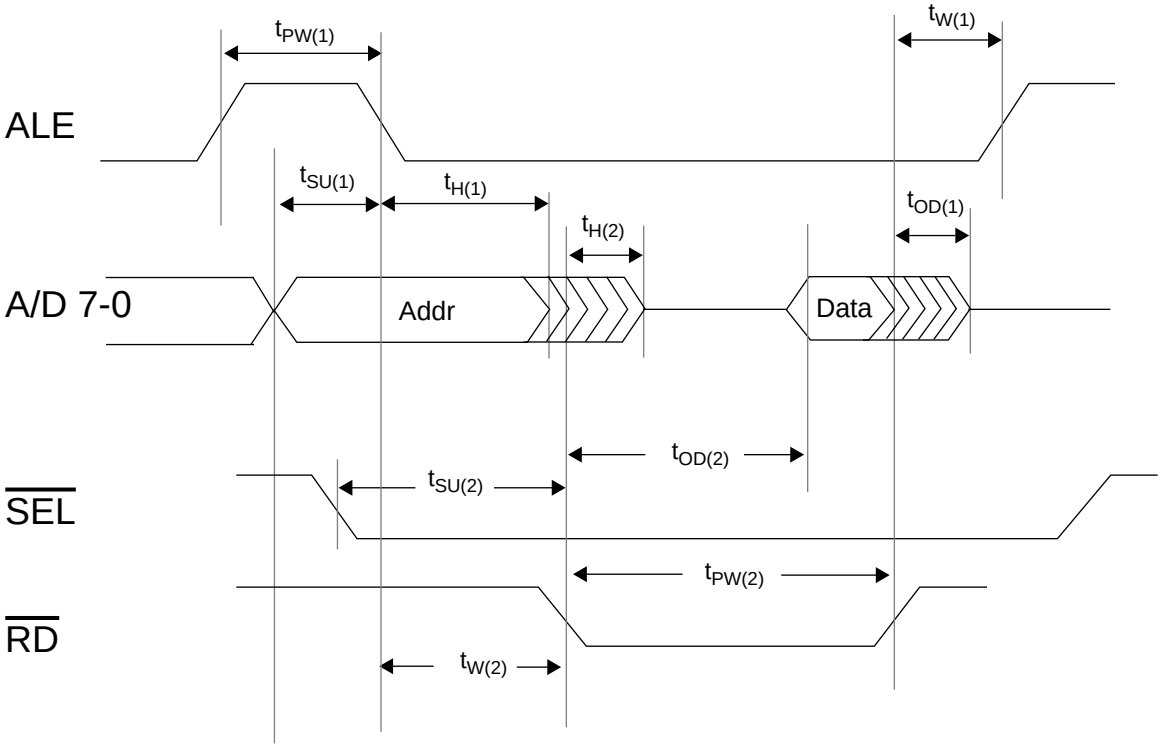
Parameter	Symbol	Min	Typ	Max	Unit
TPI/TNI set-up time to TCI ↓	t_{SU}	50			ns
TPI/TNI hold time after TCI ↓	t_H	20			ns
TCI clock period	t_{CYC}	560	647.67		ns
TCI high time	t_{PWH}	280			ns
TCI low time	t_{PWL}	280			ns

Figure 7. DS1 Output Timing



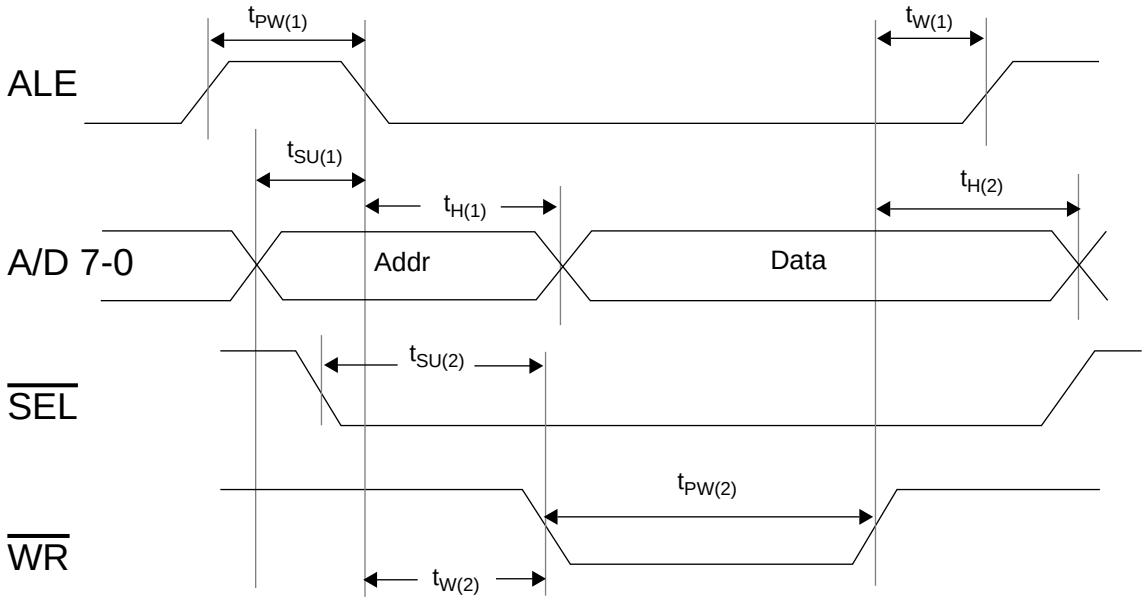
Parameter	Symbol	Min	Typ	Max	Unit
RPO/RNO output delay after RCO↑	t_{OD}	-6	0	1	ns
RCO high time	t_{PWH}	309	--	328	ns
RCO low time	t_{PWL}	--	328	--	ns
RCO clock period	t_{CYC}	637	--	656	ns

Figure 8. Microprocessor Read Cycle



Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	50			ns
ALE wait after $\overline{RD}$ ↑	$t_{W(1)}$	10			ns
Addr set-up time to ALE ↓	$t_{SU(1)}$	30			ns
Addr hold time after ALE ↓	$t_{H(1)}$	10			ns
Addr hold time after $\overline{RD}$ ↓	$t_{H(2)}$			50	ns
Data output delay after $\overline{RD}$ ↓	$t_{OD(2)}$			200	ns
Data output delay (to tristate) after $\overline{RD}$ ↑	$t_{OD(1)}$	20		50	ns
$\overline{SEL}$ set-up time to $\overline{RD}$ ↓	$t_{SU(2)}$	0			ns
$\overline{RD}$ pulse width	$t_{PW(2)}$	200			ns
$\overline{RD}$ wait after ALE ↓	$t_{W(2)}$	50			ns

Figure 9. Microprocessor Write Cycle



Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	50			ns
ALE wait after $\overline{WR}$ ↑	$t_{W(1)}$	10			ns
Addr set-up time to ALE ↓	$t_{SU(1)}$	30			ns
Addr hold time after ALE ↓	$t_{H(1)}$	10			ns
Data hold time after $\overline{WR}$ ↑	$t_{H(2)}$	20			ns
$\overline{SEL}$ set-up time to $\overline{WR}$ ↓	$t_{SU(2)}$	0			ns
$\overline{WR}$ pulse width	$t_{PW(2)}$	200			ns
$\overline{WR}$ wait after ALE ↓	$t_{W(2)}$	50			ns

OPERATION

ADMA-T1 Register Bit Map

The ADMA-T1 bit map is divided into two parts: DS1 port 1 and DS1 port 2. The signal bit names are identical for the two ports and have corresponding addresses. All of the STS errors are mapped into the two “drop” registers: 07H (Upstream Drop) and 0FH (Downstream Drop).

DS1 PORT 1

Address (Hex)	Status*	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	R/W	U/$\overline{D}$	--	--	VT1.5#				
01	R	VTAIS	BIP-2 error count						
02	R	VTLOP	FEBE count						
03	R	Neg. stuff count		Pos. stuff count		RX YEL	RX LABEL L_1	L_2	L_3
04	R/W	T1LOOP	--	1	TX VTAIS	B8ZS	TX LABEL L_3	L_2	L_1
05	R	--	--	--	--	--	VTNDF	FIFO error	
06	W	TX YEL	Generate BIP-2 error multiframe timer						
07	R	--	--	--	--	PAR	STS LOP	--	--
10	R	Coding violation counter (CERR)							

DS1 PORT 2

Address (Hex)	Status*	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08	R/W	U/$\overline{D}$	--	--	VT1.5#				
09	R	VTAIS	BIP-2 error count						
0A	R	VTLOP	FEBE count						
0B	R	Neg. stuff count		Pos. stuff count		RX YEL	RX LABEL L_1	L_2	L_3
0C	R/W	T1LOOP	--	EXTCK	TX VTAIS	B8ZS	TX LABEL L_3	L_2	L_1
0D	R	--	--	--	--	--	VTNDF	FIFO error	
0E	W	TX YEL	Generate BIP-2 error multiframe timer						
0F	R	--	--	--	--	PAR	STS LOP	--	--
18	R	Coding violation counter (CERR)							

*Read/write (R/W); Read only (R); Write only (W).

SPECIAL REGISTERS

Address (Hex)	Status*	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1E	R/W	0	0	0	0	0	BYPAS	0	0
1F	R/W	--	--	--	--	--	--	--	Reset

*Read/write (R/W); Read only (R); Write only (W).

ADMA-T1 Register Bit Map Definitions

Port 1

Address	Bit	Symbol	Description
00	7	U/$\overline{D}$	**Upstream/Downstream Drop Bus Control:** Selects the bus for dropping a VT1.5 for port 1. The VT1.5 selection is determined by the value written into bits 4-0. A one selects the upstream drop bus, while a zero selects the downstream drop bus. A VT1.5 dropped from the downstream drop bus is added to the upstream add bus, while a VT1.5 dropped from the upstream drop bus is added to the downstream add bus.
	4-0	VT1.5#	**Port 1 VT1.5 Selection:** The VT1.5 selected from a VT group is determined by the value written into bits 4 through 0. The numbering scheme corresponds to the VT group and numbering plan specified in Bellcore and ANSI documents. The binary value of 00000 and binary values greater than 28 (11101, 11110, and 11111) causes an all ones DS1 signal to be transmitted on the outgoing VT. The table below illustrates the VT1.5 selection to the value written. Bits VT1.5 Selected 4 3 2 1 0 No. 1 Group 1 0 0 0 0 1 No. 2 Group 2 0 0 0 1 0 No. 27 Group 6 1 1 0 1 1 No. 28 Group 7 1 1 1 0 0
01	7	VTAIS	**VT Alarm Indication Signal (AIS) Alarm:** A one indicates an alarm. A VTAIS alarm occurs when all ones are detected in the V1 and V2 bytes for three consecutive VT superframes. The alarm causes an unframed all ones DS1 signal. Recovery occurs when a normal New Data Flag (NDF) or valid VT pointer are detected for three consecutive VT superframes. This bit position is latched and is cleared on a processor read cycle.
	6-0	BIP-2 error count	**BIP-2 Error Counter:** This performance counter increments when there is a difference between the calculated BIP-2 value of the present VT SPE and received BIP-2 value in the following VT SPE. A maximum of two errors can occur each frame. This counter saturates at a count of 127, and is cleared on a processor read cycle. The counter is protected against a lost count during the read cycle by holding a count of two until the read cycle is completed.

Address	Bit	Symbol	Description
02	7	VTLOP	**VT Loss of Pointer Alarm:** A one indicates an alarm. A VT loss of pointer alarm occurs when a valid pointer is not found for eight consecutive superframes, or when eight consecutive NDFs are detected. Recovery occurs when a valid pointer is detected for three consecutive superframes. This bit position is latched and is cleared on a processor read cycle.
	6-0	FEBE count	**Far End Block Error (FEBE) Counter:** A FEBE indication is sent by the remote VT path terminating equipment when one or more errors are detected in the received BIP-2. The counter increments when a FEBE indication is detected in bit 3 in the path overhead byte V5. This counter saturates at a count of 127, and is cleared on a processor read cycle. The counter is protected during the read cycle by holding a count of one until the cycle is completed.
03	7-6	Neg. stuff count	**VT Negative Stuff Counter:** A two-bit counter that increments on a negative stuff. A negative stuff is indicated by the inversion of the five D bits in the V1 and V2 bytes. This counter is cleared on a processor read cycle.
	5-4	Pos. stuff count	**VT Positive Stuff Counter:** A two-bit counter that increments on a positive stuff. A positive stuff is indicated by the inversion of the five I bits in the V1 and V2 bytes. This counter is cleared on a processor read cycle.
	3	RX YEL	**VT Path Yellow Alarm:** A one indicates an alarm. A yellow alarm occurs when a one is detected in bit 8 in the V5 VT path overhead byte for 10 consecutive VT superframes. Recovery occurs when a zero is detected in bit 8 of V5 for 10 consecutive VT superframes. This bit position is latched and is cleared on a processor read cycle.
	2-0	RX LABEL	**VT Receive Signal Label:** The bits in these positions correspond to the three signal label bits found in bits 5 through 7 of the VT path overhead byte V5. Bit 2 corresponds to bit 5 of V5. The receive signal label is updated every superframe.
04	7	T1LOOP	**T1 Loopback Control:** A one written into this position causes a T1 loopback for port 1. When activated, the T1 output is looped back internally to the input, but still provided as an output. The input signal from the line is disabled.
	5	1	**Not Defined:** This bit must always be set to one.
	4	TX VTAIS	**Transmit VT Path AIS:** A VT path AIS is generated by writing a one into this position. VT path AIS consists of all ones in the entire VT, including bytes V1 through V4.
	3	B8ZS	**B8ZS CODEC Enable:** A one written into this position enables the B8ZS codec function for port 1. A zero selects AMI as the DS1 line code.
	2-0	TX LABEL	**VT Transmit Signal Label:** The bits in these positions correspond to the three signal label bits found in bits 5 through 7 in the transmit VT path overhead byte V5. Bit 2 corresponds to bit 7 in V5.
05	2	VTNDF	**VT New Data Flag (NDF) Detected:** Indicates when a New Data Flag (1001) occurs. An NDF occurs once to indicate a change in the pointer value.
	1-0	FIFO error	**Transmit and Receive FIFO Error Indications:** Bit 1 corresponds to the transmit FIFO, while bit 0 corresponds to the receive FIFO. A one occurs in either bit position when there is a FIFO underflow or overflow.

Address	Bit	Symbol	Description
06	7	TX YEL	**Transmit VT Path Yellow Alarm:** A VT path yellow alarm is sent when a one is written into this bit position. A VT path yellow alarm is a one in bit 8 of the VT path overhead byte V5.
	6-0	Gen	**Generate BIP-2 Error Counter:** Consecutive errored paired BIP-2 values can be sent by writing the selected binary value into bits 6-0. The least significant bit is bit 0. A maximum of 127 consecutive errored paired BIP-2 values (254 BIP-4 errors) can be sent. The counter decrements by one for each paired error sent. The error is generated by inverting the calculated value. Reading byte 06 also causes the BIP-2 Error Counter to decrement. Caution: If the counter is cleared to zero and then read, the decrement value will be 127. Writing zeros into bits 6-0 disables the generator.
07	3	PAR	**Parity Error:** An upstream drop parity error is a one, and it occurs when the calculated parity (odd parity check over the data byte) does not agree with the incoming parity. Parity has no effect on operation, but is provided for checking the integrity of the bus. This is a latched bit position, and is cleared on a processor read cycle.
	2	STS LOP	**STS Loss of Pointer:** A one indicates an upstream drop STS-1 loss of pointer. This is a latched bit position, and is cleared on a processor read cycle.
10	7-0	CERR	**Coding Violation Counter:** This counter counts the number of coding errors (other than normal coding sequences) that occur in the AMI or B8ZS line codes. The counter saturates at a count of 255 and a processor read cycle clears the counter. The counter is protected during a read cycle by holding a count of two until the cycle is complete. The counter is disabled when the line decoder is bypassed.

Port 2

Address	Bit	Symbol	Description
08	7	$\overline{U}/\overline{D}$	**Upstream/Downstream Drop Bus Control:** Selects the bus for dropping VT1.5 for port 2. The VT1.5 selection is determined by the value written into bits 4-0. A one selects the upstream drop bus, while a zero selects the downstream drop bus. A VT1.5 dropped from the downstream drop bus is added to the upstream add bus, while a VT1.5 dropped from the upstream drop bus is added to the downstream add bus.
	4-0	VT1.5#	**Port 2 VT1.5 Selection:** The VT1.5 selected from a VT group is determined by the value written into bits 4 through 0. The numbering scheme corresponds to the VT group and numbering plan specified in Bellcore and ANSI documents. The binary value of 00000 and binary values greater than 28 (11101, 11110, and 11111) causes an all ones DS1 signal to be transmitted on the outgoing VT. The table below illustrates the VT1.5 selection to the value written. Bits VT1.5 Selected 4 3 2 1 0 No. 1 Group 1 0 0 0 0 1 No. 2 Group 2 0 0 0 1 0 No. 27 Group 6 1 1 0 1 1 No. 28 Group 7 1 1 1 0 0

Address	Bit	Symbol	Description
09	7	VTAIS	**VT Alarm Indication Signal (AIS) Alarm:** A one indicates an alarm. A VTAIS alarm occurs when all ones are detected in the V1 and V2 bytes for three consecutive VT superframes. The alarm causes an unframed all ones DS1 signal. Recovery occurs when a valid VT pointer and a normal New Data Flag (NDF) are detected for three consecutive VT superframes. This bit position is latched and is cleared on a processor read cycle.
	6-0	BIP-2 error count	**BIP-2 Error Counter:** This performance counter increments when there is a difference between the calculated BIP-2 value of the present VT SPE and received BIP-2 value in the following VT SPE. A maximum of two errors can occur each frame. This counter saturates at a count of 127, and is cleared on a processor read cycle. The counter is protected against a lost count during the read cycle by holding a count of two until the read cycle is completed.
0A	7	VTLOP	**VT Loss of Pointer Alarm:** A one indicates an alarm. A VT loss of pointer alarm occurs when a valid pointer is not found for eight consecutive superframes, or eight consecutive NDFs are detected. Recovery occurs when a valid pointer is detected for three consecutive superframes. This bit position is latched and is cleared on a processor read cycle.
	6-0	FEBE Count	**Far End Block Error (FEBE) Counter:** A FEBE indication is sent by the remote VT path terminating equipment when one or more errors are detected in the received BIP-2. The counter increments when a FEBE indication is detected in bit 3 in the path overhead byte V5. This counter saturates at a count of 127, and is cleared on a processor read cycle. The counter is protected during the read cycle by holding a count of one until the cycle is completed.
0B	7-6	Neg. Stuff Count	**VT Negative Stuff Counter:** A two-bit counter that increments on a negative stuff. A negative stuff is indicated by the inversion of the five D bits in the V1 and V2 bytes. This counter is cleared on a processor read cycle.
	5-4	Pos. Stuff Count	**VT Positive Stuff Counter:** A two-bit counter that increments on a positive stuff. A positive stuff is indicated by the inversion of the five I bits in the V1 and V2 bytes. This counter is cleared on a processor read cycle.
	3	RX YEL	**VT Path Yellow Alarm:** A one indicates an alarm. A yellow alarm occurs when a one is detected in bit 8 in the V5 VT path overhead byte for 10 consecutive VT superframes. Recovery occurs when a zero is detected in bit 8 of V5 for 10 consecutive VT superframes. This bit position is latched and is cleared on a processor read cycle.
	2-0	RX LABEL	**VT Receive Signal Label:** The bits in these positions correspond to the three signal label bits found in bits 5 through 7 of the VT path overhead byte V5. Bit 2 corresponds to bit 5 of V5. The receive signal label is updated every superframe.

Address	Bit	Symbol	Description
0C	7	T1LOOP	**T1 Loopback Control:** A one written into this position causes a T1 loopback for port 2. When activated, the T1 output is looped back internally to the input, but is still provided as an output. The input signal from the line is disabled.
	5	EXTCK	**External Clock:** A one selects the external 51.84 MHz clock (from input pin EXTCK) instead of the clock derived from the downstream drop clock by the PLL.
	4	TX VTAIS	**Transmit VT Path AIS:** A VT path AIS is generated by writing a one into this position. VT path AIS consists of all ones in the entire VT, including bytes V1 through V4.
	3	B8ZS	**B8ZS CODEC Enable:** A one written into this position enables the B8ZS codec function for port 2. A zero selects AMI as the DS1 line code.
	2-0	TX LABEL	**VT Transmit Signal Label:** The bits in these positions correspond to the three signal label bits found in bits 5 through 7 in the transmit VT path overhead byte V5. Bit 2 corresponds to bit 7 in V5.
0D	2	VTNDF	**VT New Data Flag (NDF) Detected:** Indicates when a New Data Flag (1001) occurs. An NDF occurs once to indicate a change in the pointer value.
	1-0	FIFO error	**Transmit and Receive FIFO Error Indications:** Bit 1 corresponds to the transmit FIFO, while bit 0 corresponds to the receive FIFO. A one occurs in either bit position when there is a FIFO underflow or overflow.
0E	7	TX YEL	**Transmit VT Path Yellow Alarm:** A VT path yellow alarm is sent when a one is written into this bit position. A VT path yellow alarm is a one in bit 8 of the VT path overhead byte V5.
	6-0	Gen	**Generate BIP-2 Error Counter:** Consecutive errored paired BIP-2 values can be sent by writing the selected binary value into bits 6-0. The least significant bit is bit 0. A maximum of 127 consecutive errored paired BIP-2 values (254 BIP-4 errors) can be sent. The counter decrements by one for each paired error sent. The error is generated by inverting the calculated value. Reading byte 06 also causes the BIP-2 Error Counter to decrement. Caution: If the counter is cleared to zero and then read, the decrement value will be 127. Writing zeros into bits 6-0 disables the generator.
0F	3	PAR	**Parity Error:** A downstream drop parity error is a one, and it occurs when the calculated parity (odd parity check over the data byte) does not agree with the incoming parity. Parity has no effect on operation, but is provided for checking the integrity of the bus. This is a latched bit position and is cleared on a processor read cycle.
	2	STS LOP	**STS Loss of Pointer:** A one indicates a downstream drop STS-1 loss of pointer. This is a latched bit position and is cleared on a processor read cycle.
18	7-0	CERR	**Coding Violation Counter:** This counter counts the number of coding errors (other than normal coding sequences) that occur in the AMI or B8ZS line codes. The counter saturates at a count of 255, and a processor read cycle clears the counter. The counter is protected during a read cycle by holding a count of two until the cycle is complete. The counter is disabled when the line decoder is bypassed.

Bypass Register

This register in the ADMA-T1 (shown below) causes the two codecs in the device to be bypassed. Its address, 1E (HEX), is only accessible when the BYPAS pin (pin 71) is high; it is normally zero because of hardware or software reset. The two codecs are bypassed by writing an 04 (HEX) to register 1E (HEX). If any other value is written to location 1E, the ADMA-T1 may be put into an inoperable state.

Address	7	6	5	4	3	2	1	0
1E	0	0	0	0	0	BYPAS	0	0

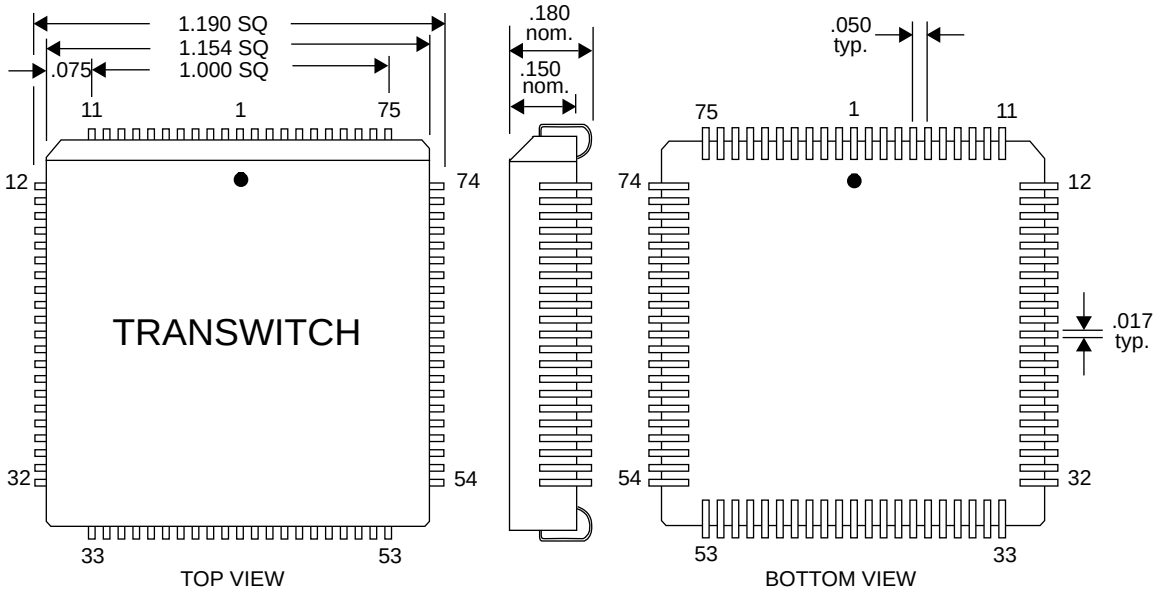
Note: Only bit 2 may be set to one; all other bits must be zero.

Reset Register

Address	Bit	Symbol	Description
1F	0	RESET	ADMA-T1 software reset bit. All status registers are reset to their internal default value and all counters are reset to zero. In order to use the RESET feature, the RESET bit must be set to one and then cleared to zero.

PACKAGING

The ADMA-T1 is packaged in an 84-pin plastic chip carrier suitable for socket or surface mounting. All dimensions shown are in inches and are nominal unless otherwise noted. All dimensions and notes for the specified JEDEC outline apply.



(JEDEC Outline MO-047)

Figure 10. ADMA-T1 84-Pin Plastic Leaded Chip Carrier

ORDERING INFORMATION

Part Number:	TXC-04001-AIPL	84-pin plastic leaded chip carrier

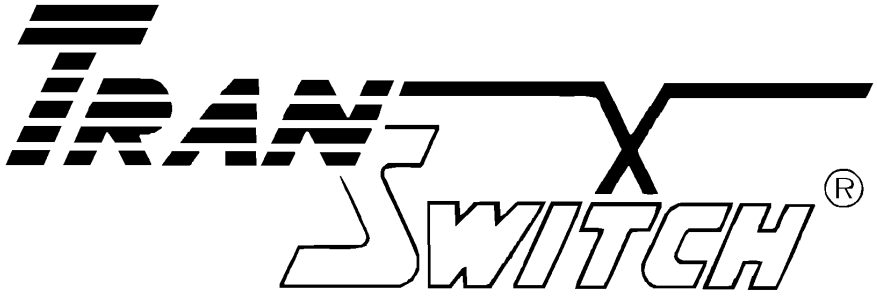
RELATED PRODUCTS

TXC-03001, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). In a single chip, it provides the SONET interface to any payload. Provides access to all of the transport and path overhead defined for an STS-1/STS-N SONET signal.

TXC-21009, ADMA-T1/SOT-1 Evaluation Board. A complete, ready-to-use single board test system that demonstrates the functions and features of the ADMA-T1 and SOT-1 VLSI devices. Includes on-board microprocessor, RS-232 interface, and MS-DOS compatible PC software. The PC software provides full access to the ADMA-T1 and SOT-1 devices for control and monitor.

- NOTES -

- NOTES -



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TranSwitch Corporation • 8 Progress Drive • Shelton, CT 06484 • USA • Tel: 203-929-8810 • Fax: 203-926-9453