ART Devices

Advanced DS3/STS-1 Receiver/Transmitter

ART: TXC-02020 (44-Pin)

ARTE: TXC-02021 (68-Pin)

DATA SHEET

FEATURES

- Single device line interface for DS3 and STS-1
- Meets ANSI Standard T1.102-1993
- Meets 'crossconnect frame' mask requirements
- Adaptive equalization for 0 - 900 ft. of cable
- Input dynamic range of 28.5 dB (35 mV - 0.95V)
- Meets approved DS3/STS-1 jitter requirements
- Selectable B3ZS line encoding/decoding
- Line and terminal side DS3 AIS insertion
- Full loopback capability
- Coding Violation and Excessive Zeros monitors
- Loss of signal detection (per T1/M1 Spec)
- On-device Tx line buffer/filter and optional Tx line build-out bypass
- Power-down mode
- Plastic leaded chip carrier packages:
  - 44-pin (ART)
  - 68-pin (ARTE) with Extended features
- Single +5V power supply

DESCRIPTION

The Advanced DS3/STS-1 Receiver/Transmitter (ART) device performs the receive and transmit line interface functions required for transmission of DS3 (44.736 Mbit/s) or STS-1 (51.840 Mbit/s) signals across a coaxial interface.

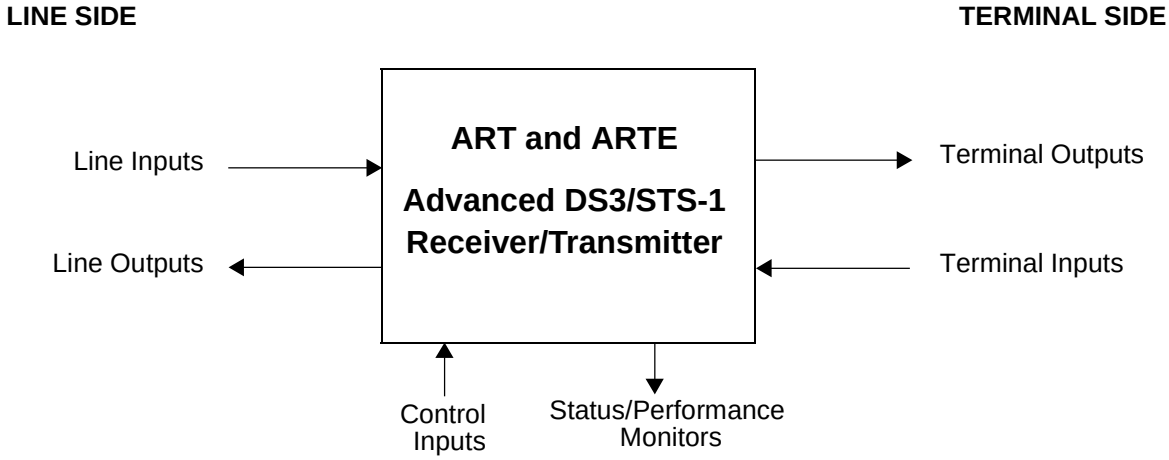
The ART operates from a single +5V supply with a minimum number of (passive) external components. Performance monitoring, loopbacks, DS3 AIS generation and B3ZS encoding/decoding functions are included.

A single-device solution for interfacing DS3 or STS-1 signals to DSX or STS-X crossconnect frames, the ART meets all applicable ANSI, BellCore, and ITU interconnection specifications for a wide range of system applications.

The ARTE has the same performance as the ART but nine additional input and output pins provide additional Extended features.

APPLICATIONS

- Multiplexers
- DSX/STSX and performance monitoring cross connects
- Fiber optic and microwave radio terminals
- High speed DSU
- Any DS3/STS-1 transmission application



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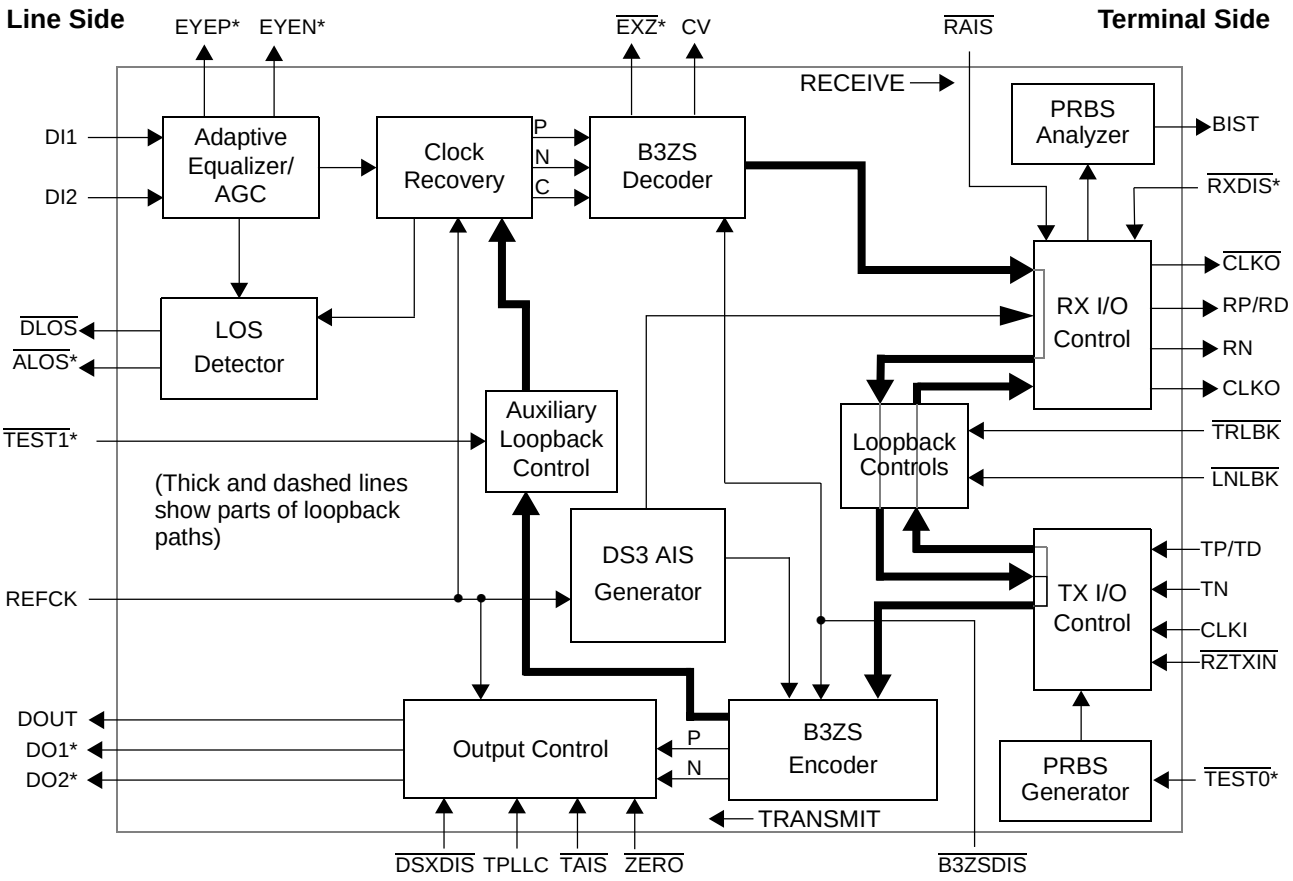
LIST OF FIGURES

BLOCK DIAGRAM



*Note: The nine signal terminations denoted with an asterisk (*) are provided in the 68-pin Extended features ARTE version of the ART (TXC-02021). These terminations are not provided in the 44-pin ART device (TXC-02020).

Figure 1. ART and ARTE Block Diagram

BLOCK DIAGRAM DESCRIPTION

Receiver Functions

The Adaptive Equalizer/AGC block in the ART receiver is used to recover CMOS level P/N rail data from the bipolar B3ZS encoded input pulses. The AGC in the ART has a dynamic range of 28.5 dB (35 mV to 0.95 volts) which allows the device to be used in applications where the input signal is attenuated beyond the level of the pulse template (such as bridging repeaters or protection switches). Adaptive equalization is included to restore the integrity of the signal after it has been attenuated by the frequency-dependent loss of up to 900 feet of coaxial cable. The equalized and automatic gain controlled differential signals are provided as outputs on the EYEP and EYEN pins.

Differential inputs DI1 and DI2 are provided to allow optimum performance of the device in noisy environments. Alternatively, single ended operation can be used in less critical environments or where the use of a transformer is not desired (the input signal can be AC coupled via a capacitor). When the differential mode is used, the AC voltage measured between DI1 and DI2 is a maximum magnitude of 0.95 volts. For single-ended operation, the voltage measured at DI1 (DI2) relative to the DC bias voltage at DI2 (DI1) is a maximum of ±0.95 volts. Since the ART/ARTE has a sensitive receiver, the 4 dB attenuator of Figure 13c should be used for all new designs. The attenuator has eliminated bit errors in some designs where noise was present. For

input levels larger than $0.95V_{peak}$, a step-down transformer or resistive attenuator should be used (see Figure 13c for suggested attenuator topology - the circuit may be modified to provide the desired attenuation).

The PLL-based Clock Recovery block is used to recover a CMOS level clock from the equalized and sliced input pulses. The filters are internal. When data is present, $\overline{\text{DLOS}}$ is high, and $\overline{\text{TEST1}}$ is high, then CLKO is the clock recovered from the data. For $\overline{\text{DLOS}}$ low and $\overline{\text{TEST1}}$ high then CLKO is equal to DCK +/- 10%. When $\overline{\text{TEST1}}$ is low or $\overline{\text{TRLBK}}$ is low then the CLKO is equal to the transmit input clock, CLKI.

The B3ZS Decoder block decodes the B3ZS encoded line signal and detects coding errors and excessive zeros in the incoming data stream. An active-high pulse is generated on the CV output whenever the input signal violates the B3ZS encoding sequence for bipolar violations or contains three or more zeros. An active-low pulse is generated on the $\overline{\text{EXZ}}$ output when a string of three or more zeros is detected, and it remains low until a one is detected. The $\overline{\text{B3ZSDIS}}$ control input is used to bypass the decoder, but the decoder is always operating.

The RX I/O Control block multiplexes the appropriate signals to the Receiver Terminal Side outputs. The output NRZ data formats include:

1. B3ZS decoded output recovered from the line (RP/RD contains recovered data; RN is held low). This mode is referred to as NRZ mode.
2. Encoded outputs from the Clock Recovery block (RP/RD contains positive data; RN contains negative data). This mode allows an external device such as a DS3 Framer (TXC-03401B) to perform the B3ZS encoding/decoding functions. $\overline{\text{B3ZSDIS}}$ enables this mode; this is referred to as PN rail mode.
3. Loopback signals from the Transmitter terminal side inputs. These signals are looped through the digital logic when $\overline{\text{TRLBK}}$ is low. The receiver and clock recovery are bypassed.
4. AIS DS3 framed format signals when $\overline{\text{RAIS}}$ is low.
5. Loopback signals from the Transmitter terminal side inputs. These signals are looped through the clock recovery when $\overline{\text{TEST1}}$ is low.

Outputs CLKO and $\overline{\text{CLKO}}$ provide true and inverted clocks for all formats.

The $\overline{\text{RXDIS}}$ signal forces the RP/RD and RN outputs to a low state.

The LOS Detector block generates active low outputs which indicate the absence of the line side input signal(s). The $\overline{\text{DLOS}}$ output goes low when a string of 175 ± 75 consecutive zeros occurs on the line. This output is reset when the detected 1's density is in the range of 28 to 33% (or $\geq$ 33%) for 175 ± 75 pulses. The $\overline{\text{ALOS}}$ output goes high when the 1's density is greater than 33% and goes low when the 1's density is below 28%. Between 28 and 33% $\overline{\text{ALOS}}$ output may toggle between the active and inactive states.

The LOS detector block always uses the receiver outputs which are based upon the receiver inputs DI1 and DI2 for LOS. When $\overline{\text{TRBLK}}$ is low the clock recovery block is still recovering the clock from the receiver inputs. Therefore the $\overline{\text{DLOS}}$ and $\overline{\text{ALOS}}$ signals are still valid. When $\overline{\text{TEST1}}$ is low the clock recovery block will recover the clock from the internally looped transmitter inputs. In this state $\overline{\text{DLOS}}$ and $\overline{\text{ALOS}}$ will be active but may no longer meet the limits given above.

Transmitter Functions

The TX I/O Control block multiplexes the appropriate signals for use by the transmitter. The selectable formats include:

1. Unencoded NRZ input data (TP/TD contains data, TN must be grounded). This is referred to as NRZ mode.
2. B3ZS encoded NRZ input data (TP/TD contains positive data, TN contains negative data). $\overline{\text{B3ZSDIS}}$ enables this mode (PN rail mode)
3. B3ZS encoded RZ input data (TP/TD contains positive data, TN contains negative data). This mode is enabled by $\overline{\text{RZTXIN}}$.
4. Loopback signals from the B3ZS Decoder when $\overline{\text{LNLBK}}$ is low.
5. AIS DS3 framed format signals when $\overline{\text{TAIS}}$ is low.
6. 2^{15}-1 PRBS Generator output when $\overline{\text{TEST0}}$ is low.

The CLKI pin is the input clock for the above formats. When $\overline{\text{RZTXIN}}$ is low, the CLKI signal is ignored and should be tied low.

The B3ZS Encoder block encodes the input NRZ mode data so as to be compliant with ANSI Specification T1.102A. Figure 10a gives examples of B3ZS coding. The $\overline{\text{B3ZSDIS}}$ control pin can be used to bypass this block. $\overline{\text{B3ZSDIS}}$ must be low when $\overline{\text{RZTXIN}}$ is low.

The Output Control block contains the pulse shaping circuitry required to transform the B3ZS-encoded data into pulses that meet the mask templates and power requirements for DS3 and STS-1 line rates. An internal line driver is included which enables the ART to drive this signal directly from DOUT into the 75 ohm load of the output cable.

The $\overline{\text{DSXDIS}}$ input determines which of two output types is enabled. DOUT is a single-ended output which meets the DS3/STS-1 mask templates. An internal transversal filter is used to create this output. Outputs DO1 and DO2 are rectangular pulses representing level-translated versions of the input digital signal(s). An external transformer is required to translate these pulses to the appropriate +/- polarity waveform. When $\overline{\text{DSXDIS}}$ is high the DOUT output is enabled. When $\overline{\text{DSXDIS}}$ is low the DO1/DO2 outputs are enabled. Figure 10b shows idealized transmitter waveforms for both output modes.

An external capacitor connected from TPLLC to the proper Analog Ground is required for the internal PLL used to calibrate the transversal filter circuit (see Figure 13a and Note 9). Input $\overline{\text{ZERO}}$ improves the DOUT pulse shape for short cable (0 to 100 feet) by lowering the amplitude and widening the pulse; the $\overline{\text{ZERO}}$ pin is active low.

Loopbacks and AIS Insertion

The Loopback Controls block enables the input signals of the ART to be looped back on both the line and terminal sides of the device. When $\overline{\text{TRLBK}}$ (Terminal Loopback) is low the TP/TD, TN, and CLKI inputs are directly looped back to the RP/RD, RN, and CLKO pins via the RX I/O Control Block (all digital signal path). When $\overline{\text{LNLBK}}$ is low the DI1/DI2 signals are looped back to the DOUT or DO1/DO2 outputs via the Adaptive Equalizer/AGC, Clock Recovery, B3ZS Decoder, RX I/O Control, Loopback Controls, TX I/O Control, B3ZS Encoder, and Output Control blocks; the looped data comes from the B3ZS decoder regardless of the state of $\overline{\text{B3ZSIDS}}$. These loopbacks may be operated independently or simultaneously. It should be noted that, when $\overline{\text{TRLBK}}$ is active, the CV, $\overline{\text{DLOS}}$, $\overline{\text{EXZ}}$ and $\overline{\text{ALOS}}$ output signals will still respond to the line input data signals applied at pins DI1 and DI2 and will be valid.

The DS3 AIS Generator block generates a DS3 alarm indication signal (AIS) compliant with Bellcore Specification TR191 on the line or terminal sides of the device (selected with $\overline{\text{TAIS}}$ or $\overline{\text{RAIS}}$). For STS-1 operation the inputs to the device must contain the correct overhead required for path sectionalization, i.e., this block generates *DS3 format AIS only.* AIS will override the loopback commands.

For the ARTE device, $\overline{\text{TEST1}}$ will loop back the terminal input data through the B3ZS Encoder, Auxiliary Loopback Control, Clock Recovery and B3ZS Decoder blocks, as described below. When $\overline{\text{TXAIS}}$ is active at the same time as $\overline{\text{TEST1}}$, AIS will loop through this path.

Testability

The 2^{15}-1 PRBS Generator and PRBS Analyzer blocks (PRBS means Pseudo-Random Binary Sequence) are used to provide diagnostic functions such as internal Built-In Self Test (BIST). When the $\overline{\text{TEST0}}$ pin is low the output of the PRBS generator is driven through the TX I/O Control, B3ZS Encoder, and Output Control block to either DOUT when $\overline{\text{DSXDIS}}$ is high or DO1/DO2 when $\overline{\text{DSXDIS}}$ is low. The encoder is always enabled when $\overline{\text{TEST0}}$ is low regardless of the $\overline{\text{B3ZSDIS}}$ pin state; the generator will work in NRZ mode or PN data mode.

The PRBS Analyzer monitors the output of the RX I/O Control block. If the output signals conform to the correct 2^{15}-1 pattern and the decoder is enabled ($\overline{\text{B3ZSDIS}}$ is high) the BIST output will go high. Note that the PRBS Analyzer always functions, regardless of the state of the $\overline{\text{TEST0}}$ pin; whenever a valid 2^{15}-1 pattern (this pattern can contain a significant number of errors and still be valid) appears at the receiver outputs the BIST pin will go high.

The analyzer must be run with the $\overline{\text{B3ZSDIS}}$ pin held high since the PRBS analyzer works with NRZ data only. The Generator/Analyzer combination can be used in conjunction with an external line-side loopback for diagnostic purposes. Since the combination of $\overline{\text{TEST0}}$ and $\overline{\text{TEST1}}$ low sends signals through all of the data path blocks in the device it is particularly useful for manufacturing test.

The $\overline{\text{TEST1}}$ pin enables an auxiliary terminal-side loopback primarily intended for use during device testing. Signals from the Transmitter terminal-side inputs are routed through the TX I/O Control, B3ZS Encoder, Auxiliary Loopback Control, Clock Recovery, B3ZS Decoder, and RX I/O Control blocks to the Receiver terminal-side outputs.

Input Reference Clock

An input CMOS level clock at the DS3 or STS-1 rate must be applied to the REFCK input for the ART to operate. This will typically be supplied by a local oscillator on the board. The tolerance required is $\pm$ 200 ppm for operation when the DS3 AIS generator is not used. To generate a valid AIS pattern a tolerance of $\pm$ 20 ppm is required.

Functional Differences Between the 68-Pin (ARTE) and 44-Pin (ART) Versions of ART

The 68-pin version (ARTE) has all of the features and terminations of the 44-pin version (ART), plus the following nine additional terminations (Extended features):

DO1	Transmit output rectangular positive pulse
DO2	Transmit output rectangular negative pulse
$\overline{\text{RXDIS}}$	Receive output disable
$\overline{\text{ALOS}}$	Analog loss of signal indicator
EYEP	Positive eye pattern monitor
EYEN	Negative eye pattern monitor
$\overline{\text{TEST0}}$	Enables internal PRBS generator. Selects PRBS output for transmitting
$\overline{\text{TEST1}}$	Enables a terminal side loopback from the TP/TD and TN signals to the receiver clock recovery, then to the receiver outputs
$\overline{\text{EXZ}}$	Excessive zeros in the received pattern

PIN DIAGRAMS

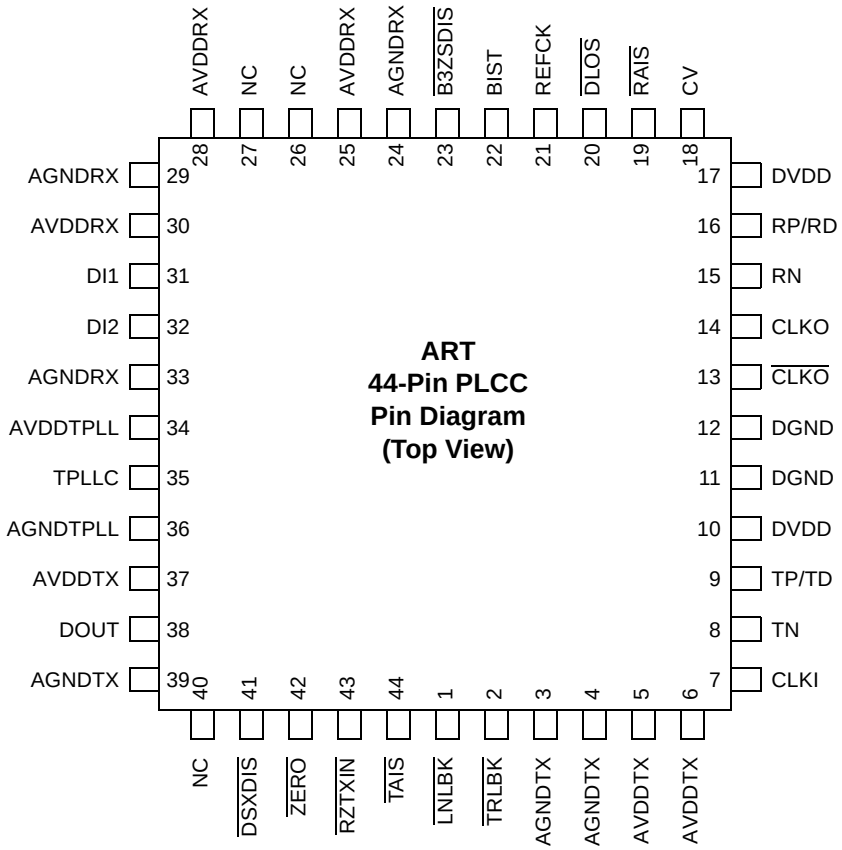
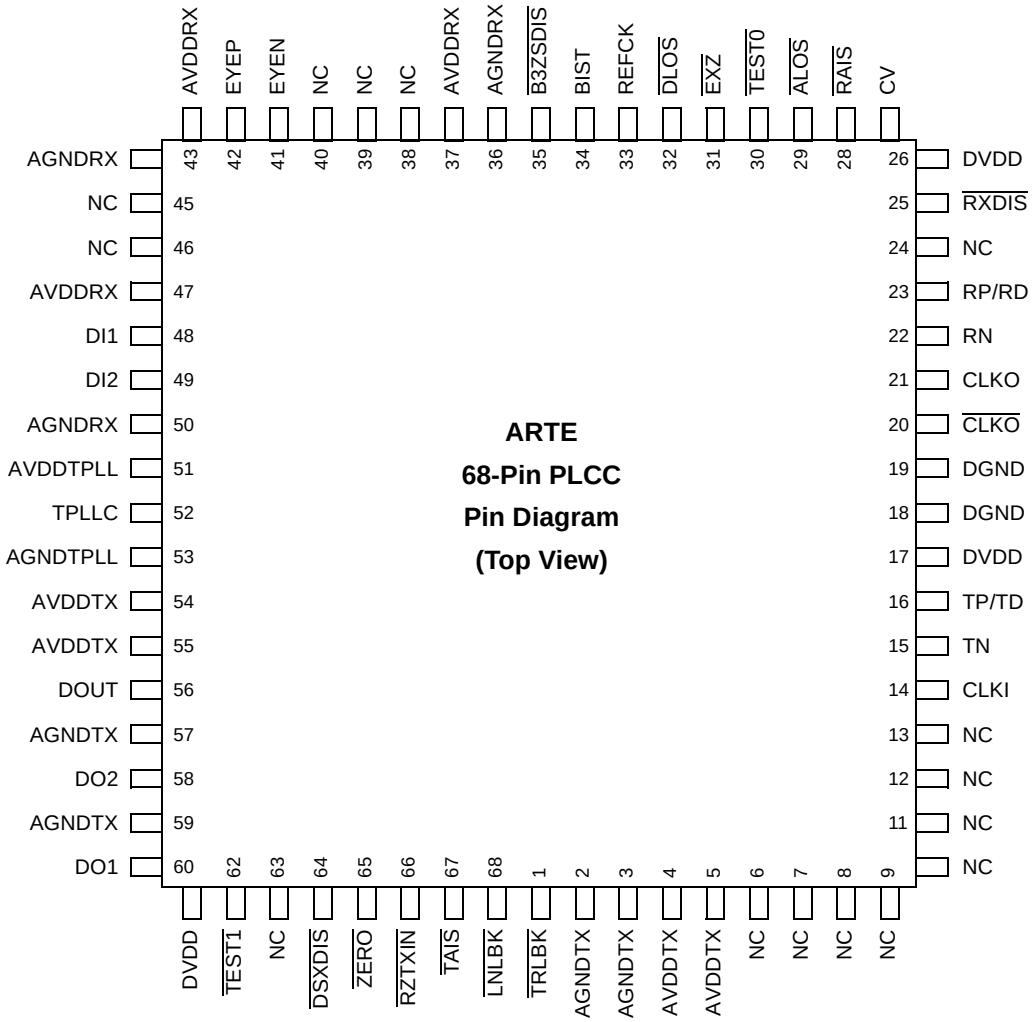


Figure 2. ART Pin Diagram - 44 PLCC Package

Figure 3. ARTE Pin Diagram - 68 PLCC Package



PIN DESCRIPTIONS

Power Supply and Ground

Symbol	Pin No.		I/O/P*	Type	Name/Function
	ART (44-Pin)	ARTE (68-Pin)			
AVDDTX	5 6 37	4 5 54 55	P		**Analog VDD Transmit:** + 5 Volt Supply ± 5%
AVDDRX	25 28 30	37 43 47	P		**Analog VDD Receive:** + 5 Volt Supply ± 5%
AVDDTPLL	34	51	P		**Analog VDD Transmit PLL:** + 5 Volt Supply ± 5%
DVDD	10 17	17 26 61	P		**Digital VDD**: + 5 Volt Supply ± 5%
AGNDTX	3 4 39	2 3 57 59	P		**Analog Ground Transmit:** 0 Volts Reference
AGNDRX	24 29 33	36 44 50	P		**Analog Ground Receive:** 0 Volts Reference
AGNDTPLL	36	53	P		**Analog Ground Transmit PLL:** 0 Volts Reference
DGND	11 12	18 19	P		**Digital Ground:** 0 Volts Reference

*Note: I = Input; O = Output; P = Power

Receive Interface

Symbol	Pin No.		I/O/P	Type *	Name/Function
	ART (44-Pin)	ARTE (68-Pin)			
DI1	31	48	I	Analog	**Data in 1, Data In 2:** Line Side Inputs. For single-ended operation DI1 or DI2 must be AC coupled to ground via a capacitor. For differential operation both inputs can be tied directly to a transformer.
DI2	32	49	I	Analog	
EYEP	N/A	42	O	Analog	**Positive Eye Pattern Monitor:** Monitors non-inverted, automatic gain controlled and equalized output from Adaptive Equalizer/AGC block.

*See Input and Output Parameters section below for digital Type definitions.

Symbol	Pin No.		I/O/P	Type *	Name/Function
	ART (44-Pin)	ARTE (68-Pin)			
EYEN	N/A	41	O	Analog	**Negative Eye Pattern Monitor:** Monitors inverted, automatic gain controlled and equalized output from Adaptive Equalizer/AGC block.
$\overline{EXZ}$	N/A	31	O	CMOS	**Excessive Zeros:** Low when three or more consecutive zeros occur in the input data stream. Valid regardless of the state of $\overline{B3ZSDIS}$**. ***
CV	18	27	O	CMOS	**Coding Violation:** High when incoming data violates B3ZS coding for bipolar violations or when three or more consecutive zeros occur in the input data stream. Valid regardless of the state of $\overline{B3ZSDIS}$. *
$\overline{DLOS}$	20	32	O	CMOS	**Digital LOS:** Low when 175 $\pm$ 75 consecutive zeros appear in the incoming data stream. Cleared when ones pulse density is in the range of 28 to 33% (or $\geq$ 33%) for 175 $\pm$ 75 pulses. Valid regardless of the state of $\overline{TRLBK}$ *
$\overline{ALOS}$	N/A	29	O	CMOS	**Analog LOS:** Low when pulse density < 28% for 175 $\pm$ 75 pulses. Cleared when pulse density is > 33% for 175 $\pm$ 75 pulses. $\overline{ALOS}$ may toggle between active and inactive when between 28 and 33%. Valid regardless of the state of $\overline{TRLBK}$. *
RP/RD	16	23	O	CMOS	**Receiver Positive/Data:** Generates B3ZS decoded NRZ, combined data ($\overline{B3ZSDIS}$ high) or the positive rail portion of PN data ($\overline{B3ZSDIS}$ low). Held low when $\overline{RXDIS}$ is low.
RN	15	22	O	CMOS	**Receiver Negative:** Generates negative rail portion of PN data when $\overline{B3ZSDIS}$ is low. Held low when $\overline{B3ZSDIS}$ is high and/or when $\overline{RXDIS}$ is low.
CLKO	14	21	O	CMOS	**Receiver Clock Out:** Receiver output clock.
$\overline{CLKO}$	13	20	O	CMOS	**Receiver Clock Out Inverted:** Receiver inverted output clock.
BIST	22	34	O	CMOS	**Built-In Self Test Output:** High when a valid unframed 2^{15}-1 PRBS pattern is detected at the receiver outputs. Valid for $\overline{B3ZSDIS}$ high only.

*Note: For $\overline{TRLBK}$ low (active), this output signal responds to the receiver input at the DI1 and DI2 pins.

Transmit Interface

Symbol	Pin No.		I/O/P	Type	Name/Function
	ART (44-Pin)	ARTE (68-Pin)			
TP/TD	9	16	I	CMOS	**Transmitter Positive/Data:** Input for unencoded NRZ mode, combined data ($\overline{\text{B3ZSDIS}}$ high) or positive portion of PN rail data ($\overline{\text{B3ZSDIS}}$ low).
TN	8	15	I	CMOS	**Transmitter Negative:** Input for negative portion of PN rail data when $\overline{\text{B3ZSDIS}}$ is low. Must be tied low when $\overline{\text{B3ZSDIS}}$ is high.
CLKI	7	14	I	CMOS	**Transmitter Input Clock:** Transmitter clock input. Required frequency tolerance is +/- 20 ppm of the nominal bit rate. Required duty cycle is (50+/-10) %
TPLLC	35	52	I	Analog	**Transmit PLL Capacitor:** Capacitor pin for transversal filter calibration PLL (see Figure 13a and its following notes for proper connection).
DO1	N/A	60	O	Analog	**Data Out Positive:** Rectangular positive pulse output - enabled when $\overline{\text{DSXDIS}}$ is low**.** High impedance when $\overline{\text{DSXDIS}}$ is high.
DO2	N/A	58	O	Analog	**Data Out Negative:** Rectangular negative pulse output - enabled when $\overline{\text{DSXDIS}}$ is low. High impedance when $\overline{\text{DSXDIS}}$ is high.
DOUT	38	56	O	Analog	**Data Out:** DSX filtered single-ended output - enabled when $\overline{\text{DSXDIS}}$ is high. Low with low impedance when $\overline{\text{DSXDIS}}$ is low.

Control/Reference Pins (All control pins perform their enable or disable functions when set low, i.e., to 0V)

Symbol	Pin No.		I/O/P	Type	Name/Function
	ART (44-Pin)	ARTE (68-Pin)			
$\overline{\text{RAIS}}$	19	28	I	TTLp	**Receive AIS Enable:** Enables generation of DS3 framed format AIS on the receiver outputs. (See Note 1.)
$\overline{\text{RXDIS}}$	N/A	25	I	TTLp	**Receive Output Disable:** Forces RP/RD and RN to a low state.
$\overline{\text{TRLBK}}$	2	1	I	TTLp	**Terminal Loopback Enable:** Enables a loopback from the transmitter inputs to the receiver outputs via the TX I/O Control block, the Loopback Controls block and the RX I/O Control block.
$\overline{\text{LNLBK}}$	1	68	I	TTLp	**Line Loopback Enable:** Enables a loopback from the DI1/DI2 inputs to the DOUT or DO1/DO2 outputs via the Adaptive Eq/AGC, Clock Recovery, B3ZS Decoder, RX I/O Control, Loopback Controls, TX I/O Control, B3ZS Encoder and Output Control blocks**.**

Symbol	Pin No.		I/O/P	Type	Name/Function
	ART (44-Pin)	ARTE (68-Pin)			
$\overline{\text{RZTXIN}}$	43	66	I	TTLp	**Transmit RZ Input Enable:** When low accepts B3ZS encoded return-to-zero pulses (properly timed) on the transmitter TP/TD and TN inputs. The CLKI and $\overline{\text{B3ZSDIS}}$ inputs must be tied low in this mode.
$\overline{\text{B3ZSDIS}}$	23	35	I	TTLp	**B3ZS Codec Disable:** Bypasses the internal B3ZS Encoder and Decoder functions.
$\overline{\text{ZERO}}$	42	65	I	TTLp	**Transmit Zero Cable Enable:** Improves DOUT output mask for short cable lengths (< 100 feet). Pin is active low.
$\overline{\text{TAIS}}$	44	67	I	TTLp	**Transmit AIS Enable:** Enables generation of DS3 AIS on the transmitter outputs. (See Note 1.)
$\overline{\text{DSXDIS}}$	41	64	I	TTLp	**Transmit DSX Output Disable:** Disables DOUT output and enables DO1/DO2 outputs.
$\overline{\text{TEST0}}$	N/A	30	I	TTLp	**Test In 0:** Enables internal unframed 2^{15}-1 PRBS generator. Valid for NRZ or PN rail mode. This function is described in the Block Diagram Description, Testability section.
$\overline{\text{TEST1}}$	N/A	62	I	TTLp	**Test In 1:** Enables a terminal side loopback from the TP/TD and TN signals to the receiver outputs via the TX I/O Control, B3ZS encoder, Clock Recovery, B3ZS Decoder, and RX I/O Control blocks.
REFCK	21	33	I	CMOS	**Reference Clock Input:** Input reference clock at the system frequency required for device operation, namely 44.736 MHz for DS3 applications or 51.840 MHz for STS-1 applications. Required tolerance is ± 20 ppm when DS3 AIS generation is required and ± 200 ppm otherwise. This clock can be the same as CLKI if not using loop timing. The duty cycle must be (50 ± 10) %.

Note 1: DS3 AIS is defined as a valid M-frame with proper subframe structure. The data payload is a 1010 ... sequence starting with a 1 after each overhead bit. Overhead bits are as follows: F0=0, F1=1, M0=0, M1=1; C-bits are set to 0; X-bits are set to 1; and P-bits are set for valid parity.

No Connects

Symbol	Pin No.		I/O/P	Type	Name/Function
	ART (44-Pin)	ARTE (68-Pin)			
NC	26 27 40	6 - 13 24 38-40 45 46 63			No Connect. NC pins are not to be connected, not even to another NC pin, but must be left floating. The device may be damaged if NC pins are connected.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+7.0	V	Note 1
DC input voltage	V_{IN}	-0.3	V_{DD} + 0.3	V	Note 1
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient operating temperature range	T_A	-40	85	^oC	0 ft/min linear airflow
Component Temperature x Time	TI		270 x 5	^oC x s	Note 1
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD		±2000	V	per MIL-STD-883D Method 3015.7

Notes:
1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance, junction to ambient, ART 44-pin PLCC	--	50	--	$^oC/W$	0 ft/min linear airflow
Thermal resistance, junction to ambient, ARTE 68-pin PLCC	--	40	--	$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}		180	190	mA	Outputs terminated
P_{DD}		950	1000	mW	Inputs switching, V_{DD}=5.25

INPUT AND OUTPUT PARAMETERS

INPUT PARAMETERS FOR TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		V_{DD} + 0.3	V	
V_{IL}	- 0.3		0.8	V	
I_{IH}			- 10	µA	V_{DD} = 5.25V
I_{IL}			550	µA	V_{DD} = 5.25V
Input Capacitance			10	pF	

Note: All TTL input pads have an internal pull-up resistor.

INPUT PARAMETERS FOR CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	V_{DD} - (V_{DD} / 3)		V_{DD} + 0.3	V	
V_{IL}	- 0.3		(V_{DD} / 3)	V	
I_{IH}			- 10	µA	V_{DD} = 5.25V
I_{IL}			10	µA	V_{DD} = 5.25V
Input Capacitance			10	pF	

OUTPUT PARAMETERS FOR CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	4 mA source
V_{OL}			0.5	V	4 mA sink
I_{OH}			- 4.0	mA	V_{DD} = 4.75V
I_{OL}			4.0	mA	V_{DD} = 4.75V
t_{RISE}	1.7	2.7	4.2	ns	C_{LOAD} = 15 pF
t_{FALL}	1.9	2.8	4.1	ns	C_{LOAD} = 15 pF

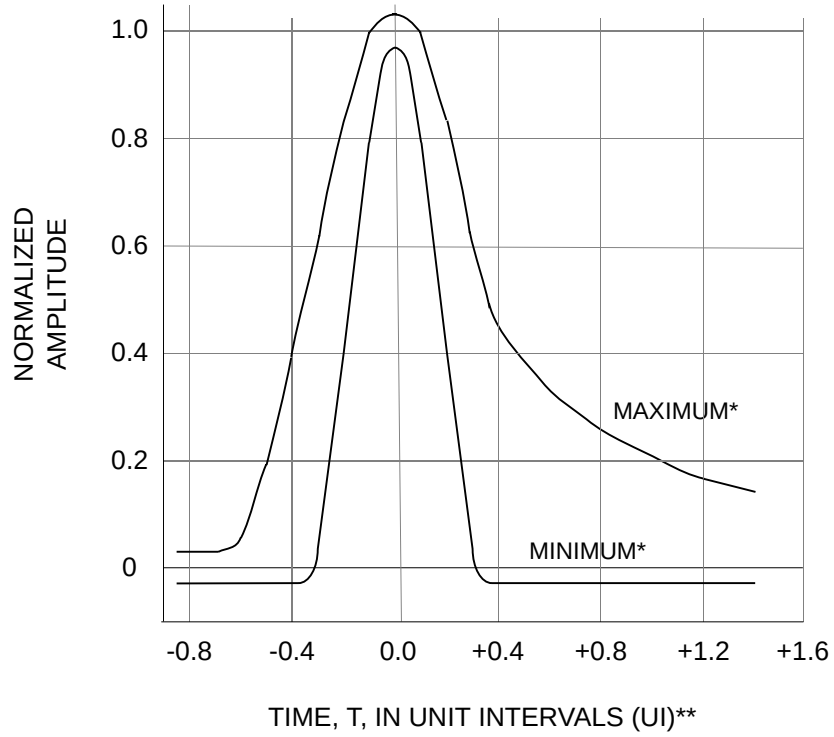
Note: For driving traces greater than 1 inch or driving multiple loads, the ART outputs should be buffered.

TIMING CHARACTERISTICS

Line Side Timing Characteristics

The line side signal characteristics are designed so that the output meets the requirements of ANSI standard T1.102-1993. When terminated into a test load of 75Ω ± 5% using ATT 734A coaxial cable the ART device will meet the DS3 or STS-1 interface isolated pulse masks defined below in Figures 4a through 4c for a cable distance of 0 to 450 feet. The pulse measurement is made using a Hewlett Packard HP54502A oscilloscope (or equivalent) in the average mode, which is described in the HP instruction manual for this instrument. The input to the ART/ARTE device is a 2^{15} - 1 pseudo-random binary sequence (PRBS) signal.

For pulse sequences the output also meets the STS-1 interface eye diagram mask shown in Figure 4d.



* Note: The DS3 curves shown are approximate representations of the equations in Figure 4b. The corresponding STS-1 curves (not shown) would be slightly different, as indicated by the equations in Figure 4c.

**Note: UI = 1 / (System Clock Frequency)

Figure 4a. DS3 Interface Isolated Pulse Mask

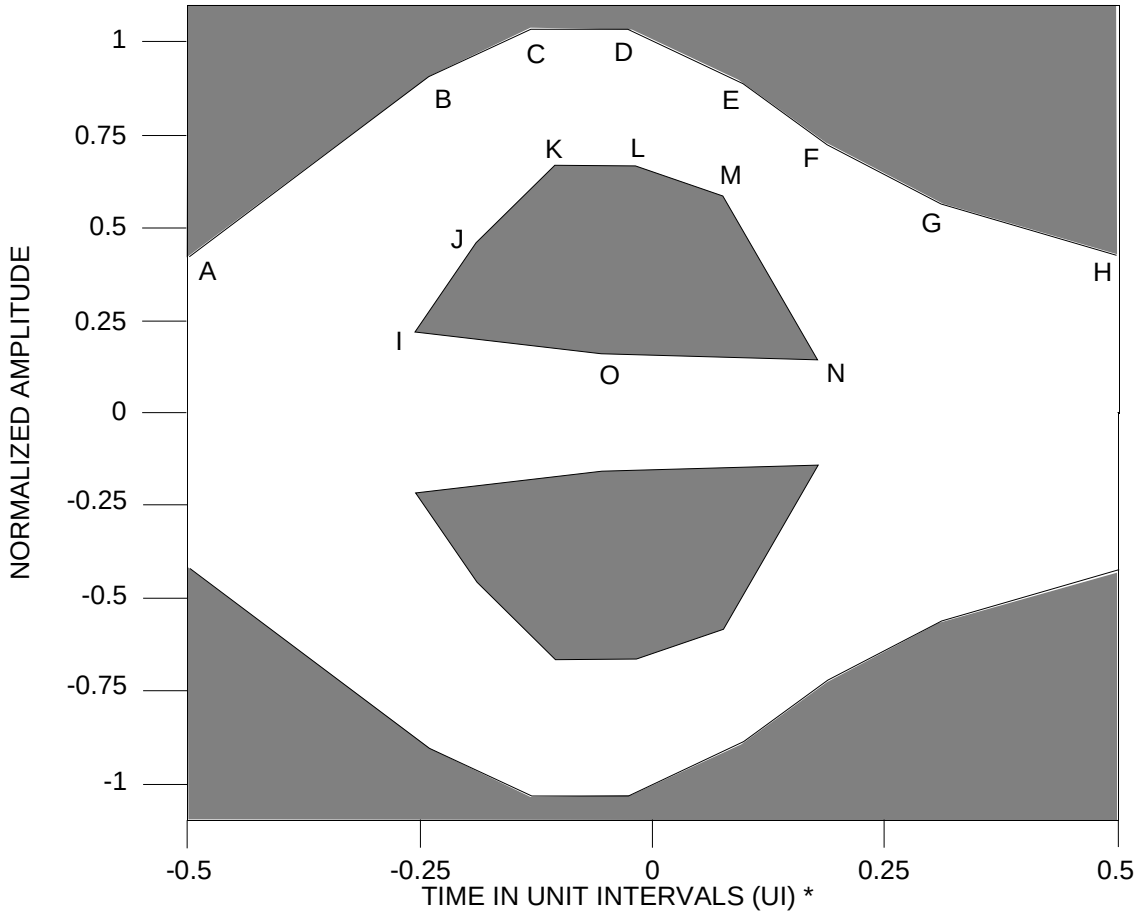
CURVE	TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
MAXIMUM (UPPER) CURVE	$-0.85 \le T \le -0.68$ $-0.68 \le T \le 0.36$ $0.36 \le T \le 1.4$	0.03 $0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.34}\right)\right]+0.03$ $0.08 + 0.407e^{-1.84(T-0.36)}$
MINIMUM (LOWER) CURVE	$-0.85 \le T \le -0.36$ $-0.36 \le T \le 0.36$ $0.36 \le T \le 1.4$	-0.03 $0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.18}\right)\right]-0.03$ -0.03

Figure 4b. DS3 Interface Isolated Pulse Mask Equations

CURVE	TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
MAXIMUM (UPPER) CURVE	$-0.85 \le T \le -0.68$ $-0.68 \le T \le 0.26$ $0.26 \le T \le 1.4$	0.03 $0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.34}\right)\right]+0.03$ $0.1 + 0.61e^{-2.4(T-0.26)}$
MINIMUM (LOWER) CURVE	$-0.85 \le T \le -0.38$ $-0.38 \le T \le 0.36$ $0.36 \le T \le 1.4$	-0.03 $0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.18}\right)\right]-0.03$ -0.03

Figure 4c. STS-1 Interface Isolated Pulse Mask Equations

Figure 4d. STS-1 Interface Eye Diagram Mask



*Note: UI = 1 / (System Clock Frequency)

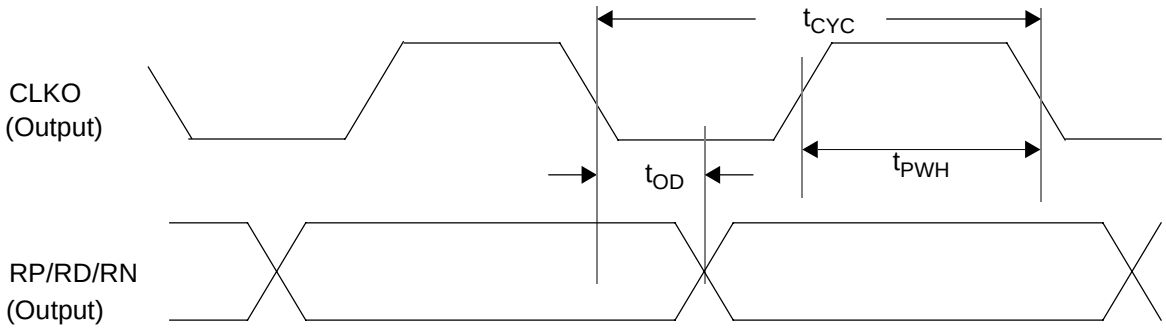
Outer region corner points			Inner region corner points		
Point	**Time**	**Amplitude**	**Point**	**Time**	**Amplitude**
A	-0.5	0.426	I	-0.245	0.214
B	-0.261	0.904	J	-0.187	0.455
C	-0.136	1.03	K	-0.104	0.67
D	-0.028	1.03	L	-0.017	0.67
E	0.094	0.883	M	0.077	0.581
F	0.187	0.723	N	0.18	0.14
G	0.31	0.566	O	-0.054	0.16
H	0.5	0.426			

Note - Both inner and outer regions are symmetric about zero amplitude axis.

Timing Diagrams

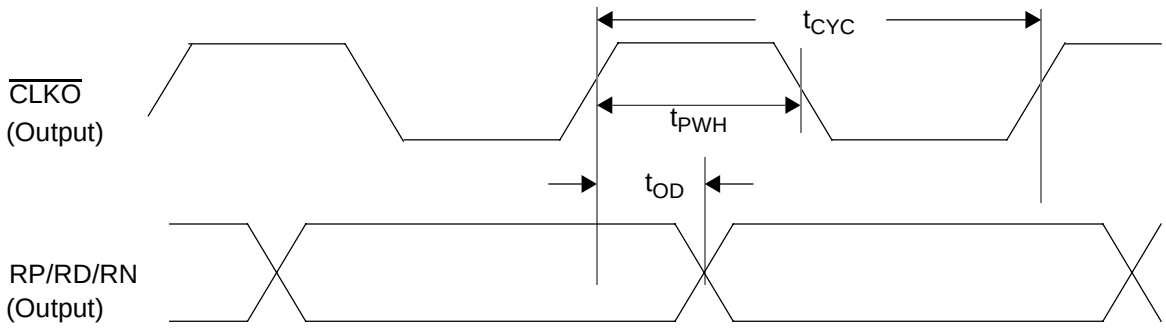
Detailed timing diagrams for the ART and ARTE are provided in Figures 5 through 9, with values of the timing intervals tabulated below them. All output times are measured with a maximum 15 pF load capacitance. Timing parameters are measured at voltage levels of $(V_{OH} + V_{OL})/2$ for output signals or $(V_{IH} + V_{IL})/2$ for input signals.

Figure 5. Receiver CLKO to Data Output Timing



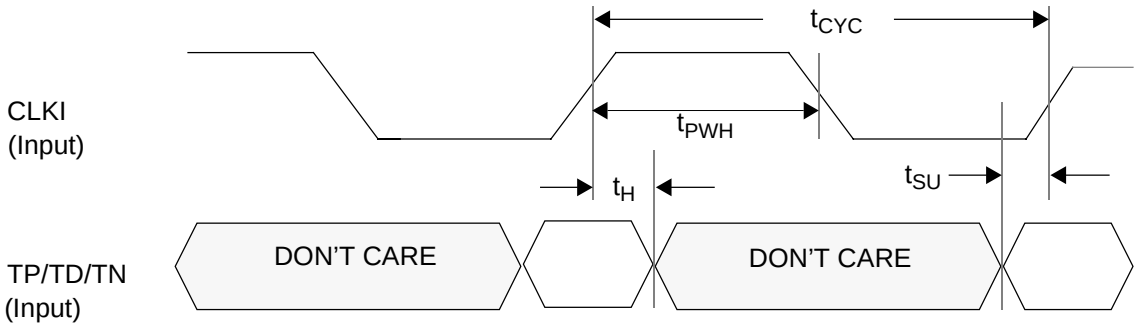
Parameter	Symbol	Min	Typ	Max	Unit
CLKO, DS3 output clock period	t_{CYC}		22.353		ns
CLKO, STS-1 output clock period	t_{CYC}		19.290		ns
Output clock duty cycle, t_{PWH}/t_{CYC}	--	45		55	%
RP/RD/RN data output delay after CLKO↓	t_{OD}	0.5		5.0	ns

Figure 6. Receiver $\overline{\text{CLKO}}$ to Data Output Timing



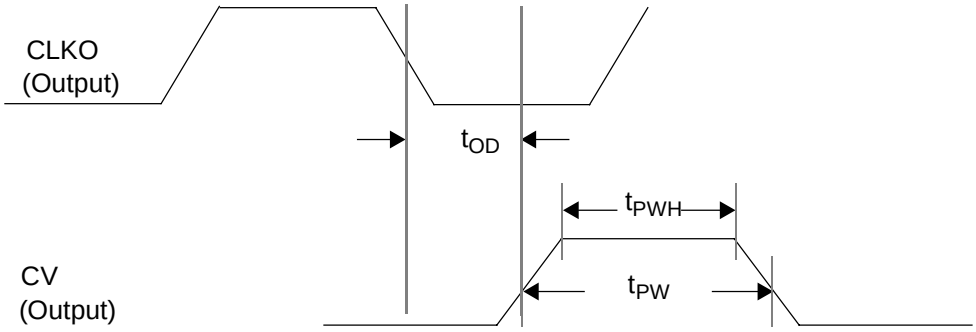
Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{CLKO}}$, DS3 output clock period	t_{CYC}		22.353		ns
$\overline{\text{CLKO}}$, STS-1 output clock period	t_{CYC}		19.290		ns
Output clock duty cycle, t_{PWH}/t_{CYC}	--	45		55	%
RP/RD/RN data output delay after $\overline{\text{CLKO}}$↑	t_{OD}	0.75		5.0	ns

Figure 7. Transmitter Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
CLKI, DS3 input clock period	t_{CYC}		22.353		ns
CLKI, STS-1 input clock period	t_{CYC}		19.290		ns
Input clock duty cycle, t_{PWH}/t_{CYC}	--	40		60	%
TP/TD/TN data stable to CLKI↑ setup time	t_{SU}	3.0			ns
CLKI↑ to TP/TD/TN data stable hold time	t_H	2.0			ns

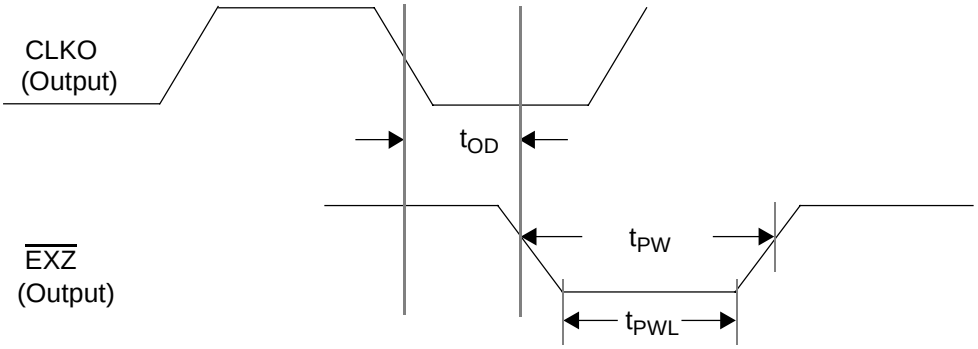
Figure 8. Coding Violation Pulse Timing



Parameter	Symbol	Min	Typ	Max	Unit*
CV pulse width	t_{PW}	0.9	1.0	1.1	UI
CV pulse high time	t_{PWH}	0.8	0.9	1.0	UI
CV delay from occurrence of violation	t_D		7.0		UI
CV Output delay after CLKO↓	t_{OD}	0.5		5.0	nS

*Note: UI = 1 / (System Clock Frequency)

Figure 9. Excessive Zeros Pulse Timing



Parameter	Symbol	Min	Typ	Max	Unit*
$\overline{EXZ}$ pulse width	t_{PW}	0.9	1.0	1.1	UI
$\overline{EXZ}$ pulse low time	t_{PWL}	0.8	0.9	1.0	UI
$\overline{EXZ}$ delay from occurrence of violation	t_D		7.0		UI
$\overline{EXZ}$ Output delay after CLKO↓	t_{OD}	0.5		5.0	nS

*Note: UI = 1 / (System Clock Frequency)

OPERATION

Receiver Input Requirements

Parameter	Value
Interface Cable	AT&T 728A/734A coaxial cable (or equivalent)
Bit Rate:	
DS3	44.736 Mbit/s ± 20 ppm
STS-1	51.840 Mbit/s ± 20 ppm
Line Code	B3ZS
Input Signal Amplitude:	
Single-Ended Input	35 mVp - 0.95 Vp AC (measured relative to other pin used for DC bias, DI1 or DI2)
Differential Input	35 mVp - 0.95 Vp AC (magnitude of differential amplitude between DI1 and DI2)
Dynamic range	28.5 dB
Cable Length	0 - 900 feet (for signals meeting the transmit masks)
Input Return Loss:	
DS3	> 26 dB at 22.368 MHz with external 75Ω resistor, effect of external transformer excluded
STS-1	> 26 dB at 25.920 MHz with external 75Ω resistor, effect of external transformer excluded
Input Resistance	> 5KΩ
Signal-to-Noise Tolerance	No greater than either the value produced by adjacent pulses in the data stream or ±10% of the peak pulse amplitude, whichever is greater.
Input Jitter Tolerance	As defined by Figures 11a and 11b: “ART and ARTE Input Jitter Tolerance”*
Signal Coupling	The input signal must be AC coupled to the ART via a transformer or capacitor.
DLOS Input level	A “0” is defined as a signal of amplitude ≤ 15 mVp at the receiver input.

*Note:
Refer to Operation - Jitter Tolerance section below for DS3 and STS-1 minimum requirements and measured values.

Interfering Tone Tolerance

The ART will properly recover clock and present error-free output to the receive terminal side interface* in the presence of a sinusoidal interfering tone signal at the following line rates:

Interfering Tone Tolerance

Data Rate (Mbit/s)	Tone Frequency (MHz)	Maximum Tone Level
51.84	25.97	-20 dB
44.736	22.4	-20 dB

*Note: See Figure 12: “Interference Margin Test Configuration”

Receiver Output Specifications

Parameter	Value
Clock Recovery Jitter Peaking	1 dB maximum
Clock Recovery PLL pull-in time	< 100 μS
Sequences Reported as Coding Violations	++, --, not B0V, not 00V, three or more consecutive zeros (excessive zeros)

Transmitter Specifications

Note: A 75 ohm ±5% output load is assumed in these specifications. Measurements made at transmitter unless otherwise noted.

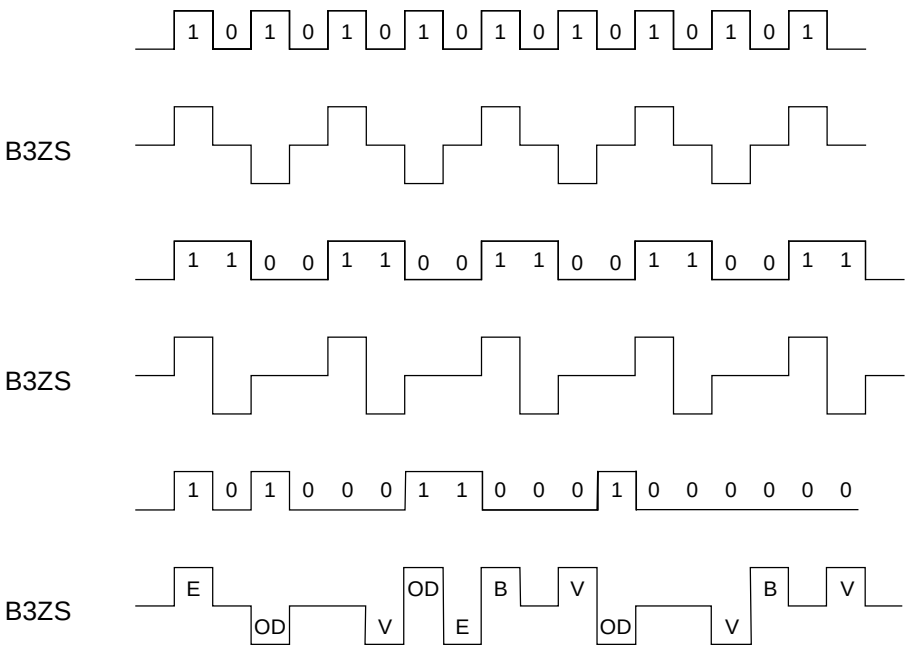
Parameter	Value
DO1/DO2 Output Characteristics:	
Amplitude	±1.75 volts ±10%
Pulse Width	1/2 UI ±10%*
Rise Time	2.5 ±1.5 nS
Overshoot/Undershoot	< 10%
Pulse Imbalance	Ratio of positive and negative pulse amplitudes: 0.9 - 1.10.
Pulse Symmetry	Output power at system frequency > 20 dB below the level at 1/2 the system frequency
DOUT Output Characteristics, $\overline{\text{ZERO}}$ high:	
Pulse Shape (DS3)	As defined by Figure 2 in ANSI TI.404-19XX, TIE1.2/93-004 for 50 to 450 feet. of coaxial cable.
Pulse Shape (STS-1)	As defined by Figure 4-10 in TA-NWT-000253, Issue 8, October 1993 for 50 to 450 feet of coaxial cable.
Amplitude	±0.81 volts ±10%
Output jitter	0.05 UI maximum with jitter-free input clock on CLKI
Output Power for STS-1	Between -2.7 and +4.7 dBm for a STS-1 framed pattern in a wide-band power measurement. The measurement equipment should have a low-pass filter having a flat passband with a cutoff frequency of 207.360 MHz. The effects of a range of connecting coaxial cable lengths from 225 feet to 450 feet must be included in the measurement. This measurement is defined in ANSI T1.102-1993.
Output Power for DS3	Between -4.7 and +3.6 dBm for a framed AIS pattern in a wide-band power measurement. The measurement equipment should have a low-pass filter having a flat passband with a cutoff frequency of 200 MHz. The effects of a range of connecting coaxial cable lengths from 225 feet to 450 feet must be included in the measurement. This measurement is defined in ANSI T1.102-1993.
All Ones Output Power for DS3	Between -1.8 and +5.7 dBm for an all ones signal measured using a bandpass filter with a 3 dB bandwidth of 3 kHz ±1 kHz centered at 22.368 MHz.This measurement is defined in ANSI T1.102-1993 and TA-TSY-000342.
Pulse Imbalance	Ratio of positive and negative pulse amplitudes: 0.9 - 1.10.
Pulse Symmetry	Output power at system frequency > 20 dB below the level at 1/2 the system frequency

This table is continued on the next page.

Parameter	Value
DOUT Output Characteristics, ZERO low:	
Pulse Shape (DS3)	As defined by Figure 2 in ANSI TI.404-19XX, TIE1.2/93-004, with 0 to 100 feet of output cable
Pulse Shape (STS-1)	As defined by Figure 4-10 in TR-TSY-000253, with 0 to 100 feet of output cable
Amplitude	±0.67 Volts ±10%
Pulse Shape (DS3)	As defined by Figure 9.6 in TR-TSY-000499
Pulse Imbalance	Ratio of positive and negative pulse amplitudes: 0.9 - 1.10.
Pulse Symmetry	Output power at system frequency > 20 dB below the level at 1/2 the system frequency

*Note: UI = 1 / (System Clock Frequency)

B3ZS PATTERNS



E = indicates even number of pulses since last violation (V).

OD = indicates odd number of pulses since last violation (V).

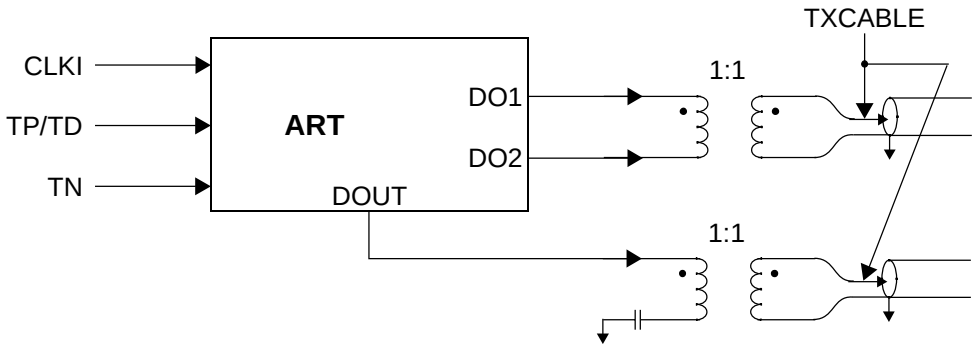
V = inserted pulse, in intentional violation of alternating plus and minus pulses used for 1's.

B = inserted pulse that follows the normal alternating Bipolar coding scheme (i.e., polarity opposite to preceding pulse).

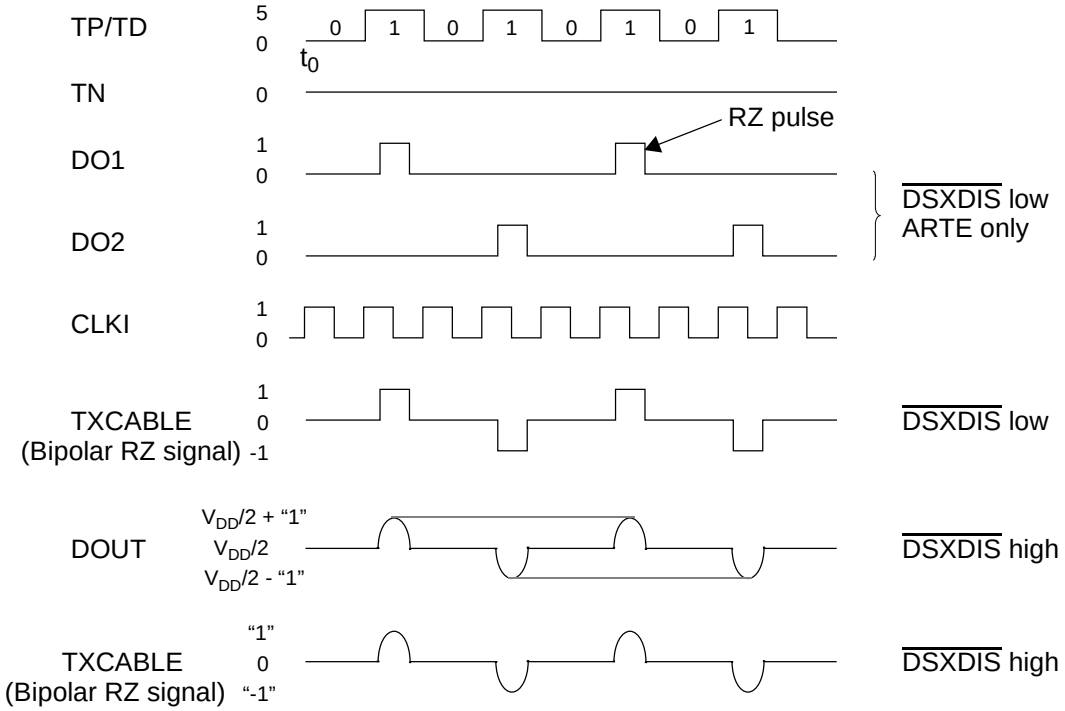
Note: Three consecutive zeros are replaced with B0V or 00V; the substitution choice is made so that the number of pulses between inserted violation pulses (V's) is odd; note that sequential violations are of opposite polarity so the net charge on the transmission medium is zero.

Figure 10a. Examples of B3ZS Coding

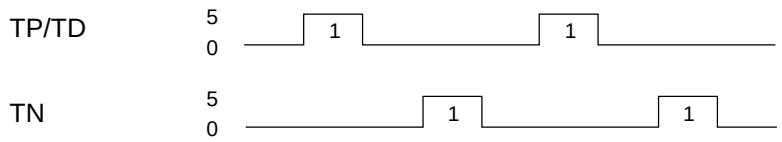
Figure 10b. Examples of Idealized Transmit Input and Output Data



Unencoded NRZ Data (0 1 0 1 0 .....)



Encoded NRZ P & N Data (0 1 0 1 0 ....)



DO1, DO2, DOUT, CLKI and TXCABLE are the same as in the unencoded NRZ case.

AIS and Loopback Control Signal Arbitration

$\overline{\text{TEST0}}$	$\overline{\text{TEST1}}$	$\overline{\text{RAIS}}$	$\overline{\text{TAIS}}$	$\overline{\text{LNLBK}}$	$\overline{\text{TRLBK}}$	RX Terminal Output	TX Line Output
1	1	1	1	1	1	Normal	Normal
1	1	1	0	X	1	Normal	AIS
1	X	1	0	X	0	Digital T_{erm} Loopback	AIS
1	X	0	1	1	X	AIS	Normal
1	X	0	1	0	X	AIS	Line Loopback
1	X	0	0	X	X	AIS	AIS
1	1	1	1	1	0	Digital T_{erm} Loopback	Normal
1	1	1	1	0	1	Normal	Line Loopback
1	1	1	1	0	0	Digital T_{erm} Loopback	Line Loopback
1	0	1	1	1	1	T_{erm} Loopback*	Normal
0	1	1	X	X	1	Normal	PRBS
0	0	1	X	X	1	T_{erm} Loopback of PRBS*	PRBS
0	X	1	X	X	0	Digital T_{erm} Loopback*	PRBS

* Through clock recovery block for terminal transmit data in ARTE device.

Notes: X = Don't Care. $\overline{\text{TEST0}}$ and $\overline{\text{TEST1}}$ inputs are provided only on ARTE device. Digital Term Loopback means that the terminal side transmitter inputs are looped digitally, directly to the terminal side receiver outputs.

Power-Down Mode

In order to reduce the current required by the ART when either the transmitter or receiver is not used, the following power pins may be tied to ground:

ART, 44-Pin Package*:*
Receiver-Only Operation: AVDDTX pins 5, 6, 37.
Transmitter-Only Operation: AVDDRX pins 25, 28, 30.

ARTE, 68-Pin Package:
Receiver-Only Operation: AVDDTX pins 4, 5, 54, 55.
Transmitter-Only Operation: AVDDRX pins 37, 43, 47.

Current reduction in the Power-Down Mode is as follows:

Receiver-Only Operation: I_{DD} is reduced by approximately 10 mA.
Transmitter-Only Operation: I_{DD} is reduced by approximately 80 mA.

Note: Power must be provided to the AVDDTPLL pin in all three operational modes (Receiver and Transmitter, Receiver-Only, Transmitter-Only). Refer to Figure 13a and associated Note 9 for power supply connections.

Jitter Transfer

Transfer of jitter through an individual unit of digital equipment is characterized by the relationship between the applied input jitter and the resulting output jitter as a function of frequency. This standard does not apply to Line Interface Units as the recovered data is either re-transmitted with a local oscillator or is re-transmitted with the recovered clock that has been dejittered using a dejitter PLL. In short, the recovered clock is never used to directly transmit data. Studying the jitter tolerance curve highlights the reason why this is not possible. The receive PLL bandwidth is dictated by the jitter tolerance curve. This prevents the clock recovery having the low bandwidth necessary for low jitter in the low frequencies necessary for transmitting.

The measurement made with the test setup shown in Figure 10c is for information only. The measurement of the jitter on CLKO is a measure of the characteristics of the clock recovery PLL, not how much jitter is transferred from the receiver input to the transmitter output.

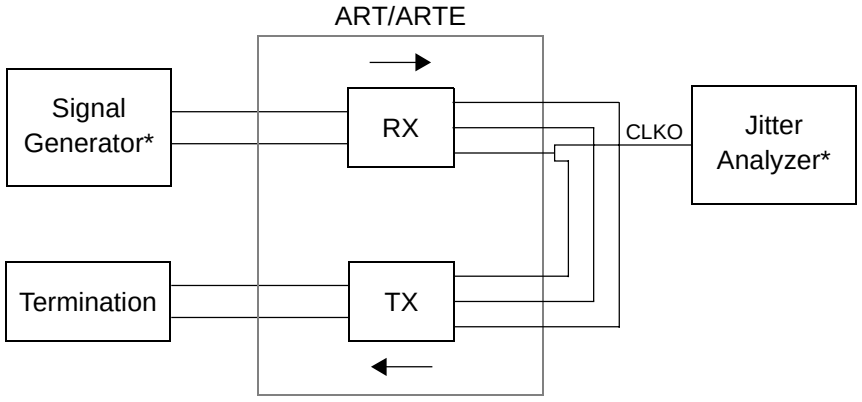
For DS3, Bellcore Technical Reference TR-TSY-000499, Issue 3, December 1989 further describes and defines jitter transfer.

For STS-1, Bellcore Technical Reference TR-NWT-000253, Issue 2, December 1991 further describes and defines jitter transfer.

When operating in a looped-back configuration (through the receive path and externally looped back through the transmit path), in the absence of applied input jitter the amount of jitter introduced by the ART and ARTE devices is maximum 0.065 Unit Intervals (UIs, where UI is 1 / System Clock Frequency) of peak-to-peak jitter over a jitter frequency range of 20 Hz to 1 MHz (filter with a high-pass of 10 Hz and a low-pass of 1.1 MHz).

The test arrangement illustrated in Figure 10c is recommended for performance of the jitter transfer test. This test is made by adding jitter to the line side data inputs (DI1 and DI2) and measuring the jitter at the terminal side receiver clock output (CLKO). Intrinsic test equipment jitter must be subtracted from the measurement. The receiver outputs (RP/RD, RN and CLKO) are looped back to the transmitter inputs (TP/TD, TN and CLKI) using cables. The transmitter is activated to ensure that there is no crosstalk between the transmitter and receiver.

.



* Hewlett Packard HP3784A Digital Transmission Analyzer, or equivalent.

Figure 10c. Jitter Transfer Test Arrangement

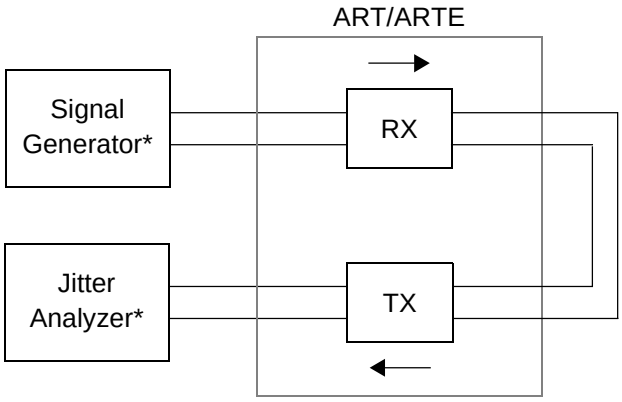
Jitter Generation

Jitter generation is the process whereby jitter appears at the output port of an individual unit of digital equipment in the absence of applied input jitter.

For DS3, Bellcore Technical Reference TR-TSY-000499, Issue 3, December 1989 specifies the maximum jitter generation to be 1.0 UI of peak-to-peak at the output of the terminal receiver for Category I equipment.

For STS-1, Bellcore Technical Reference TR-NWT-000253, Issue 2, December 1991 specifies the maximum jitter generation to be 1.5 UI peak-to-peak maximum at the output of the terminal receiver for Category I equipment.

The test arrangement illustrated in Figure 10d is recommended for performance of the jitter generation test. This test is made by adding jitter to the inputs of the receiver, looping the receiver outputs to the transmitter inputs with cables, and then measuring the jitter at the output of the transmitter. No jitter filter is used. Intrinsic test equipment jitter must be subtracted from the measurement. The DS3/STS-1 jitter generation within the ART and ARTE devices is 0.145 UI peak-to-peak maximum for all frequencies specified in the two standards referenced above. Note that the test is a worst case measurement as the clock recovery PLL adds a significant amount of jitter. In normal operation, the transmit clock is either based on a local oscillator or is coming from a VCXO of a dejitter PLL.



* Hewlett Packard HP3784A Digital Transmission Analyzer, or equivalent.

Figure 10d. Jitter Generation Test Arrangement

Jitter Tolerance

DS3:

Input jitter tolerance is the maximum amplitude of sinusoidal jitter at a given jitter frequency, which, when modulating the signal at an equipment port, results in no more than two errored seconds cumulative, where these errored seconds are integrated over successive 30-second measurement intervals, and the jitter amplitude is increased in each succeeding measurement interval.

Requirements for input jitter tolerance are specified in terms of compliance with a jitter mask, which represents a combination of points. Each point corresponds to minimum amplitude of sinusoidal jitter at a given jitter frequency which, when modulating the signal at an equipment input port, results in two or fewer errored seconds in a 30-second measurement interval. Bellcore Technical Reference TR-TSY-000499, Issue 3, December 1989 specifies the minimum requirement mask for Category II equipment. The mask is shown in Figure 11a.

Jitter tolerance within the ART and ARTE meets and exceeds the performance requirements. Figure 11a presents the DS3 Bellcore minimum jitter tolerance requirement mask and measured performance.

STS-1:

For STS-1, jitter tolerance is specified in Bellcore Technical Reference TR-NWT-000253. The minimum requirement mask is shown in Figure 11b.

Jitter tolerance within the ART and ARTE meets and exceeds performance requirements. Figure 11b presents the Bellcore STS-1 minimum jitter tolerance requirement mask and measured STS-1 performance.

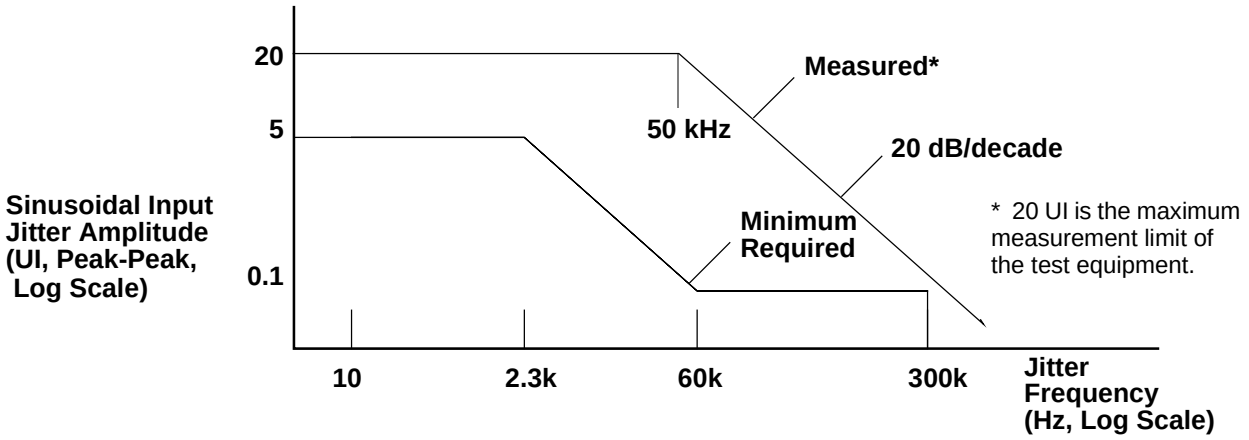


Figure 11a. ART and ARTE Input Jitter Tolerance for DS3

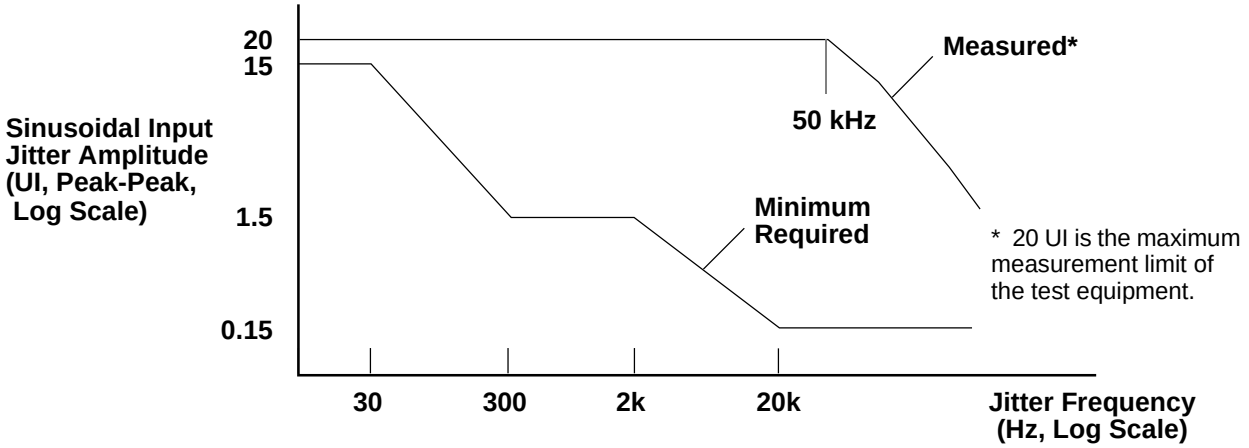


Figure 11b. ART and ARTE Input Jitter Tolerance for STS-1

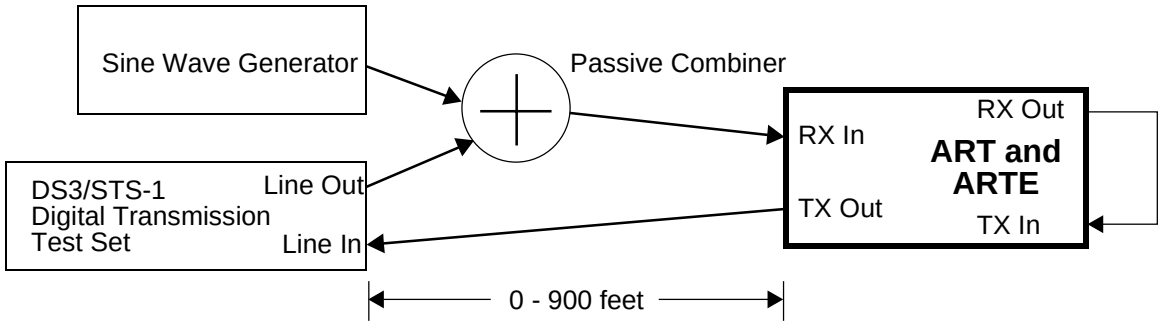


Figure 12. Interference Margin Test Configuration

Physical Design

Introduction

High-frequency design techniques must be employed for layout of the printed circuit board on which the ART or ARTE device is mounted. A summary of the special design requirements is provided below. More details are available in TranSwitch Application Note AN-406, Guidelines for ART/ARTE Printed Circuit Board Layout, Document No. TXC-02020-AN1.
The following guidelines and suggestions should be adhered to for a successful board design. At the DS3 and STS-1 frequencies it is important to use high-frequency layout techniques. The techniques discussed below are the bare minimum set that should be used.

A solid ground plane with notches should be used. 'Solid' in this instance means that the impedance from any point in the plane to the board ground connection should be low. The means having as much metal left in the plane as possible. This is very important in regards to the location of the analog ART/ARTE device since its SNR can be severely degraded by I*Z drops in these planes. Notching is used to direct (i.e., steer) noise-induced current away from the ART/ARTE ground return path. Under no circumstances should an ART/ARTE ground region be connected to the "ground" through a trace. The trace is an impedance at high frequencies; it is not a short. Ground currents through the trace impedance will cause voltage noise. Do not run AC signals across the notches in the ground plane as this will produce an impedance discontinuity and signal integrity will be affected.

Try to locate the ART/ARTE so that no high current devices (such as oscillators or drivers) are located in line with the ART/ARTE connection to card ground.

Do not use a solid power plane. Break the power plane into regions. Placing the power and ground planes in adjacent layers will produce an additional noise reduction due to capacitive coupling. For example, a six-layer board could be signal-signal-power(ground)-ground(power)-signal-signal. The following is the list of power regions:

1. Analog Receiver power, AVDDRX
2. Analog Transmitter power, AGNDTX
3. Analog PLL power, AVDDTPLL
4. ART digital power, VDD
5. Board VDD

If ferrite beads are used in the analog power lines, as is recommended, there will be a narrowing of the power plane at the ferrite bead. If the beads are not used, use as wide a path as possible back to the common connecting point. It should be noted that not using the beads may cause a large SNR reduction in the transceiver. The effect is highly board-dependent and not easily predictable.

Figures 13a and 13b show the recommended ground and power connections for the ART/ARTE. The passive components should be connected to the indicated ground (a solid plane with possible notching). Connecting the components to the wrong point will inject a noise signal into that part of the transceiver. Do not use a long trace to connect components to ground; use as short a trace as possible. The decoupling capacitors should be placed ***as close as feasible*** to their associated chip pins on the same board side as the ART/ARTE chip. Put a decoupling capacitor at every power pin. Placing the capacitors on the other side of the board may have a measurable impact on device performance. Again, it should be pointed out that a board trace is an impedance, not a short. The other passive components should also be placed ***as close as possible*** to their associated pins.

The ART/ARTE terminal side CMOS output drivers have a drive of 4 mA. If driving long traces (the longer the trace, the greater the parasitic capacitance) or multiple loads these outputs may need to be buffered.

The notes following Figure 13c give external component values and types, a listing of the various power and ground connections, and other information.

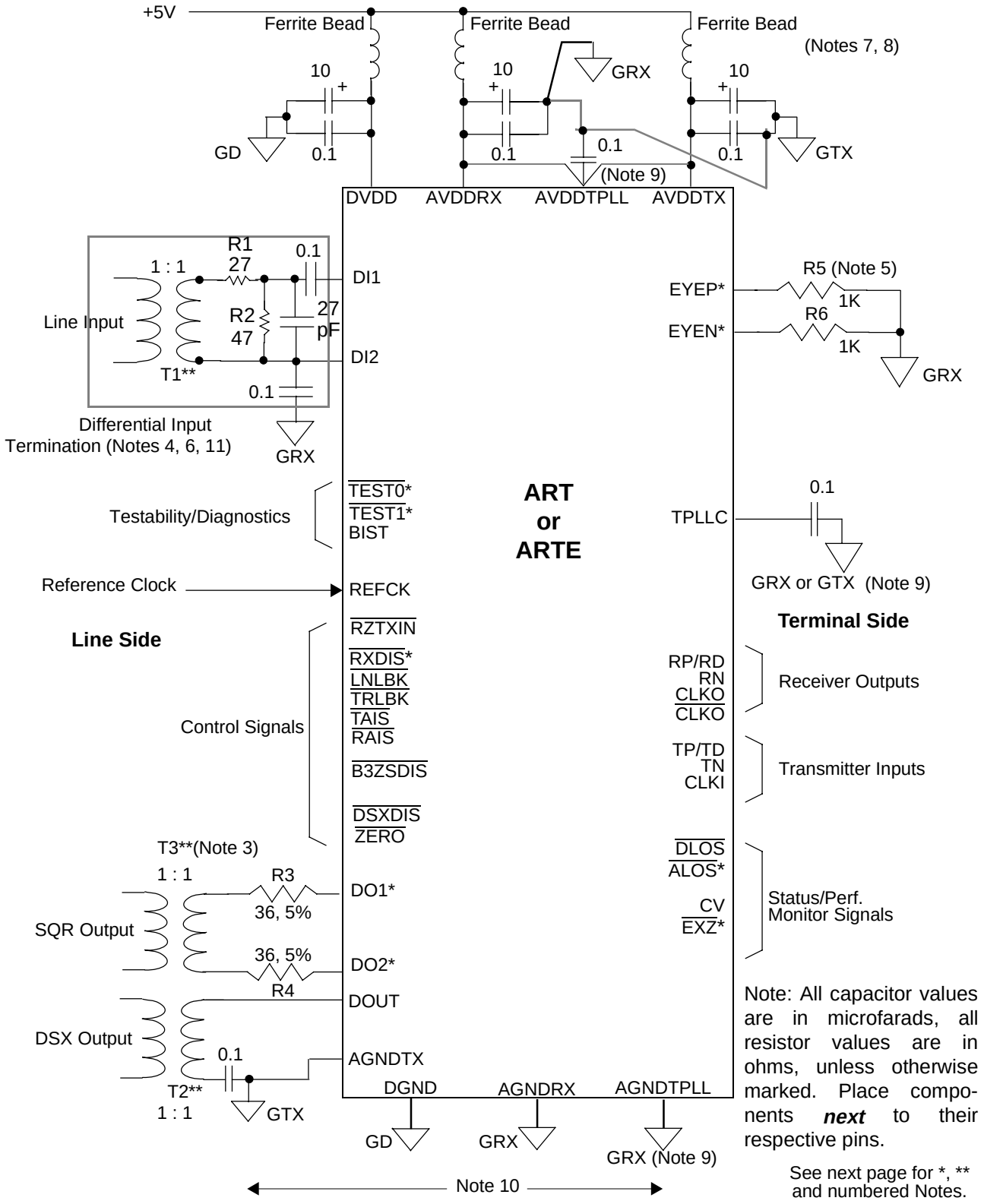
General Comments

A board trace at high frequencies is not a zero-impedance metal interconnection. It is a distributed L/C network. The values of the L and C (per unit length) parasitic components are determined by trace geometry (width and height) and the surrounding material (which determines the dielectric constant). A trace with a given geometry will have a different impedance if it is on an outside board layer from the same trace placed instead in an internal layer. Large branches (stubs) off a main trace will change the impedance at the branch point due to the effect of impedances in parallel, so branch lengths should be kept to a minimum (less than a quarter wavelength). This is very important for clock lines where load/source impedance mismatches can cause severe ringing, which leads to timing problems. Use buffers to reduce the difficulty of distributing a signal with multiple loads.

If relays are used to switch the transceivers in and out, use the 50 ohm shielded variety to minimize crosstalk, especially from the power used to energize the relay. Match the impedance of the board traces of the transmitter outputs and receiver inputs to the transmission line impedance (75 ohms if a 1:1 transformer is used) to minimize reflections. Physically separate the analog signal lines from the digital lines. Route the differential receiver lines side by side to make coupled noise common-mode. Avoid ninety-degree corners in the board lands; keep lands as straight and short as possible. Use terminating (i.e., 51 ohm series-damping) resistors in the digital signals lines where appropriate (i.e., if the line is longer than a quarter wavelength of the highest signal frequency of importance, reflections will start causing problems).

The above comments are guidelines only. High-frequency board layout is difficult and must be done with care. A bad board layout will reduce the SNR of the transceiver and cause timing problems with the board logic, perhaps to the point of requiring a complete board redesign.

Figure 13a. External Components, Pin Connections and Power/Grounds



Note: All capacitor values are in microfarads, all resistor values are in ohms, unless otherwise marked. Place components ***next*** to their respective pins.

See next page for *, ** and numbered Notes.

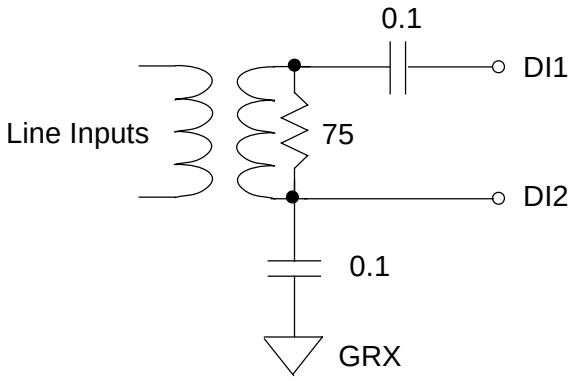


Figure 13b. Single-Ended Receive Termination

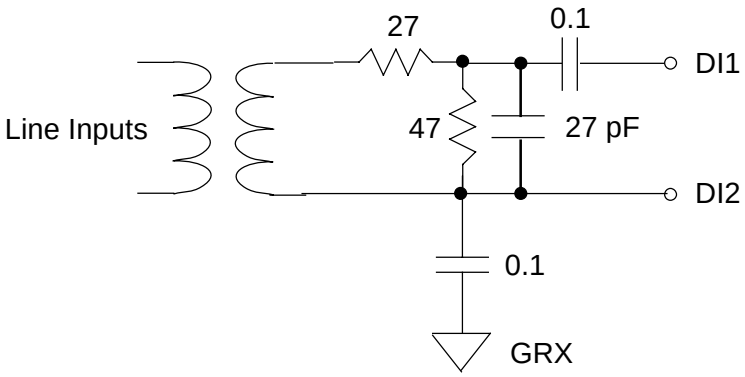


Figure 13c. Suggested Single-Ended Termination Circuit for Non-Monitor Functions

NOTES:

1. *The nine device signal terminations marked with asterisks are provided for the ARTE but not for the ART.
2. **T1, T2 and T3 are Coilcraft WB1010 Transformers or equivalent.
3. T3 is optional. T3 is only required if the ARTE square wave transmit output is used (DO1, DO2).
4. R1 and R2 are 1% resistors.
5. R5 and R6 are only required for ARTE monitoring purposes, not for device operation.
6. Differential Input Termination for line inputs can be replaced by circuit in Figure 13b for single-ended operation.
7. Fair Rite #2743002111 or equivalent should be used for each ferrite bead.
8. Locate ferrite bead/capacitor decoupling as close as possible to ART and ARTE. Locate the 10 µF capacitor as close as possible to the ferrite bead, and place an individual 0.1 µF capacitor as close as possible to each voltage pin on ART/ARTE.
9. Power Connections for Transmit PLL: Avoid trace for power connection if possible. Use a decoupling capacitor. Connect AVDDTPLL, AGNDTPLL and TPLLC as follows:

Operating Mode	AVDDTPLL Connection	AGNDTPLL	TPLLC Cap Ground
Receive and Transmit	AVDDRX	GRX	GRX
Receive Only	AVDDRX	GRX	GRX
Transmit Only	AVDDTX	GTX	GTX

10. GD=Digital Ground; GRX=Analog Receive Ground; GTX=Analog Transmit Ground.
11. Figure 13c is the single-ended circuit suggested for future board designs in a non-monitor function. The resistive attenuator will decrease high frequency noise and prevent the AGC from operating near its linear range limits.

PACKAGE INFORMATION

ART is available in a 44-pin plastic leaded chip carrier (ART) and also with extended features in a 68-pin plastic leaded chip carrier (ARTE). Both packages are suitable for socket or surface mounting. All dimensions shown are in inches and are nominal values unless otherwise indicated.

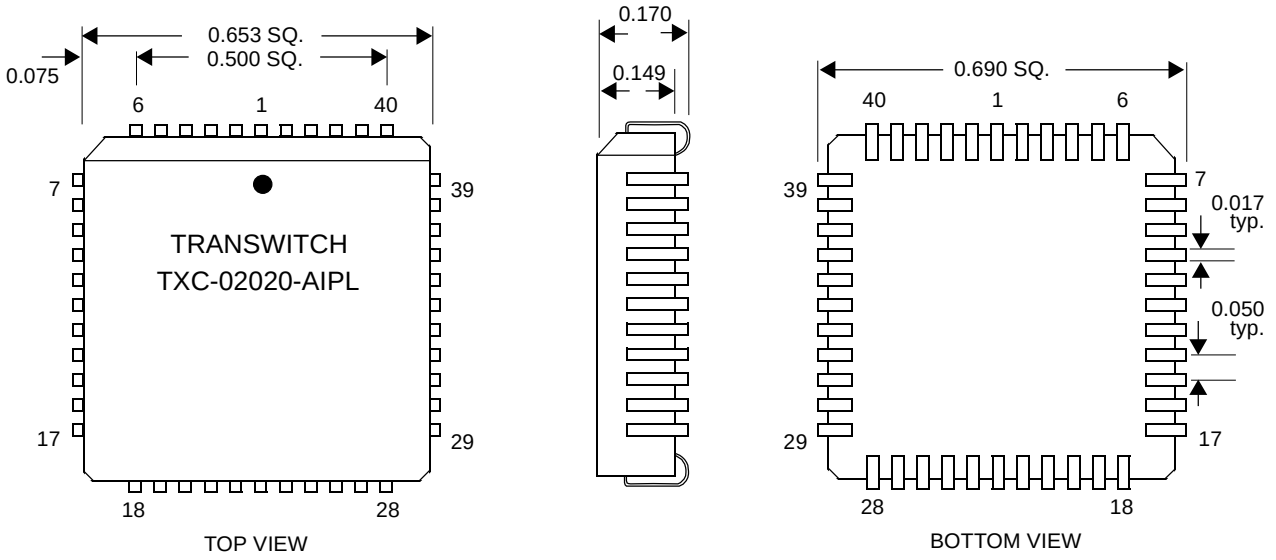


Figure 14. ART in a 44-Pin Plastic Leaded Chip Carrier

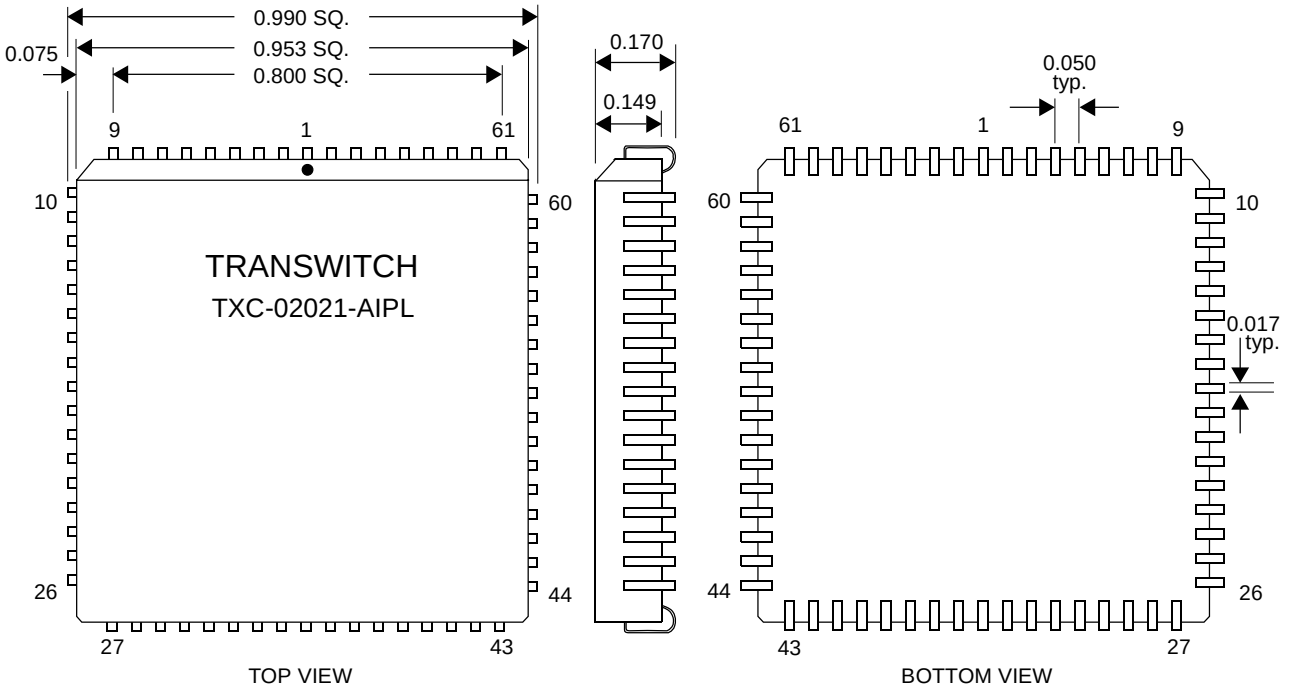


Figure 15. ARTE in a 68-Pin Plastic Leaded Chip Carrier

ORDERING INFORMATION

ART Part Number:	TXC-02020-AIPL	44-pin plastic leaded device carrier
ARTE Part Number:	TXC-02021-AIPL	68-pin plastic leaded device carrier

RELATED PRODUCTS

TXC-20153D and TXC-20153G, DS3LIM-SN DS3/STS-1 Line Interface Module. A complete analog to digital DS3/STS-1 line interface in a compact 2.6 square-inch DIP module. Includes selectable B3ZS line encoding/decoding.

TXC-02050, MRT Multi-Rate Line Interface VLSI Device. The MRT provides the functions for terminating ITU-specified 8448 kbit/s (E2) and 34368 kbit/s (E3) line rate signals, or 6312 kbit/s (JT2) line signals specified in the Japanese NTT Technical Reference for High Speed Digital Leased Circuits. An optional HDB3 codec is provided for the two ITU line rates.

TXC-03303, M13E DS3/DS1 Mux/Demux VLSI Device. This multiplex/demultiplex device provides the complete interfacing function between a single DS3 signal and 28 independent DS1 signals. The M13E has Extended features relative to the predecessor M13 (TXC-03301).

TXC-03401B, DS3F DS3 Framer VLSI Device. Maps broadband payloads into the DS3 frame format. Operates in either the C-bit parity or M13 operating modes.

TXC-03001B, SOT-1 SONET STS-1 Overhead Terminator VLSI Device. The SOT-1 provides the SONET interface to any payload. Provides access to all of the transport and path overhead defined for an STS-1/STS-N SONET signal.

TXC-06125, XBERT Bit Error Rate Generator Receiver VLSI Device. Programmable multi-rate test pattern generator and receiver in a single device with serial, nibble, or byte interface capability.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

The ATM Forum:

ATM Forum World Headquarters
303 Vintage Park Drive
Foster City, CA 94404-1138

Tel: 415-578-6860
Fax: 415-525-0182

ATM Forum European Office
14 Place Marie - Jeanne Bassot
Levallois Perret Cedex
92593 Paris France

Tel: 33 1 46 39 56 26
Fax: 33 1 46 39 56 99

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

EIA - Electronic Industries Association (U.S.A.):

Global Engineering Documents
Suite 407
7730 Carondelet Avenue
Clayton, MO 63105

Tel: 800-854-7179 (In U.S.A.)
Fax: 314-726-6418

ITU-T (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (T)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

MIL-STD Military Standard (U.S.A.):

Standardization Documents Order Desk
700 Robbins Avenue
Building 4D
Philadelphia, PA 19111-5094

Tel: 212-697-1187
Fax: 215-697-2978

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated ART and ARTE Data Sheet that have significant differences relative to the previous and now superseded ART and ARTE Data Sheet:

Updated ART and ARTE Data Sheet: Edition 5, March 1998

Previous ART and ARTE Data Sheet: *PRELIMINARY* Edition 4, March 1995

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Deleted *PRELIMINARY* document status markings and associated explanatory text (from pages 1 and 41). Changed edition number and date.
1	Changed content of Feature 4 and 5. Changed copyright year.
1, 42, 44	Changed street address for TranSwitch Corporation in Shelton, CT.
2	Updated Table of Contents and List of Figures.
3-4	Modified Receiver Functions subsection.
5	Modified Transmitter Functions subsection.
5-6	Modified Loopbacks and AIS Insertion, Testability subsections.
9-12	Identified ART pin as N/A (Not Applicable) for signals provided only in ARTE device.
10	Made changes to Name/Function column for $\overline{\text{EXZ}}$, CV, $\overline{\text{DLOS}}$, $\overline{\text{ALOS}}$, RP/RD, RN and BIST.
10	Added a note to explain how some output signals respond for $\overline{\text{TRLBK}}$ low.
11	Made changes to Name/Function column for TP/TD, TN, CLKI, TPLLC and $\overline{\text{RAIS}}$. Corrected note above Control/Reference Pins table.
12	Made changes to Name/Function column for $\overline{\text{B3ZSDIS}}$, $\overline{\text{ZERO}}$, $\overline{\text{TEST0}}$, $\overline{\text{TEST1}}$, and REFCK.
13	Added last five rows, second note and right column to (renamed) Absolute Maximum Ratings and Environmental Limitations table. Changed Conditions column in second table. Changed Max values in last two rows of last table.
14	Added Note to last table.
18	Made changes in first paragraph.
19	Added CLKO waveform and t_{OD} in Figure 8.
20	Added CLKO waveform and t_{OD} in Figure 9.
21	Modified Receiver Input Requirements table.

Page Number of Updated Data Sheet	Summary of the Change
22	Modified Interfering Tone Tolerance table.
23-24	Modified Transmitter Specifications table
27	Modified AIS and Loopback Control Signal Arbitration subsection.
28	Modified Jitter Transfer subsection.
29	Modified Jitter Generation subsection.
31-32	Modified the Physical Design subsection.
33	Modified Differential Input Termination circuit and Note.
34	Modified Figure 13b. Added Figure 13c. Modified Notes 4 and 9, added Note 11.
35	Added part number to Figure 14 and Figure 15 Top View.
36	Modified Related Products section.
37-38	Modified Standards Documentation Sources section.
39-40	Replaced List of Data Sheet Changes section.
43	Modified Documentation Update Registration Form.

- NOTES -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