ADMA-E1 Device
2 Mbit/s to TU-12 Async Mapper-Desync
TXC-04002

DATA SHEET

FEATURES

- Add/drop two 2048 kbit/s signals from a Virtual Container-4 (VC-4) using Tributary Unit-12s (TU-12s)
- Independent add/drop mode between ports
- Selectable HDB3 positive/negative rail or NRZ E1 interface. Performance counter provided for HDB3 illegal coding violations
- Digital desynchronizer reduces systemic jitter in the presence of multiple pointer movements. A register is also provided to control the internal FIFO leak rate
- Drop buses are monitored for odd parity, loss of clock, and H4 multiframe errors
- Performance counters are provided for TU pointer movements, BIP-2 errors and Far End Block Errors (FEBEs)
- TU-12s are monitored for Loss Of Pointer, New Data Flags (NDFs), AIS, Far End Receive Failures (FERF or RDI), and TU Size Errors (S-bits)
- Access to transmit and receive TU-12 labels and VC-12 overhead communication channels
- E1 loopback, generate BIP-2 errors, and send FERF capability

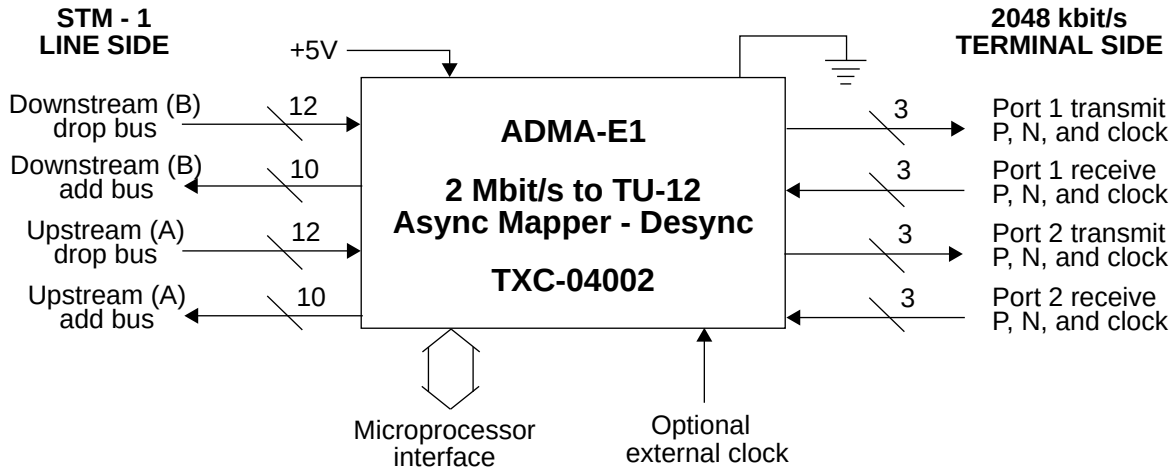
DESCRIPTION

The ADMA-E1 device is designed for add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Two E1 2048 kbit/s signals are mapped to and from asynchronous Tributary Unit - 12s (TU-12s). The ADMA-E1 interfaces to a multiple-segment, byte-parallel, SDH VC-4 formatted bus at the STM-1 byte rate. The E1 2048 kbit/s signals can be either HDB3 positive/negative rail- or NRZ-formatted signals. The ADMA-E1 provides performance counters, alarm detection, and the ability to generate errors and Alarm Indication Signals (AIS). Loopback capability is also provided.

The ADMA-E1 bus interface is used to connect to other TranSwitch devices such as the STM-1/STS-3/STS-3c Overhead Terminator (SOT-3), TXC-03003, to form an STM-1 add/drop or terminal system.

APPLICATIONS

- STM-1 to 2048 kbit/s add/drop mux/demux
- Unidirectional or bidirectional ring applications
- STM-1 termination terminal mode multiplexer
- STM-1 test equipment



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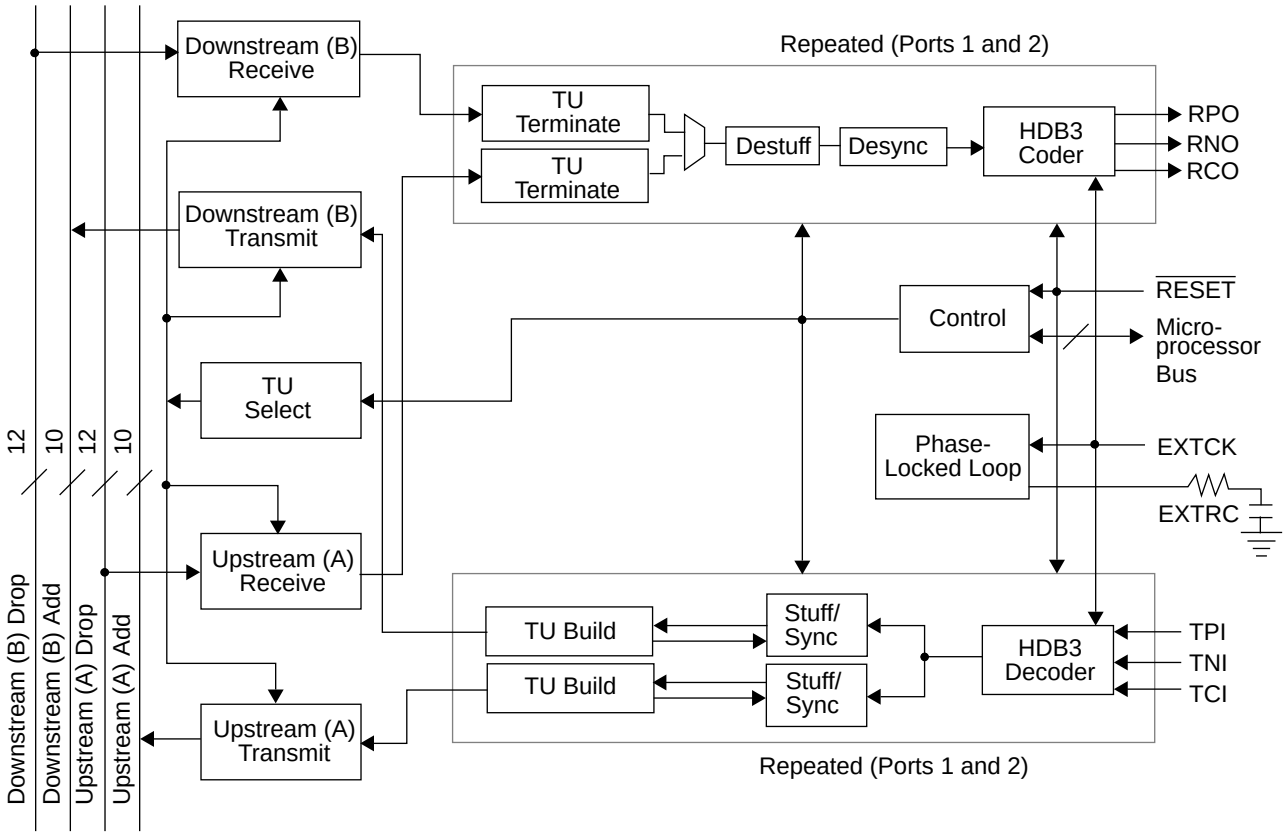


Figure 1. ADMA-E1 TXC-04002 Block Diagram

BLOCK DIAGRAM DESCRIPTION

Figure 1 is a block diagram of the ADMA-E1. The ADMA-E1 interfaces to four buses, designated as upstream (also known as A) drop, upstream (A) add, downstream (also known as B) drop, and downstream (B) add. The four buses run at the STM-1 byte rate of 19.44 Mbytes/s. The asynchronous E1 signals (2048 kbit/s) are carried in floating mode Tributary Unit - 12s (TU-12s) in the STM-1 Virtual Container - 4 structure (VC-4) using the Tributary Unit Group - 2 (TUG-2) mapping scheme. Two E1s can be connected (dropped) from one or both of the drop buses to the E1 lines. Two asynchronous E1 signals are formatted into TUs and connected (added) to either of the add buses (or both, depending upon the mode of operation). The add buses are by definition, byte, frame and multiframe synchronous with their like-named drop buses, but delayed because of internal processing. For example, if a byte from a TU-12 is to be added to the downstream (B) add bus, the time of its placement on the bus is derived from the downstream (B) drop bus timing, and from software instructions specifying which TU number is to be dropped.

The Downstream (B) Receive Block is identical to the Upstream (A) Receive Block. The TU Terminate, Destuff, Desync and HDB3 Line Coder Blocks are also repeated for both ports. Twelve leads are connected between a drop bus and the ADMA-E1 upstream (A) or downstream (B) drop bus interface. The interface consists of a byte clock, byte-wide data, a C1J1 indicator signal, a payload identification signal (SPE) and parity. Depending on the system configuration, buffers and latches may be used between the bus and an ADMA-E1. Each bus is monitored for parity, loss of clock, and H4 multiframe errors. Under microprocessor control, the two receive

blocks extract a TU-12 from the VC-4 for the TU Terminate Blocks. When the ADMA-E1 works with the Tran-Switch SOT-3 device (TXC-03003), an all ones indication is received in the VC-4 E1 byte from the SOT-3 when an STM error (STM-LOP, STM-AIS, etc.) is detected. The ADMA-E1 monitors the VC-4 E1 byte continuously and sends AIS (all ones) downstream (B) to the TU Terminate Block if a majority of ones in the STM-1 TOH E1 byte is detected.

Each Terminate Block performs pointer processing (V1 and V2), path overhead byte (V5) processing, and provides a bit status of the receive overhead communication bits located in the two stuff control bytes in the VC-12 (see Figure 2). The New Data Flag (NDF), TU AIS and TU Loss Of Pointer (TU-LOP) alarms, and a TU-12 size check are performed. Path overhead (V5) byte processing includes a BIP-2 check and a count of the detected errors, counting the number of received Far End Block Errors (FEBEs), the states of the receive label, and a status of the received Far End Receive Failure (FERF) bit, which is also called the Remote Defect Indication (RDI) bit.

Depending on the drop bus selected, the VC-12 is destuffed using majority rule for the two sets of three justification control bits (Cn) which determine if the two S-bits are data bits or justification bits.

The Desync Block removes the effect on the output of Synchronous Digital Hierarchy (SDH) systemic jitter due to signal mappings and pointer movements. The Desync Block contains two parts, a pointer leak buffer, and an E1 loop buffer. The function of the pointer leak buffer is to accept up to five consecutive positive or negative TU-12 pointer adjustments and to ramp out the effect over a specified period of time. The E1 Loop Buffer consists of a digital loop filter, designed to track the frequency of the received E1 signal and to remove both transmission and stuffing jitter. The E1 signal produced has an average frequency equal to the source frequency, and a jitter characteristic meeting the requirements in ITU-TSS Recommendation G.783.

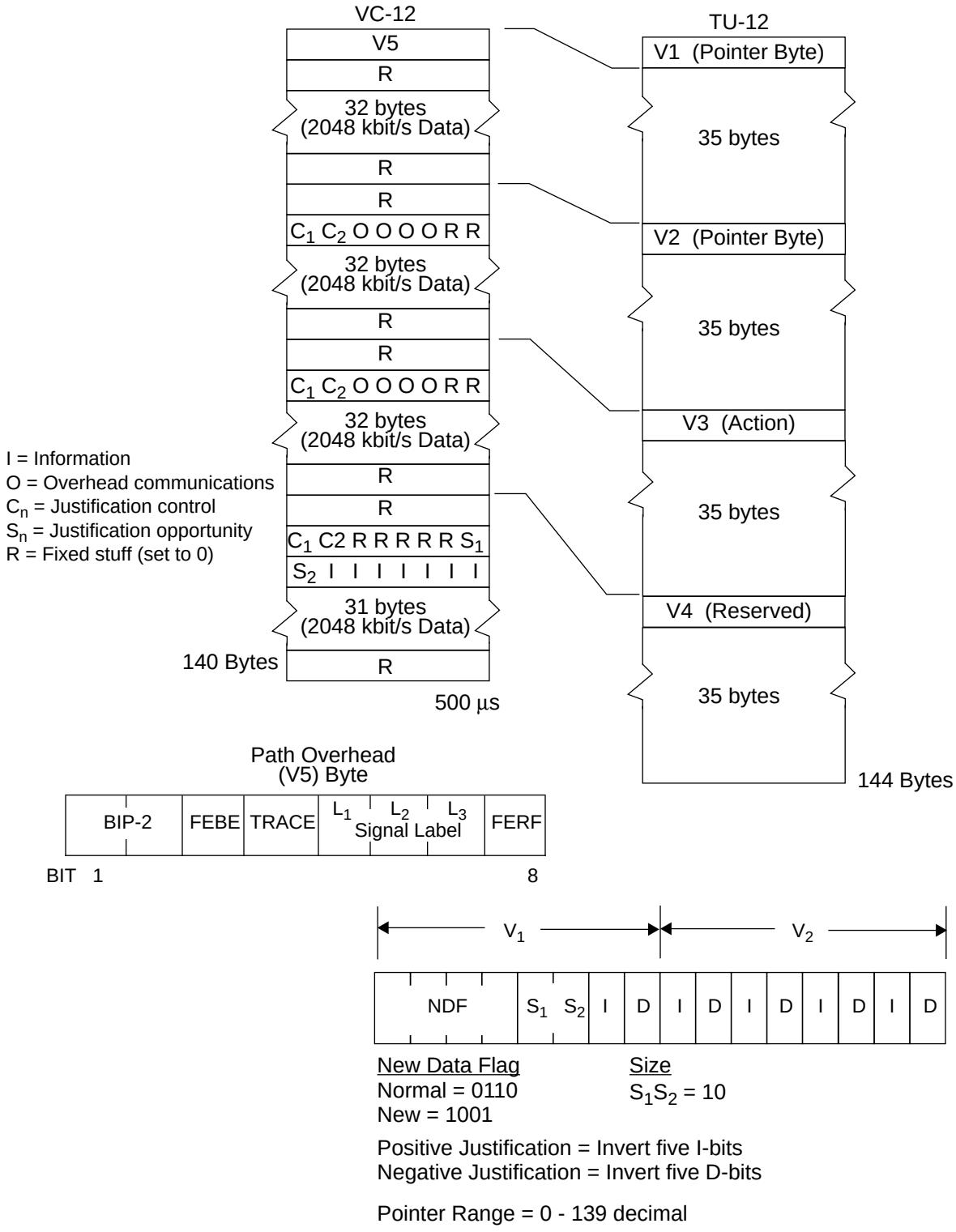
An option for each port provides either NRZ data and clock or an HDB3-coded positive and negative rail signal for the E1 line interface. Transmit data (toward the E1 line) is clocked out of the ADMA-E1 on rising edges of the clock.

Toward the STM-1 add buses, the ADMA-E1 accepts either E1 HDB3-coded positive and negative rail signals or NRZ data. An 8-bit performance counter is provided that counts illegal HDB3 coding violations. The E1 line is monitored for AIS, loss of signal, and clock errors.

The Stuff/Sync Block time buffers the E1 signal for frequency justification by the Stuff Block. The Stuff/Sync Block contains a FIFO for the VC-12 justification process. This block also permits tracking of the incoming signal having an average frequency variation as high as +/-50 ppm, and up to 5 UI of peak-to-peak jitter. The interface between this block and the TU Build Block is bidirectional. The TU Build Block request bits are based on the TU VC-12 phase. The justification algorithm fixes the first S-bit (S1) to the pattern 1110 every four multiframes. The second S-bit contains either data or a justification bit based on a length measurement. Since the ADMA-E1 supports a ring system architecture, two sets of blocks are provided for each port.

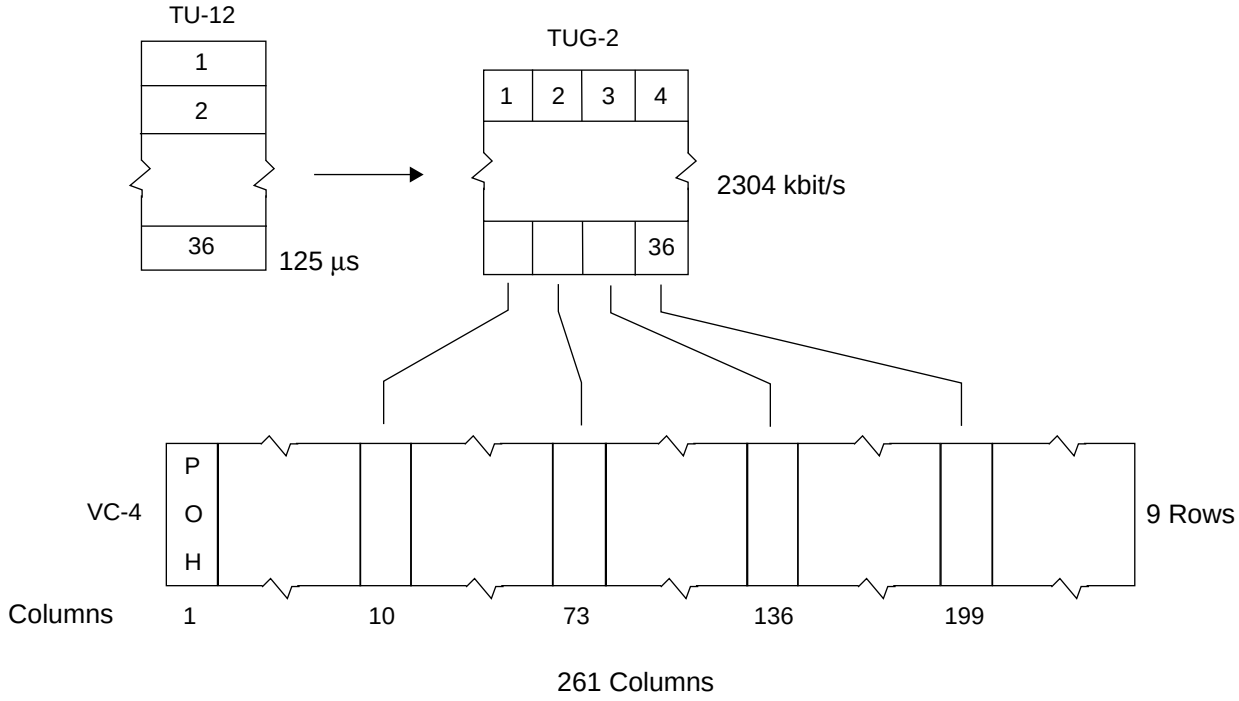
The TU Block formats the TU-12 using the VC-12 structure for asynchronous 2048 kbit/s signals, as shown in Figure 2. The pointer value (in V1 and V2) is fixed to a value of 105. Access is provided for determining the states of the overhead communications channel (O-bits) located in the two stuff control bytes in the VC-12. Access is also provided for transmitting the signal label and the Far End Receive Failure (FERF or RDI) bit, both of which are located in the path overhead byte (V5). The Far End Block Error (FEBE) bit state is determined by the BIP-2 detector in the drop side and the mode of operation. In addition, a control bit is provided that generates an AIS (all ones) in the TU-12.

Figure 2. VC-12/TU-12 Mapping



The TU Block outputs are connected to either or both Upstream (A) / Downstream (B) Transmit Blocks, which format the TU-12 bytes into software selected columns for mapping into the VC-4, as shown in Figure 3. The add interface consists of a tristate data byte, tristate odd parity bit, and an active low add signal. The signals are present only during the selected TU time slot.

Figure 3. TU-12/VC-4 Mapping



PIN DIAGRAM

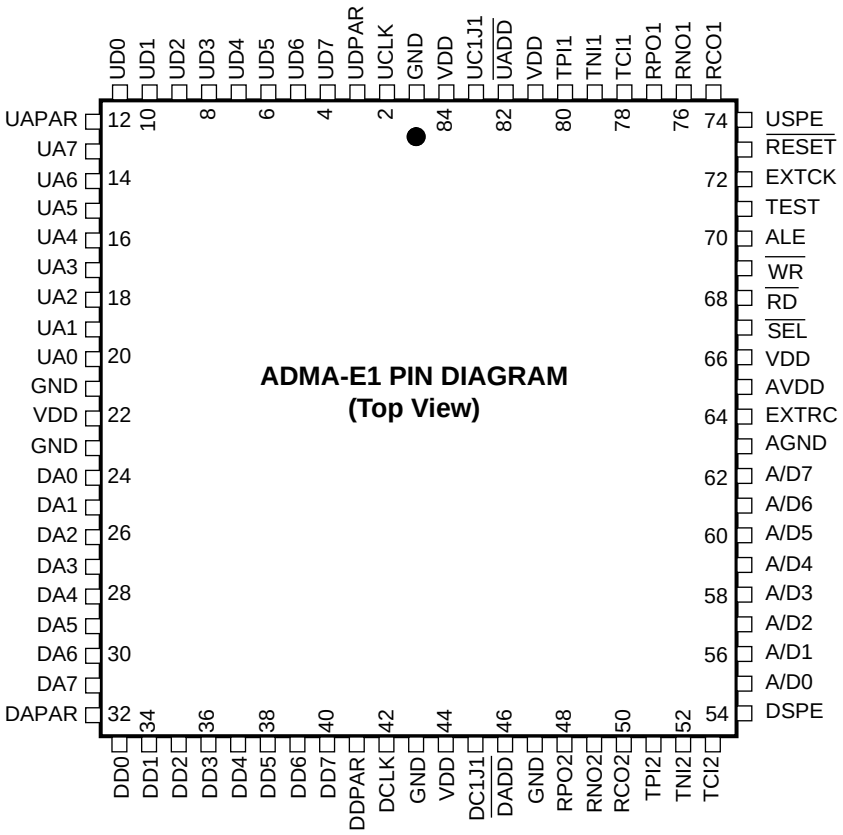


Figure 4. ADMA-E1 TXC-04002 Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY AND GROUND

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	22,44,66,81,84	P		**VDD:** +5 volt supply voltage, +/-5%.
GND	1,21,23,43,47	P		**Ground:** 0 volts reference
AVDD	65	P		**Analog VDD:** +5 volt power supply for the PLL, +/-5%
AGND	63	P		**Analog Ground:** Ground for the PLL

*Note: I = Input; O = Output; P = Power

UPSTREAM (A) BUS I/O

Symbol	Pin No.	I/O/P	Type *	Name/Function
UCLK	2	I	TTL	**Upstream (A) Bus Clock:** This clock operates at 19.44 MHz. Upstream (A) drop STM-1 byte data (UD7-UD0), parity (UDPAR), payload indicator (USPE), and the C1/J1 byte indicator (UC1J1) signals are clocked into the ADMA-E1 on the falling edges of this clock. This clock also derives timing for the upstream (A) add bus signals. Data (UA7-UA0), add indicator ($\overline{\text{UADD}}$), and parity (UAPAR) are clocked out of the ADMA-E1 on rising edges of this clock during the time slots corresponding to the selected TU.
UDPAR	3	I	TTL	**Upstream (A) Drop Bus Parity Bit:** Odd parity input signal representing a parity calculation for each data byte (UD7-UD0), USPE and UC1J1 signal from the bus.
UD(7-0)	4-11	I	TTL	**Upstream (A) Drop Data Byte:** Byte data corresponding to the STM-1 signal from the upstream (A) drop bus. The first bit received (dropped) corresponds to bit 7.
USPE	74	I	TTL	**Upstream (A) SPE Indicator:** A signal that is active high during each byte of the STM-1 payload. This indicator identifies the location of the VC-4 bytes.
UC1J1	83	I	TTL	**Upstream (A) C1J1 Indicator:** An active high timing signal which carries both STM-1 frame information and VC-4 phase information. The C1 pulse identifies the first C1 byte time in the STM-1 signal, and is active only when the VC-4 signal is inactive. The J1 part of the signal is active and identifies the location of J1 when VC-4 is active.
UAPAR	12	O (tristate)	TTL 4mA	**Upstream (A) Add Parity Bit:** A tristate output. Odd parity is calculated over the data byte for the time slots corresponding to a TU being added.
UA(7-0)	13-20	O (tristate)	TTL 4mA	**Upstream (A) Add Data Byte:** Tristate byte-wide output corresponding to the selected TU.
$\overline{\text{UADD}}$	82	O	TTL 4mA	**Upstream (A) Add Indicator:** An active low signal that is active only when the output data on the add bus is valid. It also identifies the location of the TU time slots being selected.

* See Input, Output and I/O Parameters section for Type definitions.

DOWNSTREAM (B) BUS I/O

Symbol	Pin No.	I/O/P	Type	Name/Function
DCLK	42	I	TTL	**Downstream (B) Bus Clock:** This clock operates at 19.44 MHz. Downstream (B) drop STM-1 byte data (DD7-DD0), parity (DDPAR), payload indicator (DSPE), and the C1/J1 byte indicator (DC1J1) signals are clocked into the ADMA-E1 on the falling edges of this clock. This clock also derives timing for the downstream (B) add bus signals. Data (DA7-DA0), add indicator ($\overline{\text{DADD}}$), and parity (DAPAR) are clocked out of the ADMA-E1 on rising edges of this clock during the time slots corresponding to the selected TU.
DDPAR	41	I	TTL	**Downstream (B) Drop Bus Parity Bit:** Odd parity input signal representing a parity calculation for each data byte (DD7-DD0), DSPE, and DC1J1 signal from the bus.
DD(7-0)	40-33	I	TTL	**Downstream (B) Drop Data Byte:** Byte data corresponding to the STM-1 signal from the downstream (B) drop bus. The first bit received (dropped) corresponds to bit 7.
DSPE	54	I	TTL	**Downstream (B) SPE Indicator:** A signal that is active high during each byte of the STM-1 payload. This indicator identifies the location of the VC-12 bytes.
DC1J1	45	I	TTL	**Downstream (B) C1J1 Indicator:** An active high timing signal which carries both STM-1 frame information and VC-4 phase information. The C1 pulse identifies the first C1 byte time in the STM-1 signal, and is active only when the VC-4 signal is inactive. The J1 part of the signal is active and identifies the location of J1 when VC-4 is active.
DAPAR	32	O (tristate)	TTL 4mA	**Downstream (B) Add Parity Bit:** A tristate output. Odd parity is calculated over the data byte for the time slots corresponding to a TU being added.
DA(7-0)	31-24	O (tristate)	TTL 4mA	**Downstream (B) Add Data Byte:** Tristate byte-wide output corresponding to the selected TU.
$\overline{\text{DADD}}$	46	O	TTL 4mA	**Downstream (B) Add Indicator:** An active low signal that is active only when the output data on the add bus is valid. It also identifies the location of the TU time slots being selected.

E1 PORT 1

Symbol	Pin No.	I/O/P	Type	Name/Function
RCO1	75	O (tristate)	TTL 4mA	**Receive Output Clock, Port 1:** A 2048 kHz clock output. Data is clocked out of the ADMA-E1 on the rising edge of RCO1. (Tristate output - output is enabled when a one is written to bit 1, register 01H.)
RPO1	77	O (tristate)	TTL 4mA	**Receive Data Positive Rail or NRZ, Port 1:** When the ADMA-E1 is operating with a positive/negative rail interface, the positive rail data is provided on this pin. When operating in the bypass mode, an NRZ signal is provided on this pin. (Tristate output - output is enabled when a one is written to bit 1, register 01H.)
RNO1	76	O (tristate)	TTL 4mA	**Receive Negative Rail, Port 1:** When the ADMA-E1 is operating with a positive/negative rail interface, the negative rail data is provided on this pin. (Tristate output - output is enabled when a one is written to bit 1, register 01H.)
TCI1	78	I	TTL	**Transmit Input Clock, Port 1:** A 2048 kHz clock (+/-50 ppm). Data is clocked into the ADMA-E1 on the falling edge of TCI1 in the normal mode. Data is clocked into the ADMA-E1 on the rising edge of TCI1 in the inverted clock mode (bit 0, register 02H).
TPI1	80	I	TTL	**Transmit Data Positive Rail or NRZ, Port 1:** When the ADMA-E1 is operating with a positive/negative rail interface, the positive rail data is provided on this pin. When operating in the bypass mode, an NRZ signal is provided on this pin.
TNI1	79	I	TTL	**Transmit Negative Rail, Port 1:** When the ADMA-E1 is operating with a positive/negative rail interface, the negative rail data is provided on this pin.

E1 PORT 2

Symbol	Pin No.	I/O/P	Type	Name/Function
RCO2	50	O (tristate)	TTL 4mA	**Receive Output Clock, Port 2:** A 2048 kHz clock output. Data is clocked out of the ADMA-E1 on the rising edge of RCO2. (Tristate output - output is enabled when a one is written to bit 0, register 01H.)
RPO2	48	O (tristate)	TTL 4mA	**Receive Data Positive Rail or NRZ, Port 2:** When the ADMA-E1 is operating with a positive/negative rail interface, the positive rail data is provided on this pin. When operating in the bypass mode, an NRZ signal is provided on this pin. (Tristate output - output is enabled when a one is written to bit 0, register 01H.)
RNO2	49	O (tristate)	TTL 4mA	**Receive Negative Rail, Port 2:** When the ADMA-E1 is operating with a positive/negative rail interface, the negative rail data is provided on this pin. (Tristate output - output is enabled when a one is written to bit 0, register 01H.)
TCI2	53	I	TTL	**Transmit Input Clock, Port 2:** A 2048 kHz clock (+/- 50 ppm). Data is clocked into the ADMA-E1 on the falling edge of TCI2 in the normal mode. Data is clocked into the ADMA-E1 on the rising edge of TCI2 in the inverted clock mode (bit 0, register 02H).
TPI2	51	I	TTL	**Transmit Data Positive Rail or NRZ, Port 2:** When the ADMA-E1 is operating with a positive/negative rail interface, the positive rail data is provided on this pin. When operating in the bypass mode, an NRZ signal is provided on this pin.
TNI2	52	I	TTL	**Transmit Negative Rail, Port 2:** When the ADMA-E1 is operating with a positive/negative rail interface, the negative rail data is provided on this pin.

MICROPROCESSOR BUS

Symbol	Pin No.	I/O/P	Type	Name/Function
A/D(0-7)	55-62	I/O	TTL 8mA	**Address/Data Bus:** These leads constitute the time multiplexed address and data bus for accessing the registers which reside in the ADMA-E1.
$\overline{SEL}$	67	I	TTL	**Select:** A low enables the microprocessor to access the ADMA-E1 memory map for control, status and alarm information.
$\overline{RD}$	68	I	TTL	**Read:** An active low signal generated by the microprocessor for reading the registers which reside in the memory map. The ADMA-E1 memory I/O is selected by placing a low on the select lead.
$\overline{WR}$	69	I	TTL	**Write:** An active low signal generated by the microprocessor for writing to the registers which reside in the memory map. The ADMA-E1 memory I/O is selected by placing a low on the select lead.
ALE	70	I	TTL	**Address Latch Enable:** An active high signal generated by the microprocessor. Used by the microprocessor to hold an address stable during a read/write bus cycle.

CONTROLS

Symbol	Pin No.	I/O/P	Type	Name/Function
TEST	71	I	TTL	**TranSwitch Test Pin:** Normally grounded.
EXTCK	72	I	TTL	**External Reference Clock:** A one written into bit 1 (EXTCLK) in register 02H enables an external 58.32 MHz TTL clock connected to this pin to be used in place of the internal phase-locked loop circuit. The clock must have a frequency stability of +/- 50 ppm and a duty cycle of 50 +/- 10%. If an external reference clock is not used, this pin must be connected to ground.
$\overline{RESET}$	73	I	TTL	**Hardware Reset:** A reset occurs when an active low pulse is applied to this pin for a minimum of 150 nanoseconds after power is applied. The reset clears all performance counters and read/write configuration registers, and initializes the internal FIFOs to start-up values.
EXTRC	64	--	Analog	**External RC Network:** A series RC network is connected to this pin when the internal phase-locked loop network is used. The resistor value is 1.2 kohm, 1/8 watt +/- 5%; and the capacitor value is 1000 +/-10% picofarads. The resistor is connected to pin 64 and the capacitor lead is connected to ground.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min*	Max*	Unit
Supply voltage	V_{DD}	-0.3	+7.0	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Continuous power dissipation	P_C		0.5	Watts
Ambient operating temperature	T_A	-40	85	^oC
Operating junction temperature	T_J		150	^oC
Storage temperature range	T_S	-55	150	^oC

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance: junction to ambient		41.6		$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}			50	mA	
P_{DD}			260	mW	Inputs switching

INPUT, OUTPUT AND I/O PARAMETERS

INPUT PARAMETERS FOR TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

OUTPUT PARAMETERS FOR TTL 4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -2.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 4.0$
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.8	6.5	9.2	ns	$C_{LOAD} = 15$ pF
t_{FALL}	1.3	2.3	3.4	ns	$C_{LOAD} = 15$ pF

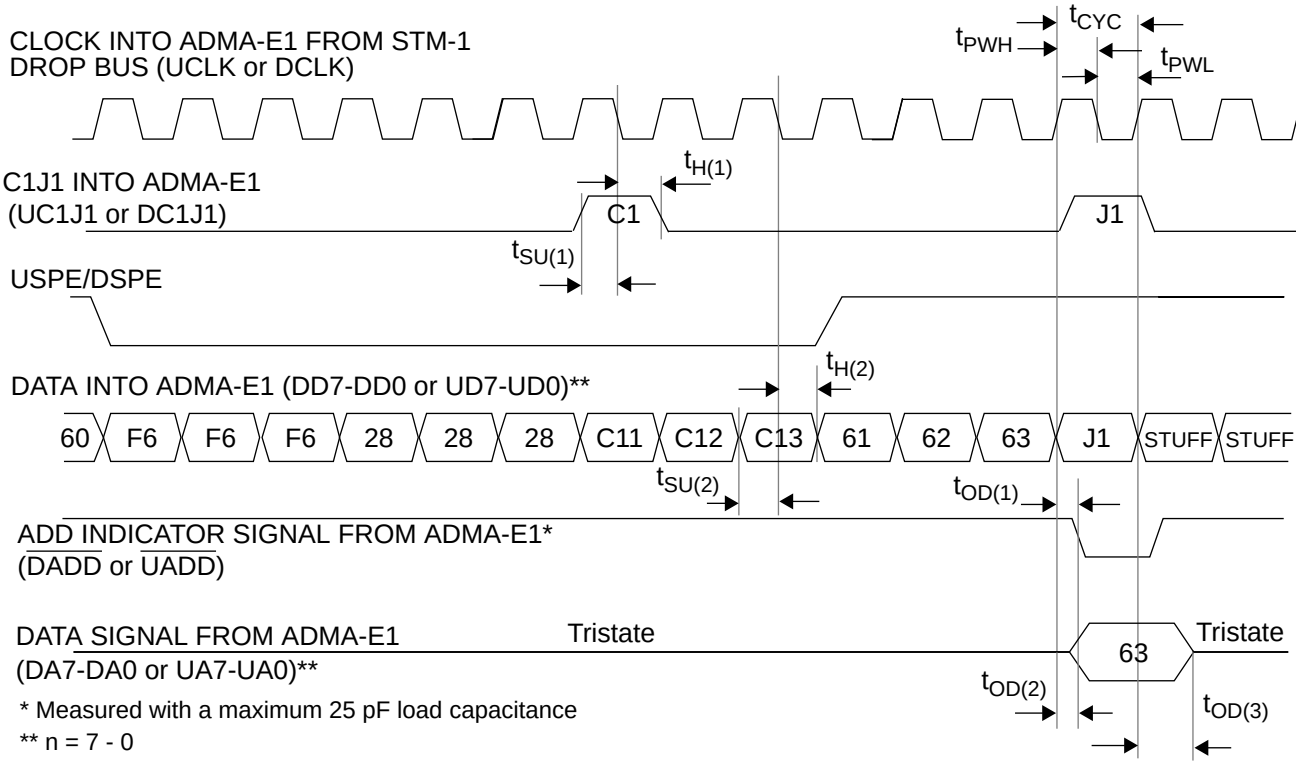
INPUT/OUTPUT PARAMETERS FOR TTL 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	mA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -4.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 8.0$
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	2.4	4.9	7.0	ns	$C_{LOAD} = 25$ pF
t_{FALL}	1.1	1.8	2.5	ns	$C_{LOAD} = 25$ pF

TIMING CHARACTERISTICS

Detailed timing diagrams for the ADMA-E1 are illustrated in Figures 5 through 9, with values of the timing intervals following each figure. All output times are measured with a maximum 75 pF load capacitance. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals and $(V_{OH} + V_{OL})/2$ for output signals.

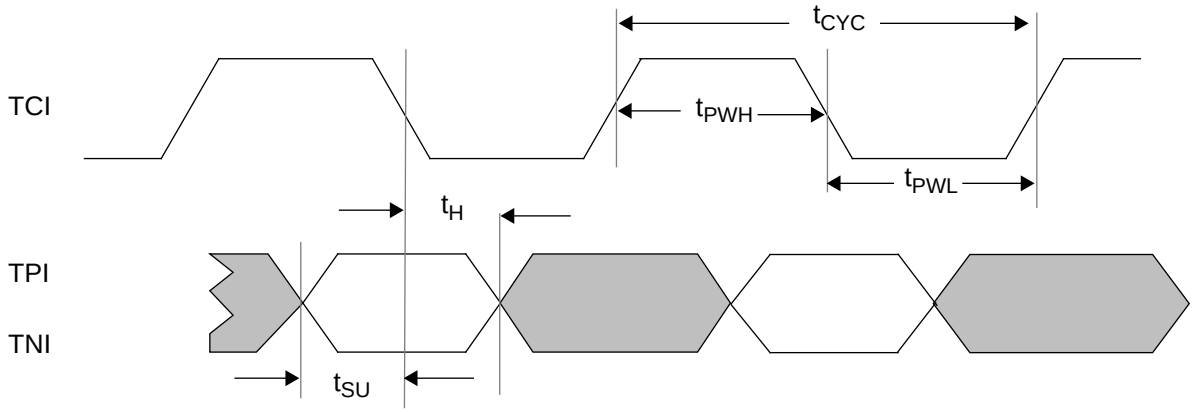
Figure 5. STM-1 I/O Timing



Parameter	Symbol	Min	Typ	Max	Unit
UCLK/DCLK clock period	t_{CYC}		51.44		ns
UCLK/DCLK high time	t_{PWH}	23			ns
UCLK/DCLK low time	t_{PWL}	23			ns
SPE and C1J1 set-up time before CLK↓	$t_{SU(1)}$	7.0			ns
SPE and C1J1 hold time after CLK↓	$t_{H(1)}$	7.0			ns
UD or DD data set-up time before CLK↓	$t_{SU(2)}$	-3.0			ns
UD or DD data hold time after CLK↓	$t_{H(2)}$	7.0			ns
$\overline{ADD}$ pulse output delay after CLK↑	$t_{OD(1)}$	7.0	10	18	ns
UA or DA data output delay (tristate to data valid) after CLK↑	$t_{OD(2)}$	12.0		33.5	ns
UA or DA data output delay (data valid to tristate) after CLK↑	$t_{OD(3)}$	7.0	13	15.5	ns

Note 1: J1 can be anywhere following C13.
Note 2: There is a one-byte delay between the drop and add bus through the ADMA-E1.

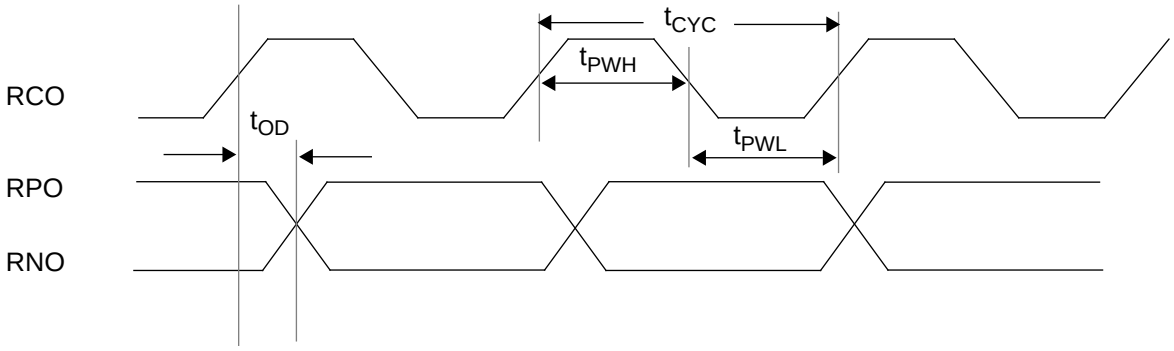
Figure 6. E1 Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
TCI clock period (Note 1)	t_{CYC}	300	488.28		ns
TCI high time	t_{PWH}	150			ns
TCI low time	t_{PWL}	150			ns
TPI/TNI set-up time before TCI↓ (Note 2)	t_{SU}	0			ns
TPI/TNI hold time after TCI↓ (Note 2)	t_H	50			ns

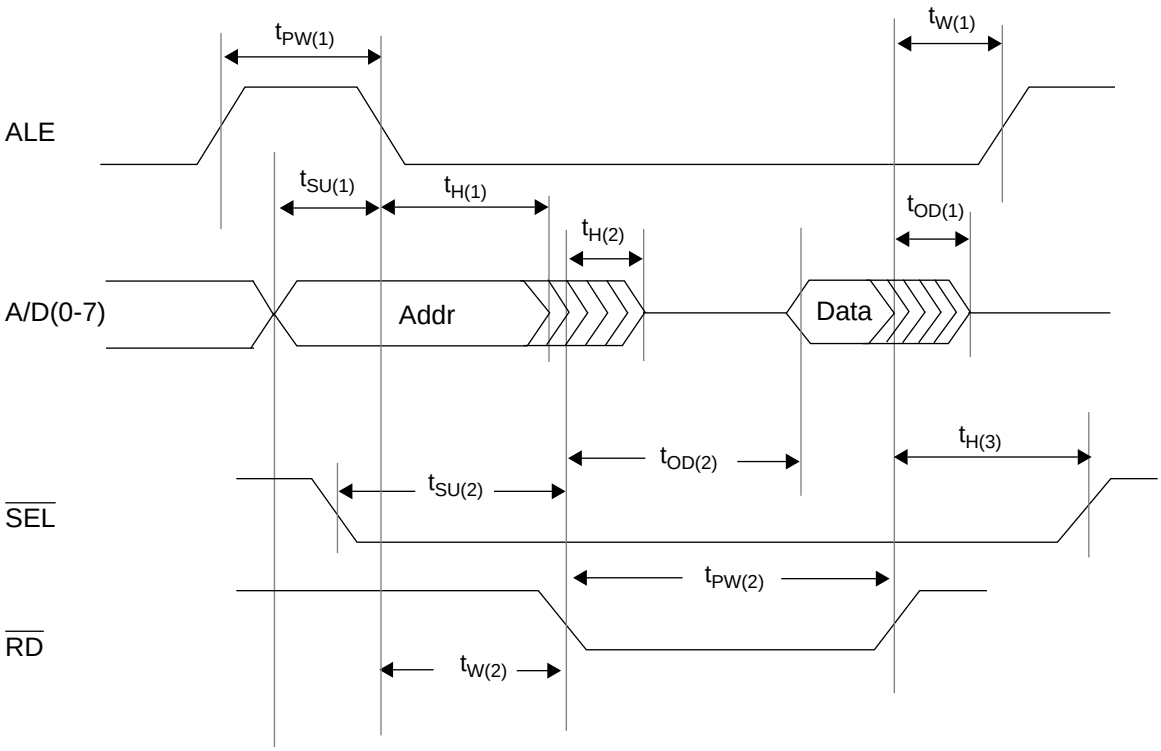
Note 1: Clock frequency for E1 signal is 2.048 MHz (+/- 50 ppm).
Note 2: When the clock is inverted in the invert E1 clock mode (bit 0, reg. 02H), set-up and hold times are the same but refer to TCI↑.

Figure 7. E1 Output Timing



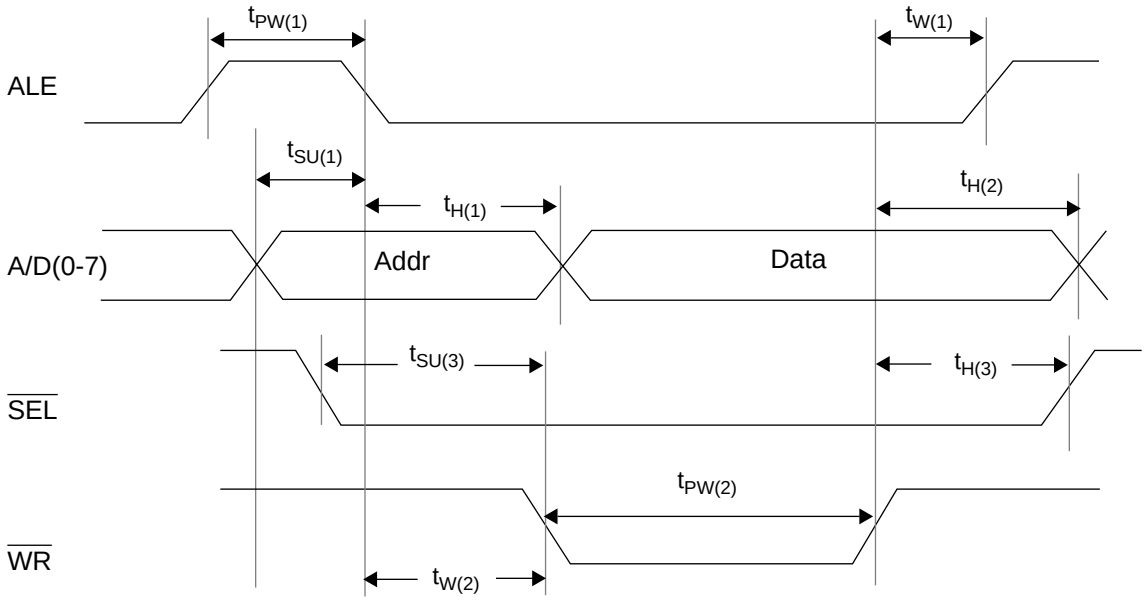
Parameter	Symbol	Min	Typ	Max	Unit
RCO clock period	t_{CYC}	480		498	ns
RCO high time	t_{PWH}	222		241	ns
RCO low time	t_{PWL}	--	257.2	--	ns
RPO/RNO output delay after RCO↑	t_{OD}	-1.5		3.9	ns

Figure 8. Microprocessor Read Cycle



Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	50			ns
ALE wait time after $\overline{RD}\uparrow$	$t_{W(1)}$	10			ns
A/D(0-7) address set-up time before ALE$\downarrow$	$t_{SU(1)}$	30			ns
A/D(0-7) address hold time after ALE$\downarrow$	$t_{H(1)}$	10			ns
A/D(0-7) address hold time after $\overline{RD}\downarrow$	$t_{H(2)}$			50	ns
A/D(0-7) data output delay after $\overline{RD}\downarrow$	$t_{OD(2)}$			200	ns
A/D(0-7) data output delay (to tristate) after $\overline{RD}\uparrow$	$t_{OD(1)}$	20		50	ns
$\overline{SEL}$ set-up time before $\overline{RD}\downarrow$	$t_{SU(2)}$	0			ns
$\overline{SEL}$ hold time after $\overline{RD}\uparrow$	$t_{H(3)}$	0			ns
$\overline{RD}$ pulse width	$t_{PW(2)}$	200			ns
$\overline{RD}$ wait time after ALE$\downarrow$	$t_{W(2)}$	50			ns

Figure 9. Microprocessor Write Cycle



Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	50			ns
ALE wait time after $\overline{WR}\uparrow$	$t_{W(1)}$	10			ns
A/D(0-7) address set-up time before ALE$\downarrow$	$t_{SU(1)}$	30			ns
A/D(0-7) address hold time after ALE$\downarrow$	$t_{H(1)}$	10			ns
A/D(0-7) data input hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	20			ns
$\overline{SEL}$ hold time after $\overline{RD}\uparrow$	$t_{H(3)}$	0			ns
$\overline{SEL}$ set-up time before $\overline{WR}\downarrow$	$t_{SU(3)}$	0			ns
$\overline{WR}$ pulse width	$t_{PW(2)}$	200			ns
$\overline{WR}$ wait time after ALE$\downarrow$	$t_{W(2)}$	50			ns

OPERATION

MODES OF OPERATION

The ADMA-E1 supports four modes of operation -- multiplexer mode, drop mode, single unidirectional ring mode, and dual unidirectional ring mode. The operating mode of each port is selected by writing the appropriate codes to P1 MODE in the 01H register and P2 MODE in the 03H register. Upstream (A) or downstream (B) bus operation for a port is selected by writing to the U/$\overline{D}$ bit located in registers 0FH (Port 1) and 2FH (Port 2).

Multiplexer Mode

For multiplexer operation, a 2048 kbit/s connection to an E1 line is made from a TU-12 in the downstream (B) (or upstream (A)) drop bus, and the return path from the E1 line is made by adding a TU-12 onto the upstream (A) (or downstream (B)) add bus. Timing for the TU-12 to be added onto the upstream (A) (or downstream (B)) add bus is derived from the upstream (A) (or downstream (B)) drop bus.

Drop Mode

In the drop mode of operation, a TU-12 is terminated from either the upstream (A) or downstream (B) bus to the 2048 kbit/s output, with no return path.

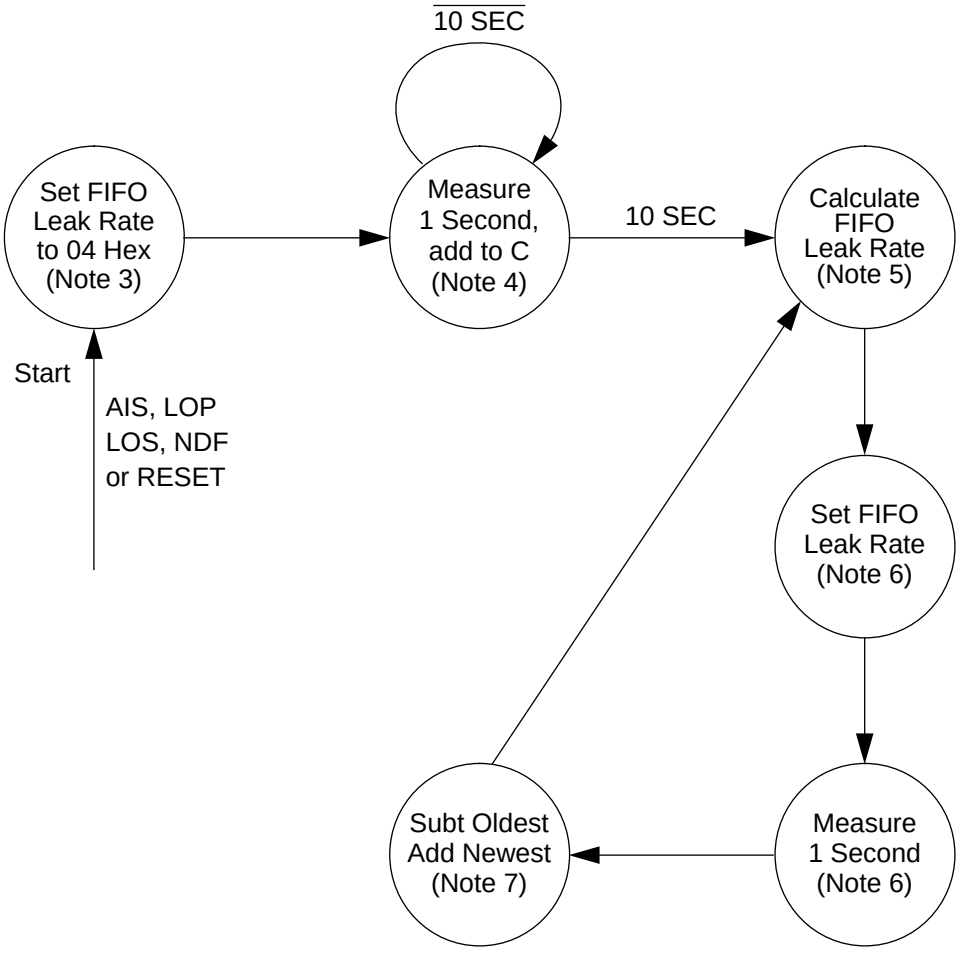
Single Unidirectional Ring Mode

In the single unidirectional ring mode of operation, a TU-12 is dropped from a downstream (B) (or upstream (A)) drop bus, and the return path for the TU-12 is to the downstream (B) (or upstream (A)) add bus. Timing for the TU-12 to be added to the downstream (B) (or upstream (A)) add bus is derived from the downstream (B) (or upstream (A)) drop bus.

Dual Unidirectional Ring Mode

In the dual unidirectional ring mode of operation, a 2048 kbit/s signal in a TU-12 is terminated from either the downstream (B) or upstream (A) drop bus, and the return path for the 2048 kbit/s signal in the TU-12 is to both the upstream (A) add and downstream (B) add bus segments. Timing for the TU-12 to be added to the downstream (B) (or upstream (A)) add bus is derived from the downstream (B) (or upstream (A)) drop bus.

POINTER LEAK RATE CALCULATIONS



Notes:

1. The procedure described in Notes 2 through 8 below must be performed independently for each of the two ports of the ADMA-E1 device.
2. The procedure shown in the diagram above uses a ten-second sliding window with a resolution of one second.
3. The initial FIFO Leak Rate Register value (in memory map address 08H or 28H) must first be set to 04 Hex.
4. Measure ten consecutive one-second samples from the Positive and Negative Stuff Counters being used. Store all ten difference values, i.e.,

   S1 = POS STUFF COUNT1 - NEG STUFF COUNT1,
   S2 = POS STUFF COUNT2 - NEG STUFF COUNT2, and so on through
   S10 = POS STUFF COUNT10 - NEG STUFF COUNT10.

   There are four pairs of stuff counters in the ADMA-E1; care should be taken to use the pair appropriate to the programmed configuration of the device. The counters are located at addresses 14H, 1CH, 34H and 3CH.
5. Calculate the leak rate (L.R.) using the following equation:

   L.R. = Hex[Int [280 / C]], where
   C = ABS [S1 + S2 + ... + S10].
   Then, if L.R. < 4, let L.R = 4,
   or if L.R. > 255, let L.R = 255.
6. Set the FIFO Leak Rate Register (address 08H or 28H) with the value between 4 and 255 calculated above, then take another one-second sample (e.g., S11).
7. Recalculate the value of 'C' by subtracting the oldest sample and adding the newest, and calculate a new leak rate, as described in Note 5 (e.g., using S2 through S11).
8. Continue to repeat the steps described in Notes 5, 6 and 7 until AIS, LOP, LOS or NDF is received or until you reset the ADMA-E1.

SOFTWARE INITIALIZATION REQUIREMENTS

The control software of the application in which the ADMA-E1 device is used should make the provisions for initialization and reset described below:

During Start-Up

Step	Action
1.	Reset ADMA-E1 device ($\overline{\text{RESET}}$, pin 73).
2.	Perform ADMA-E1 software set-up.
3.	Assign TU channels for the corresponding ports.
4.	Read the eight four-bit TU-increment and TU-decrement STUFF COUNT registers to clear them all to 0 Hex, as follows: Port 1: UD POS and UD NEG (Address 14H, Bits 7-4 and 3-0) DD POS and DD NEG (Address 1CH, Bits 7-4 and 3-0) Port 2: UD POS and UD NEG (Address 34H, Bits 7-4 and 3-0) DD POS and DD NEG (Address 3CH, Bits 7-4 and 3-0).
5.	Read the eight STUFF COUNT registers again, as in Step 4, after a time interval of between 7.5 and 30 ms.
6.	IF any STUFF COUNT register is found to contain the maximum count (F Hex), unassign the corresponding TU-channel as follows: Port 1: Write 00 Hex to Address 0F Hex. Port 2: Write 00 Hex to Address 2F Hex. THEN go to Step 3, ELSE the ADMA-E1 device is operating normally and is ready for use.

Upon Loss of Clock

Step	Action
1.	If loss of clock occurs, i.e., if UDLOC (Address 04 Hex, Bit 7) or DDLOC (Address 24 Hex, Bit 7) goes high, start from Step 4 of 'During Start-Up' above after the loss of clock condition has terminated, i.e., after the high UDLOC or DDLOC bit goes back low.

MEMORY MAP

The ADMA-E1 memory map consists of register bit positions and counters which may be accessed by a microprocessor read/write cycle. Addresses which are shown as wholly 'Unused' bytes in the memory map should not be accessed by the microprocessor. No value is specified for the content to be read from an 'Unused' bit position when the address which contains it is selected for a read cycle, but the bit position should be written as 0 when the address is selected for a write cycle (if it is a R/W address).

CONTROL

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	R/W	RESET	0	0	0	0	0	0	0
01	R/W	P1 MODE		P1BP	P2BP	P1E1LB	P2E1LB	P1E1EN	P2E1EN
02	R/W	0	0	0	0	P1TE1AIS	P2TE1AIS	EXTCLK	E1CLKI
03	R/W	0	0	0	0	0	P2 MODE		0

Note: Bits shown as 0 must be set to zero by the microprocessor during device initialization and any subsequent write cycles for the Address.

* Read/Write (R/W); Read Only (R); Read Only, Latched R(L).

UPSTREAM (A) DROP STATUS REGISTERS

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04	R(L)	UDLOC	Unused					H4ERR	PARERR
05		Unused							
06		Unused							
07		Unused							

PORT 1 STATUS/TRANSMIT REGISTERS

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08	R/W	FIFO LEAK RATE							
09	R	HDB3 CODING ERROR COUNT							
0A	R(L)	Unused					RFIFO ERR	E1 LOS	E1 AIS
0B		Unused							
0C		Unused							
0D	R/W	TAIS	GBIP2E	Unused	TFERF	TX TRACE	TX LABEL		
0E	R/W	TX "O" BITS							
0F	R/W	U/$\overline{D}$	Unused	TU NUMBER					

PORT 1 UPSTREAM (A) DROP RECEIVE REGISTERS

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10	R	UD BIP-2 ERROR COUNT							
11	R	UD FEBE COUNT							
12	R(L)	Unused				NDF	Unused		TFIFO ERR
13	R(L)	AIS	LOP	SIZE ERR	RFERF	RX TRACE	RX LABEL		
14	R	UD POS STUFF COUNT				UD NEG STUFF COUNT			
15	R(L)	RX “O” BITS							
16		Unused							
17	R	TU POINTER TEST							

PORT 1 DOWNSTREAM (B) DROP RECEIVE REGISTERS

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18	R	DD BIP-2 ERROR COUNT							
19	R	DD FEBE COUNT							
1A	R(L)	Unused				NDF	Unused		TFIFO ERR
1B	R(L)	AIS	LOP	SIZE ERR	RFERF	RX TRACE	RX LABEL		
1C	R	DD POS STUFF COUNT				DD NEG STUFF COUNT			
1D	R(L)	RX “O” BITS							
1E		Unused							
1F	R	TU POINTER TEST							

DOWNSTREAM (B) DROP STATUS REGISTERS

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
24	R(L)	DDLOC	Unused					H4ERR	PARERR
25		Unused							
26		Unused							
27		Unused							

PORT 2 STATUS/TRANSMIT REGISTERS

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
28	R/W	FIFO LEAK RATE							
29	R	HDB3 CODING ERROR COUNT							
2A	R(L)	Unused					RFIFO ERR	E1 LOS	E1 AIS
2B		Unused							
2C		Unused							
2D	R/W	TAIS	GBIP2E	Unused	TFERF	TX TRACE	TX LABEL		
2E	R/W	TX “O” BITS							
2F	R/W	U/$\overline{D}$	Unused	TU NUMBER					

PORT 2 UPSTREAM (A) DROP RECEIVE REGISTERS

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
30	R	UD BIP-2 ERROR COUNT							
31	R	UD FEBE COUNT							
32	R(L)	Unused				NDF	Unused		TFIFO ERR
33	R(L)	AIS	LOP	SIZE ERR	RFERF	RX TRACE	RX LABEL		
34	R	UD POS STUFF COUNT				UD NEG STUFF COUNT			
35	R(L)	RX “O” BITS							
36		Unused							
37	R	TU POINTER TEST							

PORT 2 DOWNSTREAM (B) DROP RECEIVE REGISTERS

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
38	R	DD BIP-2 ERROR COUNT							
39	R	DD FEBE COUNT							
3A	R(L)	Unused				NDF	Unused		TFIFO ERR
3B	R(L)	AIS	LOP	SIZE ERR	RFERF	RX TRACE	RX LABEL		
3C	R	DD POS STUFF COUNT				DD NEG STUFF COUNT			
3D	R(L)	RX “O” BITS							
3E		Unused							
3F	R	TU POINTER TEST							

MEMORY MAP DESCRIPTIONS

CONTROL REGISTERS

Address	Bit	Symbol	Description
00	7	RESET	**ADMA-E1 Software Reset:** Writing a one resets all counters and status registers to zero except the read/write configuration registers, which require a hardware reset or which must be written with value zero to clear. In addition, the internal FIFOs are initialized. This must be followed by another write cycle in which a zero is written into this location for normal operation.
01	7-6	P1 MODE	**Port 1 Mode Selection:** These bits work in conjunction with the Up/Down (U/$\overline{D}$) bit in register 0FH. The following system configuration codes are defined: Bit 7 / Bit 6 / MODE 0 / 0 / Drop Only Mode 0 / 1 / Single Unidirectional Ring Mode 1 / 0 / Multiplexer Mode 1 / 1 / Dual Unidirectional Ring Mode
	5	P1BP	**Port 1 Codec Bypass:** A one written into this location causes the Port 1 codec to be bypassed. NRZ transmit and receive data are provided on the pins labeled TPI1 and RPI1.
	4	P2BP	**Port 2 Codec Bypass:** A one written into this location causes the Port 2 codec to be bypassed. NRZ transmit and receive data are provided on the pins labeled TPI2 and RPI2.
	3	P1E1LB	**Port 1 E1 Loopback:** A one written into this location with the E1 clock invert mode turned off (reg. 02H, bit 0) causes the E1 receive data to be looped back as transmit data for Port 1. Receive data (toward the E1 line) is provided at the E1 Port 1 interface.
	2	P2E1LB	**Port 2 E1 Loopback:** A one written into this location with the E1 clock invert turned off (reg. 02H, bit 0) causes the E1 receive data to be looped back as transmit data for Port 2. Receive data (toward the E1 line) is provided at the E1 port 2 interface.
	1	P1E1EN	**Port 1 E1 Enable:** A one enables the Port 1 E1 receive output (toward the E1 line). A zero forces the receive clock and data leads to a high impedance state. However, Port 1 E1 loopback capability is operative.
	0	P2E1EN	**Port 2 E1 Enable:** A one enables the Port 2 E1 receive output (toward the E1 line). A zero forces the receive clock and data leads to a high impedance state. However, the Port 2 E1 loopback capability is operative.

Address	Bit	Symbol	Description
02	3	P1TE1AIS	**Port 1 Transmit E1 AIS:** A one written into this location causes the 2 MHz Port 1 data being transmitted to the add bus to be all ones. This function only affects the E1 data and not the Tributary Unit (e.g., pointer and V5).
	2	P2TE1AIS	**Port 2 Transmit E1 AIS:** A one written into this location causes the 2 MHz Port 2 data being transmitted to the add bus to be all ones. This function only affects the E1 data and not the Tributary Unit (e.g., pointer and V5).
	1	EXTCLK	**External Clock Enable:** A one enables an external 58.32 MHz clock, connected to the EXTCLK input pin, to be used in place of the internal phase-locked loop circuit.
	0	E1CLKI	**E1 Clock Invert:** A one causes the ADMA-E1 to accept data (E1) on the rising edge of the transmit clock instead of the falling edge as in the normal mode. When Port 1 E1 Loopback (reg. 01H, bit 3), or Port 2 E1 Loopback (reg. 01H, bit 2) is enabled, E1 clock invert must be turned off.
03	2-1	P2 MODE	**Port 2 Mode Selection:** These bits work in conjunction with the Up/Down (U/$\overline{D}$) bit in register 2FH. The following system configuration codes are defined: Bit 2 — Bit 1 — MODE 0 — 0 — Drop Only Mode 0 — 1 — Single Unidirectional Ring Mode 1 — 0 — Multiplexer Mode 1 — 1 — Dual Unidirectional Ring Mode

UPSTREAM (A) DROP STATUS REGISTERS

Address	Bit	Symbol	Description
04	7	UDLOC	**Upstream (A) Drop Loss of Clock Alarm:** Reading a one indicates the upstream (A) drop bus clock has been stuck high or low for approximately 10 or more clock cycles. This bit is latched, and is cleared on a microprocessor read cycle.
	1	H4ERR	**Upstream (A) Drop H4 Error Indication:** A one indicates that the anticipated H4 multiframe sequence of 00, 01, 10, and 11 has not been received properly. The ADMA-E1 locks to H4 after two consecutive sequences have been received properly. This bit is latched, and is cleared on a microprocessor read cycle.
	0	PARERR	**Upstream (A) Drop Parity Error:** A one indicates an upstream (A) drop parity error has been detected. The incoming parity state is compared against an internally generated parity. This bit is latched, and is cleared on a microprocessor read cycle.

PORT 1 TRANSMIT REGISTERS

Address	Bit	Symbol	Description
08	7-0	FIFO LEAK RATE	**FIFO Leak Rate Register:** A value written by the microprocessor to control the rate at which pointer movements are leaked out. The value written to this register is calculated by an external software routine to average leak rate occurrences, which is described in the Operation subsection for Pointer Leak Rate Calculations. Each unit of the value in this register represents 64 multiframes per pointer leak. Bit 7 is the MSB. Control software must initialize this register to a value of 04 Hex. The register must not be set to 00 Hex.
09	7-0	HDB3 CODING ERROR COUNT	**HDB3 Coding Error Counter:** An 8-bit saturating counter that contains the number of detected coding violations. The counter clears on a microprocessor read cycle.
0A	2	RFIFO ERR	**FIFO Error Indication:** A one indicates that the internal FIFO toward the E1 line has either overflowed or underflowed. This error indication is a latched bit, and is cleared on a microprocessor read cycle.
	1	E1 LOS	**E1 Loss of Signal:** A loss of signal occurs when the two E1 rails are both zero for more than 250 microseconds. This alarm is a latched bit, and is cleared on a microprocessor read cycle. Note: E1 LOS detection is disabled when both DDLOC and UDLOC are high.
	0	E1 AIS	**E1 Alarm Indication Signal:** A one indicates that the ADMA-E1 has detected that the incoming E1 data (toward the bus) has less than four zeros in one multiframe (500 microseconds). This alarm is a latched bit, and is cleared on a microprocessor read cycle.
0D	7	TAIS	**Transmit Alarm Indication Signal:** A one written into this location generates and sends an AIS (all ones) in the Tributary Unit (TU).
	6	GBIP2E	**Generate BIP-2 Error:** A one written into this location causes bits 1 and 2 in the transmitted path overhead (V5) byte (toward the bus) to be sent inverted from the calculated values.
	4	TFERF	**Transmit Far End Receive Failure (FERF or RDI):** A one written into this location causes a one to be transmitted (toward the bus) in bit 8 in the path overhead (V5) byte.
	3	TX TRACE	**Transmit Trace Bit:** Sets the state of bit 4 in path overhead byte (V5).
	2-0	TX LABEL	**Transmit Label:** Bits 2-0 correspond to the signal label in bits 5-7 in the path overhead (V5) byte.
0E	7-0	TX “O” BITS	**Transmit Overhead Communication Channel Bits:** Bits 3-0 correspond to bits 3-6 in the first justification control byte in the VC-12; bits 7-4 correspond to bits 3-6 in the second VC-12 justification control byte.

Address	Bit	Symbol	Description
0F	7	U/$\overline{D}$	**Upstream (A) or Downstream (B) Add Selection for Port 1:** This bit works in conjunction with the Port 1 mode control bits in reg. 01H to provide the following selections. The Tributary Unit (TU) number is selected by the code written into bits 5 through 0. REG 01H BIT / PORT 1 MODE — BIT 7 6 U/$\overline{D}$ — DROP BUS — ADD BUS Drop Only — 0 0 0 — Downstream (B) — - 0 0 1 — Upstream (A) — - Single Unidir. — 0 1 0 — Downstream (B) — Downstream (B) 0 1 1 — Upstream (A) — Upstream (A) Mux — 1 0 0 — Downstream (B) — Upstream (A) 1 0 1 — Upstream (A) — Downstream (B) Dual Unidir. — 1 1 0 — Downstream (B) — Up (B), Down (A) 1 1 1 — Upstream (A) — Up (B), Down (A)
	5-0	TU NUMBER	**Tributary Unit Number Selection for Port 1:** Binary count that corresponds to the TU selected for the TU-12 mapping into a VC-4 payload. Bit 5 4 3 2 1 0 — TU-12 MAPPING 0 0 0 0 0 0 — Idle, no TU selected 0 0 0 0 0 1 — TU 1 Col 10, 73, 136, 199 0 0 0 0 1 0 — TU 2 Col 11, 74, 137, 200 . . . . . . 1 1 1 1 1 0 — TU 62 Col 71, 134, 197, 260 1 1 1 1 1 1 — TU 63 Col 72, 135, 198, 261

PORT 1 UPSTREAM (A) DROP RECEIVE REGISTERS

Address	Bit	Symbol	Description
10	7-0	UD BIP-2 ERROR COUNT	**Receive BIP-2 Error Counter:** A saturating 8-bit binary performance counter which contains the number of BIP-2 errors detected by comparing the dropped path overhead (V5) byte BIP-2 values, bits 1 and 2, against the calculated BIP-2 value. Two errors are possible in one multiframe. The MSB bit corresponds to bit 7. The counter is cleared on a microprocessor read cycle.
11	7-0	UD FEBE COUNT	**Receive Far End Block Error (FEBE) Counter:** A saturating 8-bit binary performance counter that increments when bit 3 in the received path overhead byte (V5) is equal to one. A FEBE indication indicates the distant end has detected a BIP-2 error in the received data. The MSB bit corresponds to bit 7. The counter is cleared on a microprocessor read cycle.

Address	Bit	Symbol	Description
12	3	NDF	**New Data Flag Indication:** A one indicates a New Data Flag (NDF) has been detected in the received pointer byte (V1) in the TU. An NDF is defined as the inverse (1001) value of the normal N-bits (0110) value in bits 1 through 4 of the pointer word (V1). This is a latched bit, and is cleared on a microprocessor read cycle.
	0	TFIFO ERR	**Transmit FIFO Error:** A one indicates the transmit FIFO (toward the bus) has either overflowed or underflowed. This causes the ADMA-E1 to substitute and transmit all ones for the E1 data in the VC-12. This is a latched bit, and is cleared on a microprocessor read cycle. This alarm is not suppressed while the ADMA-E1 port is programmed for drop-only operation.
13	7	AIS	**Receive TU Alarm Indication Signal Alarm:** A one indicates that all ones have been received in the two pointer bytes (V1 and V2) for three consecutive Tributary Unit (TU) multiframes. The alarm state is exited when a pointer byte other than all ones is received. This is a latched bit, and is cleared on a microprocessor read cycle.
	6	LOP	**Receive Loss Of Pointer Alarm:** A one indicates a Loss of Pointer (LOP) has been detected. An LOP alarm occurs when eight consecutive NDFs are detected, or invalid pointers are received for eight consecutive multiframes. The LOP alarm state is exited when three consecutive TU-12 multiframes with a valid pointer are received. When AIS and LOP (bits 7 and 6) are both high, it indicates an AIS condition instead of LOP. This is a latched bit, and is cleared on a microprocessor read cycle.
	5	SIZE ERR	**TU-12 Receive Size Error Indication:** A one indicates the ADMA-E1 has detected a value other than 10 in bits 5 and 6 in the pointer byte (V1). A value of 10 designates the TU as a TU-12 (carrying a 2048 kbit/s signal). This is a latched bit, and is cleared on a microprocessor read cycle.
	4	RFERF	**Receive Far End Receive Failure Alarm:** A one indicates that the ADMA-E1 has detected a one in bit 8 in the path overhead byte (V5) for 10 consecutive multiframes. This is a latched bit, and is cleared on a microprocessor read cycle.
	3	RX TRACE	**Receive Trace Bit:** Indicates the state of bit 4 in the received path overhead byte (V5). This is a latched bit, which remains stable until set with a new value in the next multiframe.
	2-0	RX LABEL	**Receive Label:** Bits 2 through 0 correspond to the states received for the signal label in bits 5 through 7 in the path overhead (V5) byte. This is a latched field, which remains stable until set with a new value in the next multiframe.
14	7-4	UD POS. STUFF COUNT	**Upstream (A) Drop Positive Stuff Counter:** A 4-bit saturating counter that counts the TU pointer increments. Both stuff counters clear on a microprocessor read cycle.
	3-0	UD NEG. STUFF COUNT	**Upstream (A) Drop Negative Stuff Counter:** A 4-bit saturating counter that counts the TU pointer decrements. Both stuff counters clear on a microprocessor read cycle.

Address	Bit	Symbol	Description
15	7-0	RX “O” BITS	**Receive Overhead Communication Channel Bits:** Bits 3 through 0 correspond to the received states in bits 3 through 6 in the first justification control byte in VC-12; bits 7 through 4 correspond to bits 3 through 6 in the second justification control byte in VC-12. This is a latched field, which remains stable until set with a new value in the next multiframe.
17	7-0	TU POINTER TEST	**TU Pointer Value Test Register:** A test register that provides the binary value corresponding to the received pointer.

PORT 1 DOWNSTREAM (B) DROP RECEIVE REGISTERS

Address	Bit	Symbol	Description
18	7-0	DD BIP-2 ERROR COUNT	**Receive BIP-2 Error Counter:** A saturating 8-bit binary performance counter which contains the number of BIP-2 errors detected by comparing the dropped path overhead (V5) byte BIP-2 values, bits 1 and 2, against the calculated BIP-2 value. Two errors are possible in one multiframe. The MSB bit corresponds to bit 7. The counter is cleared on a microprocessor read cycle.
19	7-0	DD FEBE COUNT	**Receive Far End Block Error (FEBE) Counter:** A saturating 8-bit binary performance counter that increments when bit 3 in the received path overhead byte (V5) is equal to 1. A FEBE indication indicates the distant end has detected a BIP-2 error in the received data. The MSB bit corresponds to bit 7. The counter is cleared on a microprocessor read cycle.
1A	3	NDF	**New Data Flag Indication:** A one indicates a New Data Flag (NDF) has been detected in the received pointer byte (V1) in the TU. An NDF is defined as the inverse (1001) value of the normal N-bits (0110) value in bits 1 through 4 of the pointer word (V1). This is a latched bit, and is cleared on a microprocessor read cycle.
	0	TFIFO ERR	**Transmit FIFO Error:** A one indicates the transmit FIFO (toward the bus) has either overflowed or underflowed. This causes the ADMA-E1 to substitute and transmit all ones for the E1 data in the VC-12. This is a latched bit, and is cleared on a microprocessor read cycle. This alarm is not suppressed while the ADMA-E1 port is programmed for drop-only operation.

Address	Bit	Symbol	Description
1B	7	AIS	**Receive TU Alarm Indication Signal Alarm:** A one indicates that all ones have been received in the two pointer bytes (V1 and V2) for three consecutive Tributary Unit (TU) multiframes. The alarm state is exited when a pointer byte other than all ones is received. This is a latched bit, and is cleared on a microprocessor read cycle.
	6	LOP	**Receive Loss of Pointer Alarm:** A one indicates a Loss of Pointer (LOP) has been detected. An LOP alarm occurs when eight consecutive NDFs are detected, or invalid pointers are received for eight consecutive multiframes. The LOP alarm state is exited when three consecutive TU-12 multiframes with a valid pointer are received. When AIS and LOP (bits 7 and 6) are both high, it indicates an AIS condition instead of LOP. This is a latched bit, and is cleared on a microprocessor read cycle.
	5	SIZE ERR	**TU-12 Receive Size Error Indication:** A one indicates the ADMA-E1 has detected a value other than 10 in bits 5 and 6 in the pointer byte (V1). A value of 10 designates the Tributary Unit (TU) as a TU-12 (carrying a 2048 kbit/s signal). This is a latched bit, and is cleared on a microprocessor read cycle.
	4	RFERF	**Receive Far End Receive Failure Alarm:** A one indicates that the ADMA-E1 has detected a one in bit 8 in the path overhead byte (V5) for 10 consecutive multiframes. This is a latched bit, and is cleared on a microprocessor read cycle. This is a latched bit, and is cleared on a microprocessor read cycle.
	3	RX TRACE	**Receive Trace Bit:** Indicates the state of bit 4 in the received path overhead byte (V5). This is a latched bit, which remains stable until set with a new value in the next multiframe.
	2-0	RX LABEL	**Receive Label:** Bits 2 through 0 correspond to the states received for the signal label in bits 5 through 7 in the path overhead (V5) byte.This is a latched field, which remains stable until set with a new value in the next multiframe.
1C	7-4	DD POS. STUFF COUNT	**Downstream (B) Drop Positive Stuff Counter:** A 4-bit saturating counter that counts the TU pointer increments. Both stuff counters clear on a microprocessor read cycle.
	3-0	DD NEG. STUFF COUNT	**Downstream (B) Drop Negative Stuff Counter:** A 4-bit saturating counter that counts the TU pointer decrements. Both stuff counters clear on a microprocessor read cycle.
1D	7-0	RX “O” BITS	**Receive Overhead Communication Channel Bits:** Bits 3 through 0 correspond to the received states in bits 3 through 6 in the first justification control byte in VC-12; bits 7 through 4 correspond to bits 3 through 6 in the second justification control byte in VC-12. This is a latched field, which remains stable until set with a new value in the next multiframe.
1F	7-0	TU POINTER TEST	**TU Pointer Value Test Register:** A test register that provides the binary value corresponding to the received pointer.

DOWNSTREAM (B) DROP STATUS REGISTERS

Address	Bit	Symbol	Description
24	7	DDLOC	**Downstream (B) Drop Loss of Clock Alarm:** Reading a one indicates that the downstream (B) drop bus clock has been stuck high or low for approximately 10 or more clock cycles. This bit is latched, and is cleared on a microprocessor read cycle.
	1	H4ERR	**Downstream (B) Drop H4 Error Indication:** A one indicates that the anticipated H4 multiframe sequence of 00, 01, 10, 11 has not been received properly. The ADMA-E1 locks to H4 after two consecutive sequences have been received properly. This bit is latched, and is cleared on a microprocessor read cycle.
	0	PARERR	**Downstream (B) Drop Parity Error:** A one indicates a downstream (B) drop parity error has been detected. The incoming parity state is compared against an internally generated parity. This bit is latched, and is cleared on a microprocessor read cycle.

PORT 2 TRANSMIT REGISTERS

Address	Bit	Symbol	Description
28	7-0	FIFO LEAK RATE	**FIFO Leak Rate Register:** A value written by the microprocessor to control the rate at which pointer movements are leaked out. The value written to this register is calculated by an external software routine to average leak rate occurrences, which is described in the Operation subsection for Pointer Leak Rate Calculations. Each unit of the value in this register represents 64 multiframes per pointer leak. Bit 7 is the MSB. Control software must initialize this register to a value of 04 Hex. The register must not be set to 00 Hex.
29	7-0	HDB3 CODING ERROR COUNT	**HDB3 Coding Error Counter:** An 8-bit saturating counter that contains the number of detected coding violations. The counter clears on a microprocessor read cycle.
2A	2	RFIFO ERR	**FIFO Error Indication:** A one indicates that the internal FIFO toward the E1 line has either overflowed or underflowed. This error indication is a latched bit, and is cleared on a microprocessor read cycle.
	1	E1 LOS	**E1 Loss of Signal:** A loss of signal occurs when the two E1 rails are both zero for more than 250 microseconds. This alarm is a latched bit, and is cleared on a microprocessor read cycle. Note: E1 LOS detection is disabled when both DDLOC and UDLOC are high.
	0	E1 AIS	**E1 Alarm Indication Signal:** A one indicates that the ADMA-E1 has detected that the incoming E1 data (toward the bus) has less than four zeros in one multiframe (500 microseconds). This alarm is a latched bit, and is cleared on a microprocessor read cycle.

Address	Bit	Symbol	Description
2D	7	TAIS	**Transmit Alarm Indication Signal:** A one written into this location generates and sends an AIS (all ones) in the Tributary Unit (TU).
	6	GBIP2E	**Generate BIP-2 Error:** A one written into this location causes bits 1 and 2 in the transmitted path overhead (V5) byte (toward the bus) to be sent inverted from calculated values.
	4	TFERF	**Transmit Far End Receive Failure (FERF or RDI):** A one written into this location causes a one to be transmitted (toward the bus) in bit 8 in the path overhead (V5) byte.
	3	TX TRACE	**Transmit Trace Bit:** Sets the state of bit 4 in the path overhead byte (V5).
	2-0	TX LABEL	**Transmit Label:** Bits 2 through 0 correspond to the signal label in bits 5 through 7 in the path overhead (V5) byte.
2E	7-0	TX "O" BITS	**Transmit Overhead Communication Channel Bits:** Bits 3 through 0 correspond to bits 3 through 6 in the first justification control byte in the VC-12; bits 7 through 4 correspond to bits 3 through 6 in the second justification control byte in the VC-12.
2F	7	U/$\overline{D}$	**Upstream (A) or Downstream (B) Add Selection for Port 2:** This bit works in conjunction with the Port 2 mode control bits in reg. 03H to provide the following selections. The Tributary Unit (TU) number is selected by the code written into bits 5 through 0. REG 03H BIT / PORT 2 MODE — BIT 2 1 — U/$\overline{D}$ — DROP BUS — ADD BUS Drop Only — 0 0 — 0 — Downstream (B) — - — 0 0 — 1 — Upstream (A) — - Single Unidir. — 0 1 — 0 — Downstream (B) — Downstream (B) — 0 1 — 1 — Upstream (A) — Upstream (A) Mux — 1 0 — 0 — Downstream (B) — Upstream (A) — 1 0 — 1 — Upstream (A) — Downstream (B) Dual Unidir. — 1 1 — 0 — Downstream (B) — Up (A), Down (B) — 1 1 — 1 — Upstream (A) — Up (A), Down (B)
	5-0	TU NUMBER	**Tributary Unit (TU) Number Selection for Port 2:** Binary count that corresponds to the TU selected for the TU-12 mapping into a VC-4 payload. Bit 5 4 3 2 1 0 — TU-12 MAPPING 0 0 0 0 0 0 — Idle, no TU selected 0 0 0 0 0 1 — TU 1 Col 10, 73, 136, 199 0 0 0 0 1 0 — TU 2 Col 11, 74, 137, 200 . . . . . . 1 1 1 1 1 0 — TU 62 Col 71, 134, 197, 260 1 1 1 1 1 1 — TU 63 Col 72, 135, 198, 261

PORT 2 UPSTREAM (A) DROP RECEIVE REGISTERS

Address	Bit	Symbol	Description
30	7-0	UD BIP-2 ERROR COUNT	**Received BIP-2 Error Counter:** A saturating 8-bit binary performance counter which contains the number of BIP-2 errors detected by comparing the dropped path overhead (V5) byte BIP-2 values, bits 1 and 2, against the calculated BIP-2 value. Two errors are possible in one multiframe. The MSB bit corresponds to bit 7. The counter is cleared on a microprocessor read cycle.
31	7-0	UD FEBE COUNT	**Receive Far End Block Error (FEBE) Counter:** A saturating 8-bit binary performance counter that increments when bit 3 in the received path overhead byte (V5) is equal to one. A FEBE indication indicates the distant end has detected a BIP-2 error in the received data. The MSB bit corresponds to bit 7. The counter is cleared on a microprocessor read cycle.
32	3	NDF	**New Data Flag Indication:** A one indicates a New Data Flag (NDF) has been detected in the received pointer byte (V1) in the TU. An NDF is defined as the inverse (1001) value of the normal N-bits (0110) value in bits 1 through 4 of the pointer word (V1). This is a latched bit, and is cleared on a microprocessor read cycle.
	0	TFIFO ERR	**Transmit FIFO Error:** A one indicates the transmit FIFO (toward the bus) has either overflowed or underflowed. This causes the ADMA-E1 to substitute and transmit all ones for the E1 data in the VC-12. This is a latched bit, and is cleared on a microprocessor read cycle. This alarm is not suppressed while the ADMA-E1 port is programmed for drop-only operation.

Address	Bit	Symbol	Description
33	7	AIS	**Receive TU Alarm Indication Signal Alarm:** A one indicates that all ones have been received in the two pointer bytes (V1 and V2) for three consecutive Tributary Unit (TU) multiframes. The alarm state is exited when a pointer byte other than all ones is received. This is a latched bit, and is cleared on a microprocessor read cycle.
	6	LOP	**Receive Loss of Pointer Alarm:** A one indicates a loss of Pointer (LOP) has been detected. An LOP alarm occurs when eight consecutive NDFs are detected, or invalid pointers are received for eight consecutive multiframes. The LOP alarm state is exited when three consecutive TU-12 multiframes with valid pointers are received. When AIS and LOP (bits 7 and 6) are both high, it indicates an AIS condition instead of LOP. This is a latched bit, and is cleared on a microprocessor read cycle.
	5	SIZE ERR	**TU-12 Receive Size Error Indication:** A one indicates the ADMA-E1 has detected a value other than 10 in bits 5 and 6 in the pointer byte (V1). A value of 10 designates the TU as a TU-12 (with a 2048 kbit/s signal). This is a latched bit, and is cleared on a microprocessor read cycle.
	4	RFERF	**Receive Far End Receive Failure Alarm:** A one indicates that the ADMA-E1 has detected a one in bit 8 in the path overhead byte (V5) for 10 consecutive multiframes. This is a latched bit, and is cleared on a microprocessor read cycle.
	3	RX TRACE	**Receive Trace Bit:** Indicates the state of bit 4 in the received path overhead (V5) byte. This is a latched bit, which remains stable until set with a new value in the next multiframe.
	2-0	RX LABEL	**Receive Label:** Bits 2 through 0 correspond to the states received in the signal label in bits 5 through 7 in the path overhead (V5) byte. This is a latched field, which remains stable until set with a new value in the next multiframe.
34	7-4	UD POS. STUFF COUNT	**Upstream (A) Drop Positive Stuff Counter:** A 4-bit saturating counter that counts the TU pointer increments. Both stuff counters clear on a microprocessor read cycle.
	3-0	UD NEG. STUFF COUNT	**Upstream (A) Drop Negative Stuff Counter:** A 4-bit saturating counter that counts the TU pointer decrements. Both stuff counters clear on a microprocessor read cycle.
35	7-0	RX “O” BITS	**Receive Overhead Communication Channel Bits:** Bits 3 through 0 correspond to the received states in bits 3 through 6 in the first justification control byte in VC-12; bits 7 through 4 correspond to bits 3 through 6 in the second justification control byte in VC-12. This is a latched field, which remains stable until set with a new value in the next multiframe.
37	7-0	TU POINTER TEST	**TU Pointer Value Test Register:** A test register that provides the binary value corresponding to the received pointer.

PORT 2 DOWNSTREAM (B) DROP RECEIVE REGISTERS

Address	Bit	Symbol	Description
38	7-0	DD BIP-2 ERROR COUNT	**Received BIP-2 Error Counter:** A saturating 8-bit binary performance counter which contains the number of BIP-2 errors detected by comparing the dropped path overhead (V5) byte BIP-2 values, bits 1 and 2, against the calculated BIP-2 value. Two errors are possible in one multiframe. The MSB bit corresponds to bit 7. The counter is cleared on a microprocessor read cycle.
39	7-0	DD FEBE COUNT	**Receive Far End Block Error (FEBE) Counter:** A saturating 8-bit binary performance counter that increments when bit 3 in the received path overhead byte (V5) is equal to one. A FEBE indication indicates the distant end has detected a BIP-2 error in the received data. The MSB bit corresponds to bit 7. The counter is cleared on a microprocessor read cycle.
3A	3	NDF	**New Data Flag Indication:** A one indicates a New Data Flag (NDF) has been detected in the received pointer byte (V1) in the TU. An NDF is defined as the inverse (1001) value of the normal N-bits (0110) value in bits 1 through 4 of the pointer word (V1). This is a latched bit, and is cleared on a microprocessor read cycle.
	0	TFIFO ERR	**Transmit FIFO Error:** A one indicates the transmit FIFO (toward the bus) has either overflowed or underflowed. This causes the ADMA-E1 to substitute and transmit all ones for the E1 data in the VC-12. This is a latched bit, and is cleared on a microprocessor read cycle. This alarm is not suppressed while the ADMA-E1 port is programmed for drop-only operation.

Address	Bit	Symbol	Description
3B	7	AIS	**Receive TU Alarm Indication Signal Alarm:** A one indicates that all ones have been received in the two pointer bytes (V1 and V2) for three consecutive Tributary Unit (TU) multiframes. The alarm state is exited when a pointer byte other than all ones is received. This is a latched bit, and is cleared on a microprocessor read cycle.
	6	LOP	**Receive Loss of Pointer Alarm:** A one indicates a Loss of Pointer (LOP) has been detected. An LOP alarm occurs when eight consecutive NDFs are detected, or invalid pointers are received for eight consecutive multiframes. The LOP alarm state is exited when three consecutive TU-12 multiframes with a valid pointer are received. When AIS and LOP (bits 7 and 6) are both high, it indicates an AIS condition instead of LOP. This is a latched bit, and is cleared on a microprocessor read cycle.
	5	SIZE ERR	**TU-12 Receive Size Error Indication:** A one indicates the ADMA-E1 has detected a value other than 10 in bits 5 and 6 in the pointer byte (V1). A value of 10 designates the TU as a TU-12 (carrying a 2048 kbit/s signal). This is a latched bit, and is cleared on a microprocessor read cycle.
	4	RFERF	**Receive Far End Receive Failure Alarm:** A one indicates that the ADMA-E1 has detected a one in bit 8 in the path overhead byte (V5) for 10 consecutive multiframes. This is a latched bit, and is cleared on a microprocessor read cycle.
	3	RX TRACE	**Receive Trace Bit:** Indicates the state of bit 4 in the received path overhead byte (V5). This is a latched bit, which remains stable until set with a new value in the next multiframe.
	2-0	RX LABEL	**Receive Label:** Bits 2 through 0 correspond to the states received for the signal label in bits 5 through 7 in the path overhead (V5) byte. This is a latched field, which remains stable until set with a new value in the next multiframe.
3C	7-4	DD POS. STUFF COUNT	**Downstream (B) Drop Positive Stuff Counter:** A 4-bit saturating counter that counts the TU pointer increments. Both stuff counters clear on a microprocessor read cycle.
	3-0	DD NEG. STUFF COUNT	**Downstream (B) Drop Negative Stuff Counter:** A 4-bit saturating counter that counts the TU pointer decrements. Both stuff counters clear on a microprocessor read cycle.
3D	7-0	RX “O” BITS	**Receive Overhead Communication Channel Bits:** Bits 3 through 0 correspond to the received states in bits 3 through 6 in the first justification control byte in VC-12; bits 7 through 4 correspond to bits 3 through 6 in the second justification control byte in VC-12. This is a latched field, which remains stable until set with a new value in the next multiframe.
3F	7-0	TU POINTER TEST	**TU Pointer Value Test Register:** A test register that provides the binary value corresponding to the received pointer.

TRIBUTARY UNIT - 12 (TU-12) MAPPING

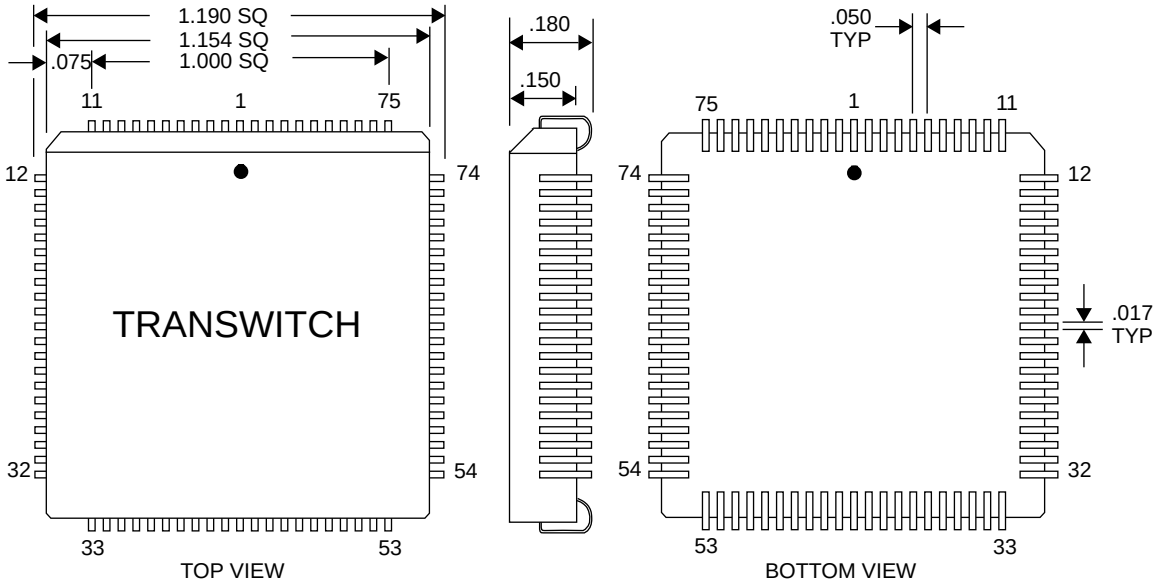
A Tributary Unit - 12 (TU-12) is mapped to and from four time slots in a Virtual Container - 4 (VC-4) based on the binary TU number written into register 0FH for Port 1 and register 2FH for Port 2, as shown in the table below.

TU	0F/2FH Registers 5	4	3	2	1	0	Column Nos.			
1	0	0	0	0	0	1	10	73	136	199
2	0	0	0	0	1	0	11	74	137	200
3	0	0	0	0	1	1	12	75	138	201
4	0	0	0	1	0	0	13	76	139	202
5	0	0	0	1	0	1	14	77	140	203
6	0	0	0	1	1	0	15	78	141	204
7	0	0	0	1	1	1	16	79	142	205
8	0	0	1	0	0	0	17	80	143	206
9	0	0	1	0	0	1	18	81	144	207
10	0	0	1	0	1	0	19	82	145	208
11	0	0	1	0	1	1	20	83	146	209
12	0	0	1	1	0	0	21	84	147	210
13	0	0	1	1	0	1	22	85	148	211
14	0	0	1	1	1	0	23	86	149	212
15	0	0	1	1	1	1	24	87	150	213
16	0	1	0	0	0	0	25	88	151	214
17	0	1	0	0	0	1	26	89	152	215
18	0	1	0	0	1	0	27	90	153	216
19	0	1	0	0	1	1	28	91	154	217
20	0	1	0	1	0	0	29	92	155	218
21	0	1	0	1	0	1	30	93	156	219
22	0	1	0	1	1	0	31	94	157	220
23	0	1	0	1	1	1	32	95	158	221
24	0	1	1	0	0	0	33	96	159	222
25	0	1	1	0	0	1	34	97	160	223
26	0	1	1	0	1	0	35	98	161	224
27	0	1	1	0	1	1	36	99	162	225
28	0	1	1	1	0	0	37	100	163	226
29	0	1	1	1	0	1	38	101	164	227
30	0	1	1	1	1	0	39	102	165	228
31	0	1	1	1	1	1	40	103	166	229
32	1	0	0	0	0	0	41	104	167	230

TU	0F/2FH Registers 5	4	3	2	1	0	Column Nos.			
33	1	0	0	0	0	1	42	105	168	231
34	1	0	0	0	1	0	43	106	169	232
35	1	0	0	0	1	1	44	107	170	233
36	1	0	0	1	0	0	45	108	171	234
37	1	0	0	1	0	1	46	109	172	235
38	1	0	0	1	1	0	47	110	173	236
39	1	0	0	1	1	1	48	111	174	237
40	1	0	1	0	0	0	49	112	175	238
41	1	0	1	0	0	1	50	113	176	239
42	1	0	1	0	1	0	51	114	177	240
43	1	0	1	0	1	1	52	115	178	241
44	1	0	1	1	0	0	53	116	179	242
45	1	0	1	1	0	1	54	117	180	243
46	1	0	1	1	1	0	55	118	181	244
47	1	0	1	1	1	1	56	119	182	245
48	1	1	0	0	0	0	57	120	183	246
49	1	1	0	0	0	1	58	121	184	247
50	1	1	0	0	1	0	59	122	185	248
51	1	1	0	0	1	1	60	123	186	249
52	1	1	0	1	0	0	61	124	187	250
53	1	1	0	1	0	1	62	125	188	251
54	1	1	0	1	1	0	63	126	189	252
55	1	1	0	1	1	1	64	127	190	253
56	1	1	1	0	0	0	65	128	191	254
57	1	1	1	0	0	1	66	129	192	255
58	1	1	1	0	1	0	67	130	193	256
59	1	1	1	0	1	1	68	131	194	257
60	1	1	1	1	0	0	69	132	195	258
61	1	1	1	1	0	1	70	133	196	259
62	1	1	1	1	1	0	71	134	197	260
63	1	1	1	1	1	1	72	135	198	261

PACKAGE INFORMATION

The ADMA-E1 is packaged in an 84-pin plastic leaded chip carrier (PLCC) suitable for socket or surface mounting, as illustrated in Figure 10.



Note: All dimensions are shown in inches and are nominal unless otherwise indicated.

Figure 10. ADMA-E1 TXC-04002 84-Pin Plastic Leaded Chip Carrier

ORDERING INFORMATION

Part Number: TXC-04002-AIPL	84-pin plastic leaded chip carrier

RELATED PRODUCTS

TXC-02302B, SYN155C VLSI Device (155 Mbit/s Synchronizer, Clock and Data Output). Provides complete STS-3/STM-1 frame synchronization on incoming 155 Mbit/s signals in a single, low power CMOS unit. This enhanced version of the SYN155 device provides a clock output in addition to the data output on the line side.

TXC-03003, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). Provides all aspects of section, line and path overhead processing for STM-1/STS-3/STS-3c 155.52 Mbit/s signals in a single chip.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator / Receiver). A Programmable multi-rate test pattern generator and receiver in a single chip with serial, nibble and byte interface capability.

TXC-21061, SOT-3/SYN155/ADMA-E1 Evaluation Board. A complete, ready-to-use single board test system that demonstrates the functions and features of the ADMA-E1, SOT-3, and SYN155 VLSI devices. Includes on-board microprocessor, RS-232 interface, and MS-DOS compatible PC software. The PC software provides full access to the ADMA-E1 and SOT-3 devices for control and monitoring.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

ITU-TSS (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (TSS)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated ADMA-E1 Data Sheet that have technical differences relative to the previous and now superseded ADMA-E1 Data Sheet:

Updated ADMA-E1 Data Sheet: Edition 3A, August 1995

Superseded ADMA-E1 Data Sheet: Edition 2, September 1992

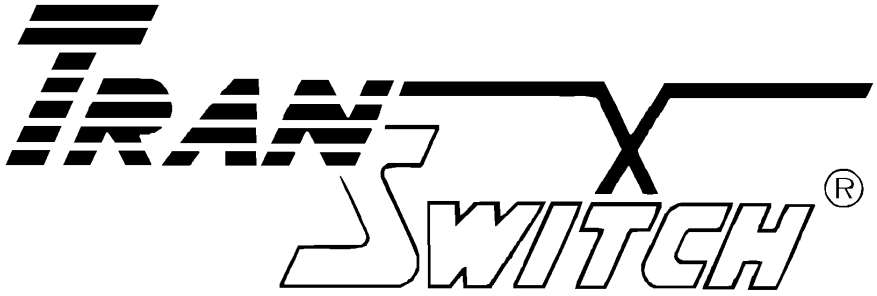
The page numbers indicated below of this updated data sheet include changes relative to the superseded data sheet.

Page Number of Updated Data Sheet	Summary of the Change
1	Changed edition number and date.
2-45	Added edition number and date. Added (A) after upstream and (B) after downstream throughout.
2	Added Table of Contents and List of Figures.
3	Made minor clarifications to Figure 1.
4	Made minor changes in first, second, fourth, fifth, seventh and eighth paragraphs.
8	Added a note to the bottom to explain Type column heading.
12	Changed clock stability in Name/Function column for EXTCK (pin 72).
13	Changed Min for Symbol T_S.
13	Added Typ to Thermal resistance: junction to ambient and deleted Thermal resistance: junction to case. Added test condition.
15	Changed introductory paragraph. Made minor clarifications to Figure 5.
16	Changed Note 1 and Min for Symbol t_H in Figure 6.
17, 18	Added $t_{H(3)}$ in Figures 8 and 9.
19	Modified the first paragraph.
20	Added Pointer Leak Rate Calculations section.
21	Added Software Initialization Requirements section.
22-24	Modified the first paragraph, the unassigned bits in the tables and the notes.
22-24	Changed Status from R to R(L) for Addresses 04H, 0AH, 12H, 13H, 15H, 1AH, 1BH, 1DH, 24H, 2AH, 32H, 33H, 35H, 3AH, 3BH and 3DH.
25	Modified Description column for Bits 7-6 (P1 MODE) and 2 (P2E1LB) of Address 01H to specify correct port number.
26	Modified Description column for Bits 3 (P1TE1AIS), 2 (P2TE1AIS), 1 (EXTCLK) and 0 (E1CLKI) of Address 02H.

Page Number of Updated Data Sheet	Summary of the Change
26	Modified Description column for Bits 2-1 (P2 MODE) of Address 03H to specify port number.
27	Modified Description column for Bits 7-0 (FIFO LEAK RATE) of Address 08H.
27	Modified Description column for Bit 1 (E1 LOS) of Address 0AH.
27	Modified Description column for Bit 4 (TFERF) of Address 0DH.
28	Modified Description column for Bit 7 (U/$\overline{D}$) of Address 0FH.
29	Modified Description column for Bit 0 (TFIFO ERR) of Address 12H.
29	Modified Description column for Bits 7 (AIS), 6 (LOP), 3 (RX TRACE) and 2-0 (RX LABEL) of Address 13H.
30	Modified Description column for Bits 7-0 (RX “O” BITS) of Address 15H.
30	Modified Description column for Bit 0 (TFIFO ERR) of Address 1AH.
31	Modified Description column for Bits 7 (AIS), 6 (LOP), 3 (RX TRACE) and 2-0 (RX LABEL) of Address 1BH.
31	Modified Description column for Bits 7-0 (RX “O” BITS) of Address 1DH.
32	Modified Description for Bits 7-0 (FIFO LEAK RATE) of Address 28H.
32	Modified Description column for Bit 1 (E1 LOS) of Address 2AH.
33	Modified Description column for Bit 4 (TFERF) of Address 2DH.
33	Modified Description column for Bit 7 (U/$\overline{D}$) of Address 2FH.
34	Modified Description column for Bit 0 (TFIFO ERR) of Address 32H.
35	Modified Description column for Bits 7 (AIS), 6 (LOP), 5 (SIZE ERR), 3 (RX TRACE) and 2-0 (RX LABEL) of Address 33H.
35	Modified Description column for Bits 7-0 (RX “O” BITS) of Address 35H.
36	Modified Description column for Bit 0 (TFIFO ERR) of Address 3AH.
37	Modified Description column for Bits 7 (AIS), 6 (LOP), 3 (RX TRACE) and 2-0 (RX LABEL) of Address 3BH.
37	Modified Description column for Bits 7-0 (RX “O” BITS) of Address 3DH.
38	Made minor changes to the introductory paragraph.
39	Modified Package Information section.
40	Modified Related Products section.
41	Added Standards Documentation Sources section.
42-43	Added List of Data Sheet Changes.

- NOTES -

- NOTES -



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DOCUMENTATION UPDATE REGISTRATION FORM

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