

DUAL J - K FLIP FLOP WITH PRESET AND CLEAR

The TC74AC112 is an advanced high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

In accordance with the logic level given J and K input this device changes state on negative going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corresponding input. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

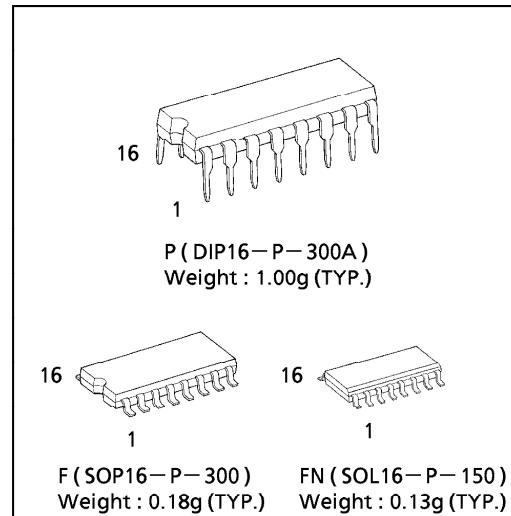
- High Speed..... $f_{MAX} = 170\text{MHz}$ (typ.) at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Symmetrical Output Impedance..... $|I_{OH}| = |I_{OL}| = 24\text{mA}(\text{Min.})$
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range.... $V_{CC} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Pin and Function Compatible with 74F112

TRUTH TABLE

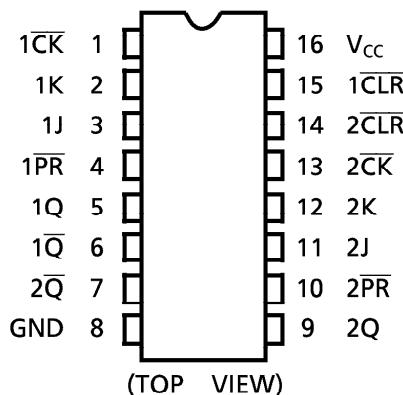
INPUTS					OUTPUTS		FUNCTION
CLR	PR	J	K	\bar{CK}	Q	\bar{Q}	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	↓	Q _n	\bar{Q}_n	NO CHANGE
H	H	L	H	↓	L	H	
H	H	H	L	↓	H	L	
H	H	H	H	↓	\bar{Q}_n	Q _n	TOGGLE
H	H	X	X	↑	Q _n	\bar{Q}_n	NO CHANGE

X : Don't Care

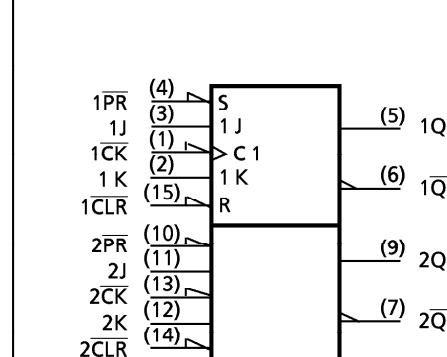
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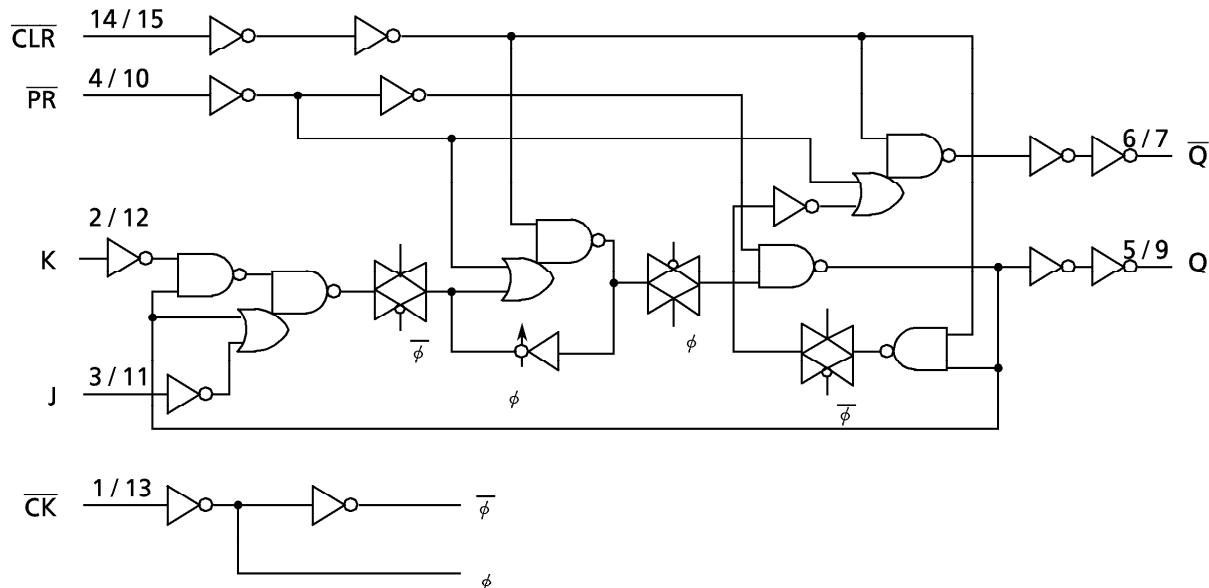
PIN ASSIGNMENT



IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 100	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{STG}	-65~150	°C

* 500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{OPR}	-40~85	°C
Input Rise and Fall Time	dt/dV	0~ 100 ($V_{CC} = 3.3 \pm 0.3\text{V}$) 0~ 20 ($V_{CC} = 5 \pm 0.5\text{V}$)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V_{IH}		2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V	
Low - Level Input Voltage	V_{IL}		2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	V	
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	V	
			$I_{OH} = -4mA$ $I_{OH} = -24mA$ $I_{OH} = -75mA^*$	3.0 4.5 5.5	2.58 3.94 —	— — —	— — —	2.48 3.80 3.85		
			$I_{OL} = 50\mu A$	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —		
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 12mA$ $I_{OL} = 24mA$ $I_{OL} = 75mA^*$	3.0 4.5 5.5	— — —	— — —	0.36 0.36 —	— — —	V	
			$I_{OL} = 12mA$ $I_{OL} = 24mA$ $I_{OL} = 75mA^*$	3.0 4.5 5.5	— — —	— — —	0.44 0.44 1.65	— — —		
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	4.0	—	40.0	

* : This spec indicates the capability of driving 50Ω transmission lines.

One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V_{CC} (V)	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (\overline{CK})	$t_W(L)$ $t_W(H)$		3.3 ± 0.3 5.0 ± 0.5	7.5 5.0	7.5 5.0	7.5 5.0	ns
Minimum Pulse Width (\overline{CLR} , \overline{PR})	$t_W(L)$		3.3 ± 0.3 5.0 ± 0.5	7.0 5.0	7.0 5.0	7.0 5.0	
Minimum Set - up Time	t_s		3.3 ± 0.3 5.0 ± 0.5	11.0 6.0	11.0 6.0	11.0 6.0	
Minimum Hold Time	t_h		3.3 ± 0.3 5.0 ± 0.5	0.0 0.0	0.0 0.0	0.0 0.0	
Minimum Removal Time (\overline{CLR} , \overline{PR})	t_{rem}		3.3 ± 0.3 5.0 ± 0.5	3.0 2.0	3.0 2.0	3.0 2.0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\Omega$, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	
Propagation Delay Time ($\overline{CK}-Q, \overline{Q}$)	t_{pLH}		3.3 ± 0.3	—	9.1	15.5	1.0	17.8
	t_{pHL}		5.0 ± 0.5	—	6.5	9.4	1.0	10.8
Propagation Delay Time ($\overline{CLR}, \overline{PR}-Q, \overline{Q}$)	t_{pLH}		3.3 ± 0.3	—	8.6	14.6	1.0	16.8
	t_{pHL}		5.0 ± 0.5	—	5.8	8.3	1.0	9.6
Maximum Clock Frequency	f_{MAX}		3.3 ± 0.3	45	90	—	45	—
			5.0 ± 0.5	80	150	—	80	—
Input Capacitance	C_{IN}			—	5	10	—	10
Power Dissipation Capacitance	$C_{PD}(1)$			—	85	—	—	—

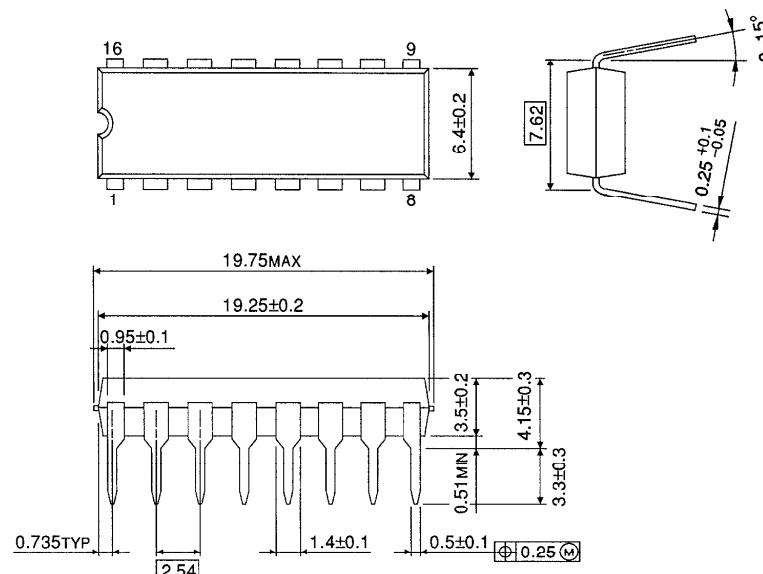
Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300A)

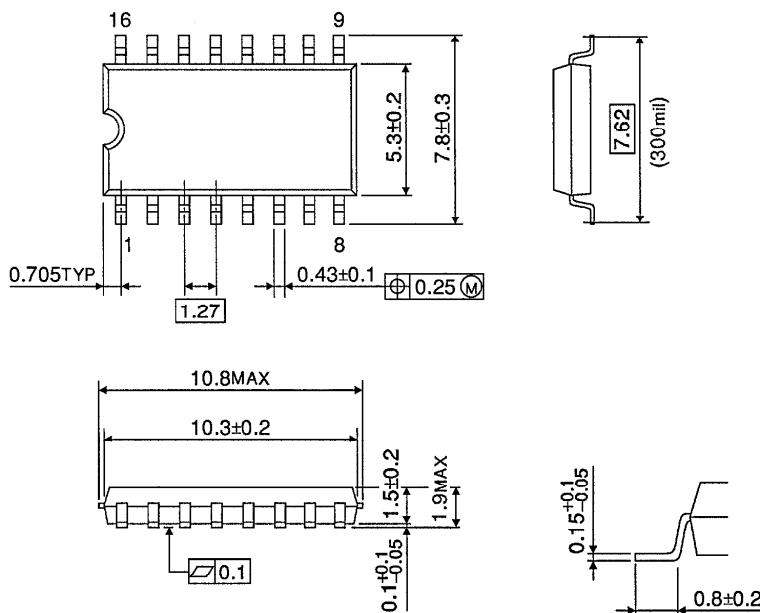
Unit in mm



Weight : 1.00g (TYP.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300)

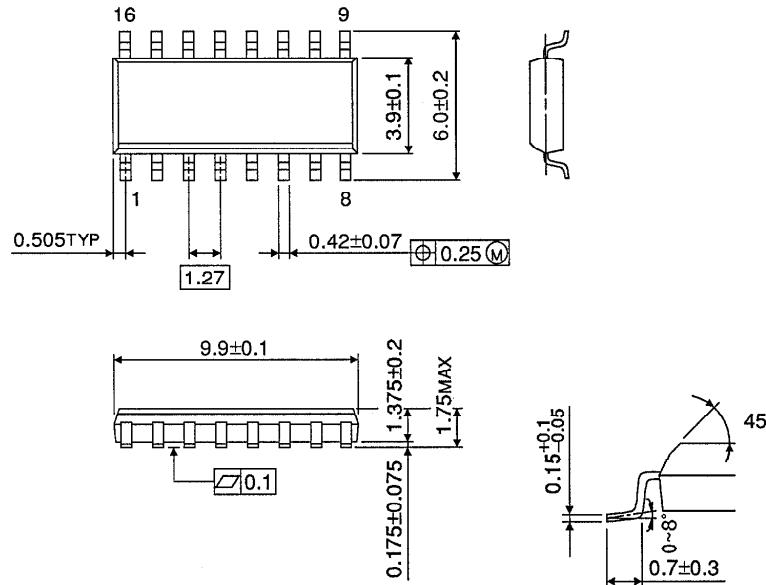
Unit in mm



Weight : 0.18g (TYP.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150)

Unit in mm



Weight: 0.13g (TYP.)