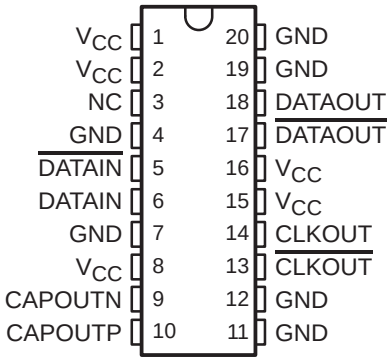
- **Recovers a 622.08-MHz Clock Signal From a 622.08-Mbit/s STS-12/STM-4 NRZ Data Stream**
- **Accepts Pseudo-ECL (PECL) Input Voltage Levels on the Input Data Stream**
- **Requires a Single 5-V Supply**
- **Provides PECL-Clock and PECL-Data Outputs**

DW PACKAGE
(TOP VIEW)



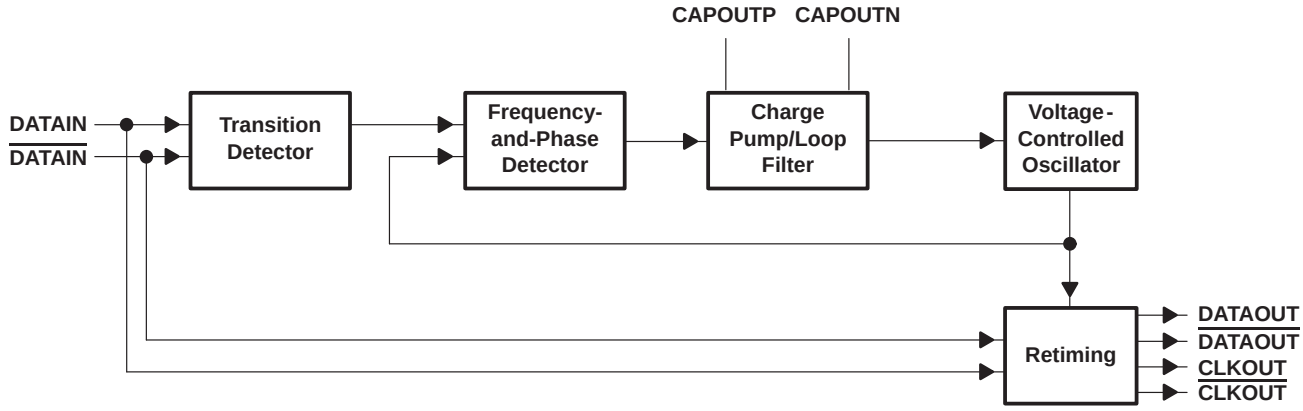
NC – No internal connection

description

The TNETA1622 recovers an embedded clock signal from a 622.08-Mbit/s STS-12/STM-4 nonreturn-to-zero (NRZ) data stream using a frequency/phase-locked loop. The device accepts PECL (ECL signals referenced to 5 V instead of GND) input-voltage levels. The recovered clock and data outputs are PECL compatible. The serial data input and recovered clock and data outputs are differential to provide maximum noise immunity.

The TNETA1622 requires only a positive 5-V supply (5 V ± 5%) for operation. The TNETA1622 is characterized for operation over a temperature range of –40°C to 85°C.

functional block diagram



PRODUCT PREVIEW

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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CAPOUTN CAPOUTP	9 10	I	Capacitor connection for phase-locked-loop filter
$\overline{\text{CLKOUT}}$ CLKOUT	13 14	O	Recovered clock output, PECL compatible
$\overline{\text{DATAIN}}$ DATAIN	5 6	I	Serial data input, PECL compatible
$\overline{\text{DATAOUT}}$ DATAOUT	17 18	O	Serial data output, PECL compatible
GND	4, 7, 11, 12, 19, 20		Ground (0-V reference)
V_{CC}	1, 2, 8, 15, 16		Supply voltage
NC	3		No connection. Leave floating (open).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, V_I, PECL . . . . . 0 V to 7 V
Power dissipation . . . . . 562 mW
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	PECL (see Note 2)	V_{CC}–1.15		V_{CC}–0.80	V
V_{IL}	Low-level input voltage	PECL (see Note 2)	V_{CC}–1.90		V_{CC}–1.50	V
T_A	Operating free-air temperature		– 40		85	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.

PRODUCT PREVIEW

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Figure 1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	DATAOUT, $\overline{\text{DATAOUT}}$	V_{CC} = 4.75 V to 5.25 V, See Notes 2 and 3	$V_{CC}-1.03$		$V_{CC}-0.85$	V
V_{OL}	Low-level output voltage	DATAOUT, $\overline{\text{DATAOUT}}$	V_{CC} = 4.75 V to 5.25 V, See Notes 2 and 3	$V_{CC}-1.85$		$V_{CC}-1.62$	V
V_{OH}	High-level output voltage	CLKOUT, $\overline{\text{CLKOUT}}$	V_{CC} = 5 V		$V_{CC}-1.0$		V
V_{OL}	Low-level output voltage	CLKOUT, $\overline{\text{CLKOUT}}$	V_{CC} = 5 V		$V_{CC}-1.6$		V
$V_{O(PP)}$	Output voltage swing, PECL	CLKOUT, $\overline{\text{CLKOUT}}$	V_{CC} = 4.75 V to 5.25 V, See Note 3	400			mV
I_{IH}	High-level input current	DATAIN, $\overline{\text{DATAIN}}$	V_{CC} = 5.25 V, V_I = 4.45 V				μA
I_{IL}	Low-level input current	DATAIN, $\overline{\text{DATAIN}}$	V_{CC} = 5.25 V, V_I = 3.35 V				μA
I_{CC}	Supply current		V_{CC} = 5.25 V, f = 622.08 Mbit/s, Outputs open			107	mA
			V_{CC} = 5.25 V, f = 622.08 Mbit/s, See Note 4			107	

NOTES: 2. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.
3. PECL outputs are terminated through a 50-Ω resistor to $V_{CC}-2$ V.
4. CLKOUT, $\overline{\text{CLKOUT}}$, DATAOUT, and $\overline{\text{DATAOUT}}$ each are terminated with a 50-Ω resistor to $V_{CC}-2$ V.

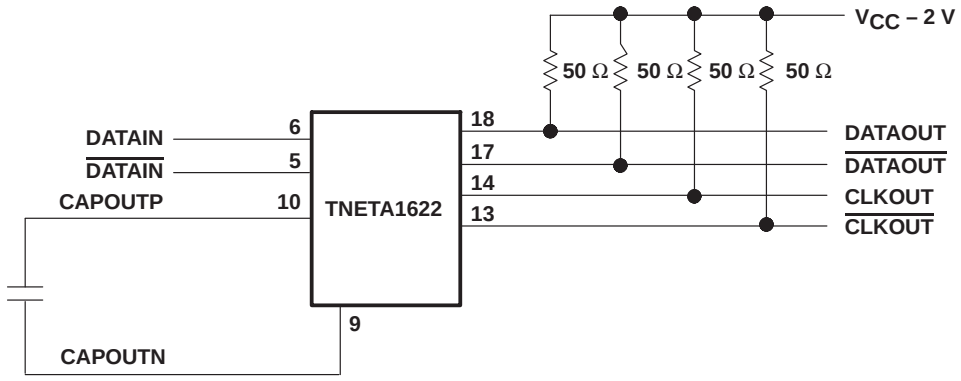
operating characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Acquisition time	See Note 5				ms
Deviation of clock-sampling point, t_{csp}	See Figure 1				ps
RMS jitter, recovered clock	See Note 6				ps
Peak-to-peak jitter, recovered clock					ps
Input data rate			622.08		Mbit/s
Duty cycle, recovered clock	See Note 3	45%		55%	
Maximum number of consecutive bits (1 or 0) in input data stream	See Note 7				

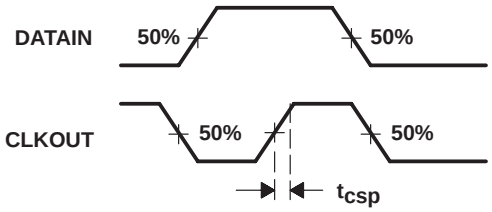
NOTES: 3. PECL outputs are terminated through a 50-Ω resistor to $V_{CC}-2$ V.
5. Acquisition time is the time required to achieve a valid clock output while applying a 2^7-1 pseudo-random bit sequence.
6. RMS jitter is measured with a $2^{31}-1$ pseudo-random bit sequence.
7. This measurement is made with a $2^{13}-1$ pseudo-random bit sequence with string substitution.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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