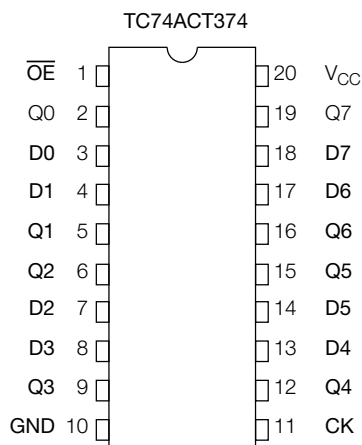


### Features:

- **High Speed:**  $f_{\text{MAX}} = 180\text{MHz}$  (typ.) at  $V_{\text{CC}} = 5\text{V}$
- **Low Power Dissipation:**  $I_{\text{CC}} = 8\mu\text{A}$  (max.) at  $T_a = 25^\circ\text{C}$
- **Compatible with TTL Outputs:**  $V_{\text{IL}} = 0.8\text{V}$  (max.);  $V_{\text{IH}} = 2.0\text{V}$  (min.)
- **Symmetrical Output Impedance:**  $I_{\text{OH}} = I_{\text{OL}} = 24\text{mA}$  (min.). Capability of driving  $50\Omega$  transmission lines.
- **Balanced Propagation Delays:**  $t_{\text{pLH}} = t_{\text{pHL}}$
- **Pin and Function Compatible with 74F374**
- **ACT374 Available in DIP, SOIC, SOP and SSOP Packages**

### Pin Assignment



The TC74ACT374 is an advanced high speed CMOS OCTAL FLIP-FLOPS with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL, while maintaining the CMOS low power dissipation.

This device may be used as a level converters for interfacing TTL or NMOS to high speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and an output enable input (OE).

When the OE input is high, the eight outputs are in a high impedance state.

The TC74ACT374 has non-inverting outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Truth Table

INPUTS			OUTPUTS
OE	CK	D	Q(374)
H	X	X	Z
L		X	Q <sub>n</sub>
L		L	L
L		H	H

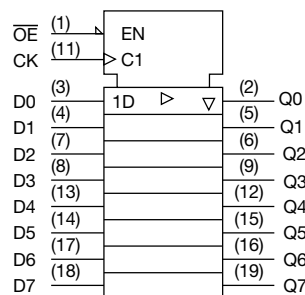
X: Don't Care

Z: High Impedance

Q<sub>n</sub> ( $\bar{Q}_n$ ): No Change

### IEC Logic Symbol

TC74ACT374



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## Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	$\pm 20$	mA
Output Diode Current	$I_{OK}$	$\pm 50$	mA
DC Output Current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 200$	mA
Power Dissipation	$P_D$	500 (DIP) */180 (SOP)	mW
Storage Temperature	$T_{stg}$	-65~150	°C
Lead Temperature 10sec	$T_L$	300	°C

\* 500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ .  
From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  
-10mW/°C should be applied up to 300mW.

## Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	4.5~5.5	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$dt/dv$	0~10	ns/v

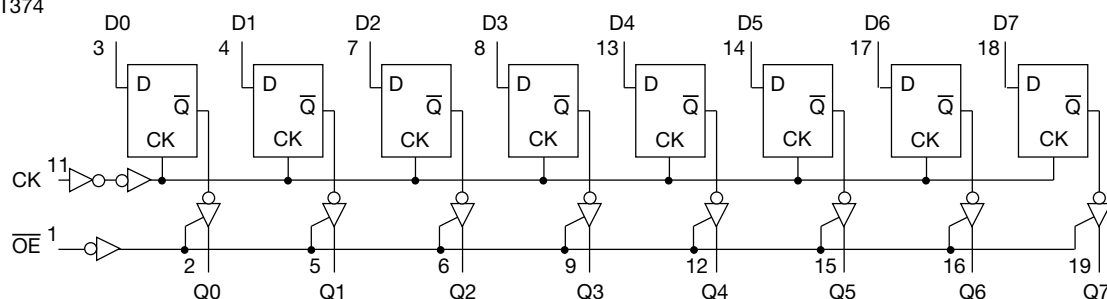
## DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT	
				Vcc	Min.	Typ.	Max.	Min.		Max.
High-Level Input Voltage	VIH	—		4.5~5.5	2.0	—	—	2.0	—	V
Low-Level Input Voltage	VIL	—		4.5~5.5	—	—	0.8	—	0.8	V
High-Level Output Voltage	VOH	VIN = VIH or VIL	IOH = -50μA	4.5	4.4	4.5	—	4.4	—	V
			IOH = -24mA	4.5	3.94	—	—	3.80	—	
			IOH = -75mA*	5.5	—	—	—	3.85	—	
Low-Level Output Voltage	VOL	VIN = VIH or VIL	IOL = 50μA	4.5	—	0.0	0.1	—	0.1	V
			IOL = 24mA	4.5	—	—	0.36	—	0.44	
			IOL = 75mA*	5.5	—	—	—	—	1.65	
3-State Output Off-State Current	IOZ	VIN = VIH or VIL VOUT = VCC or GND		5.5	—	—	±0.5	—	±5.0	μA
Input Leakage Current	IIN	VIN = VCC or GND		5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	ICC	VIN = VCC or GND		5.5	—	—	8.0	—	80.0	
	ΔICC	Per input: VCC = 3.4V Other input: VCC or GND		5.5	—	—	1.35	—	1.5	mA

\* This spec indicates the capability of driving  $50\Omega$  transmission lines.  
One output should be tested at a time for a 10ms maximum duration.

## System Diagram

TC74ACT374

Timing Requirements (Input  $t_r = t_f = 3\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	Ta=25°C		Ta= -40~85°		UNIT
			V <sub>CC</sub>	Typ.	Max.	Max.	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$	—	5.0±0.5	—	5.0	5.0	ns
Minimum Set-up Time	$t_s$	—	5.0±0.5	—	3.0	3.0	
Minimum Hold Time	$t_h$	—	5.0±0.5	—	2.0	2.0	

AC Electrical Characteristics (C<sub>L</sub> = 50pF, R<sub>L</sub> = 500Ω, Input  $t_r = t_f = 3\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C				Ta = -40~85°C		UNIT
			VCC	Min.	Typ.	Max.	Min.	Max.	
Propagation Delay Time (CK→Q, $\bar{Q}$ )	$t_{pLH}$ $t_{pHL}$	—	5.0±0.5	—	6.1	9.6	1.0	11.0	ns
Output Enable Time	$t_{pZL}$ $t_{pZH}$	—	5.0±0.5	—	6.2	10.1	1.0	11.5	
Output Disable Time	$t_{pLZ}$ $t_{pHZ}$	—	5.0±0.5	—	5.6	7.9	1.0	9.0	
Maximum Clock Frequency	f <sub>MAX</sub>	—	5.0±0.5	95	160	—	95	—	MHz
Input Capacitance	C <sub>IN</sub>	—	—	—	5	10	—	10	pF
Output Capacitance	C <sub>OUT</sub>	—	—	—	10	—	—	—	
Power Dissipation Capacitance	C <sub>PD</sub> <sup>1</sup>	—	—	—	34	—	—	—	

Note (1): C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:  $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$  (per F/F).

And the total C<sub>PD</sub> when n pcs. of Flio-Flop operate can be gained by the following equation:  $C_{PD}(total) = 22 + 12 \cdot n$ .