

OCTAL D-TYPE FLIP FLOP WITH CLEAR

The TC74ACT273 is an advanced high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the CLR input is held "L", the Q outputs are at a low logic level independent of the other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

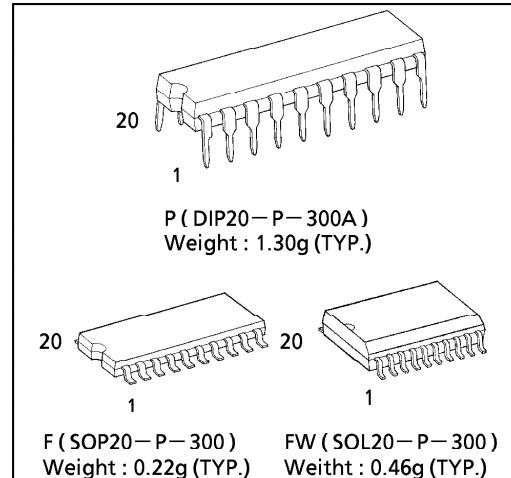
FEATURES :

- High Speed..... $f_{MAX} = 170\text{MHz}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 8\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs $V_{IL} = 0.8\text{V}(\text{Max.})$ $V_{IH} = 2.0\text{V}(\text{Min.})$
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 24\text{mA}(\text{Min.})$ Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays.... $t_{PLH} \approx t_{PHL}$
- Pin and Function Compatible with 74F273

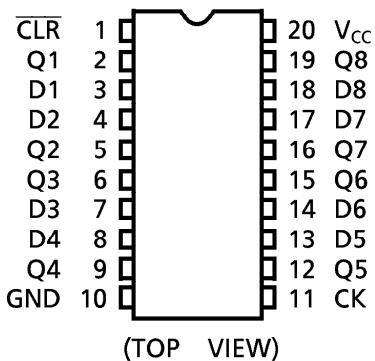
TRUTH TABLE

INPUTS			OUTPUTS		FUNCTION
CLR	D	CK	Q		
L	X	X	L		CLEAR
H	L	↑	L		—
H	H	↑	H		—
H	X	↓	Q _n		NO CHANGE

X : Don't care

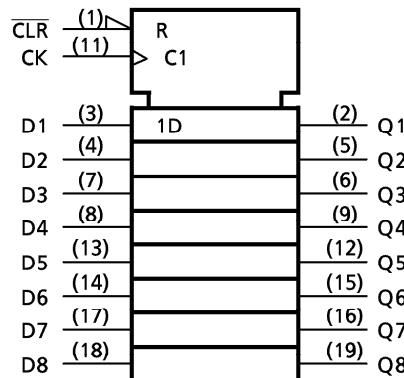


PIN ASSIGNMENT



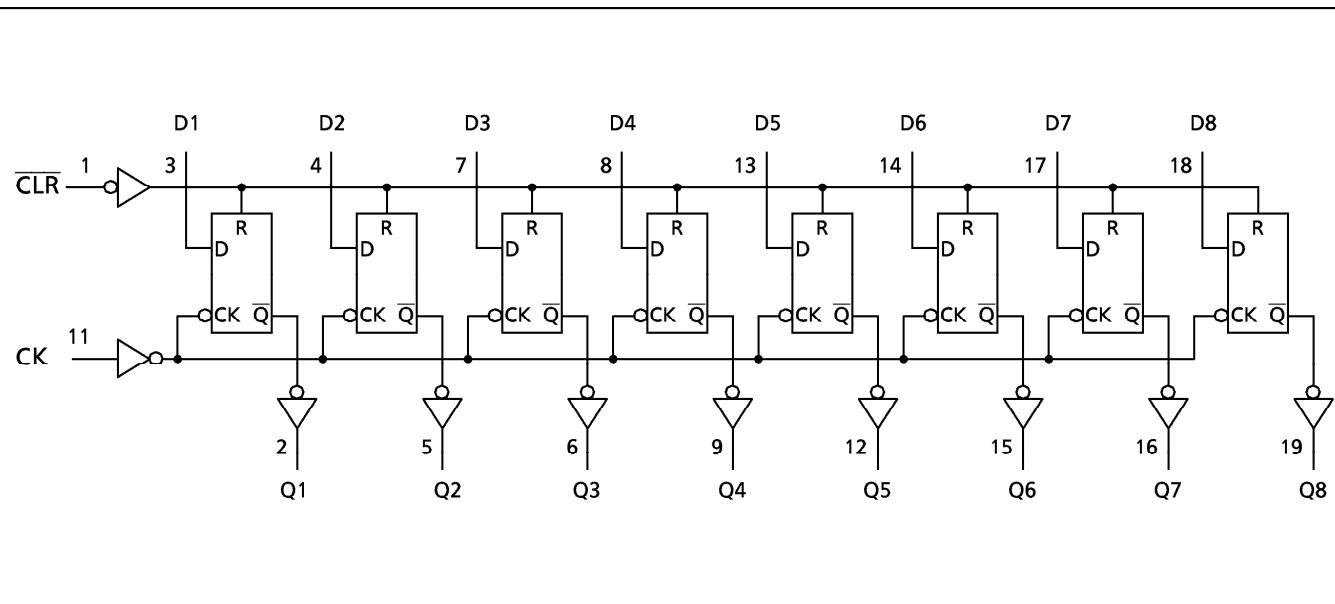
(TOP VIEW)

IEC LOGIC SYMBOL



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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt/dV	0~10	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		4.5 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}		4.5 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu A$ $I_{OH} = -24mA$ $I_{OH} = -75mA^*$	4.5 4.5 5.5	4.4 3.94 —	4.5 — —	—	4.4 3.80 3.85	— — —
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\mu A$ $I_{OL} = 24mA$ $I_{OL} = 75mA^*$	4.5 4.5 5.5	— — —	0.0 0.36 —	0.1 — —	0.1 0.44 1.65	V
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	—	± 0.1	—	± 1.0
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	8.0	—	80.0	μA
	I_C	PER INPUT : $V_{IN} = 3.4V$ OTHER INPUT : V_{CC} or GND	5.5	—	—	1.35	—	1.5	

* : This spec indicates the capability of driving 50Ω transmission lines.

One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V_{CC} (V)	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_W(L)$ $t_W(H)$		5.0 ± 0.5	5.0	5.0	5.0	ns
Minimum Pulse Width (\overline{CLR})	$t_W(L)$		5.0 ± 0.5	5.0	5.0	5.0	
Minimum Set - up Time	t_s		5.0 ± 0.5	3.5	3.5	3.5	
Minimum Hold Time	t_h		5.0 ± 0.5	1.5	1.5	1.5	
Minimum Removal Time (\overline{CLR})	t_{rem}		5.0 ± 0.5	3.0	3.0	3.0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\Omega$, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	
Propagation Delay Time (CK-Q)	t_{pLH} t_{pHL}		5.0 ± 0.5	—	6.6	10.5	1.0	12.0
Propagation Delay Time (CLR-Q)	t_{pHL}		5.0 ± 0.5	—	7.4	10.8	1.0	12.3
Maximum Clock Frequency	f _{MAX}		5.0 ± 0.5	80	150	—	80	—
Input Capacitance	C _{IN}			—	5	10	—	10
Power Dissipation Capacitance	C _{PD} (1)			—	34	—	—	—

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

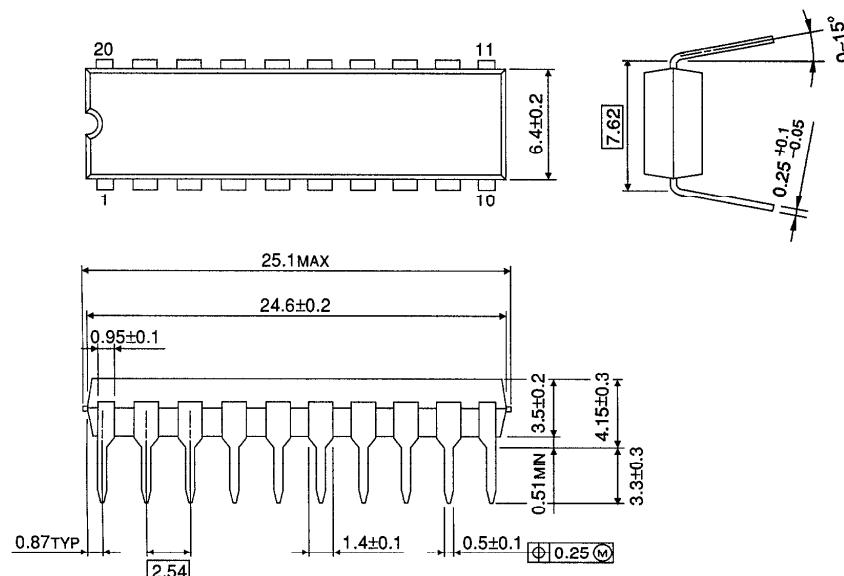
$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation :

$$C_{PD}(\text{total}) = 23 + 11 \cdot n$$

DIP 20PIN OUTLINE DRAWING (DIP20-P-300A)

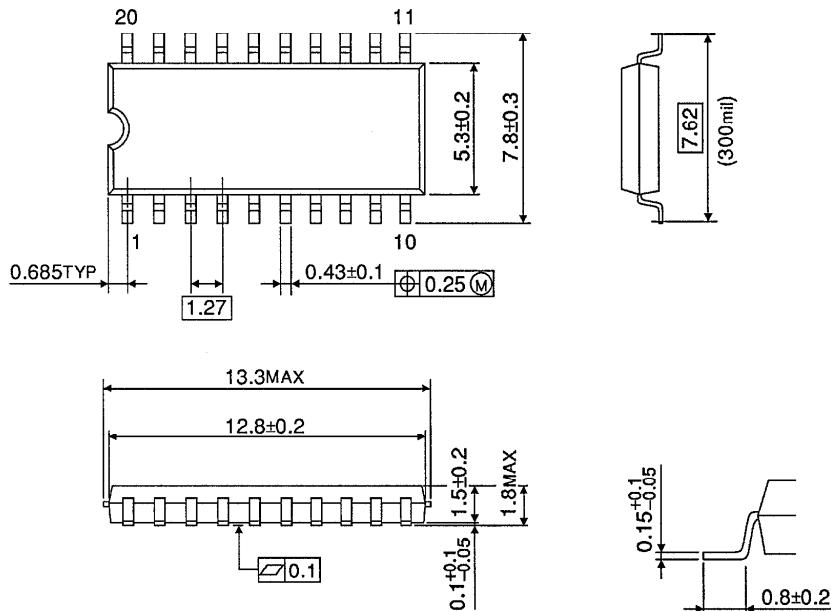
Unit in mm



Weight: 1.30g (TYP.)

SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300)

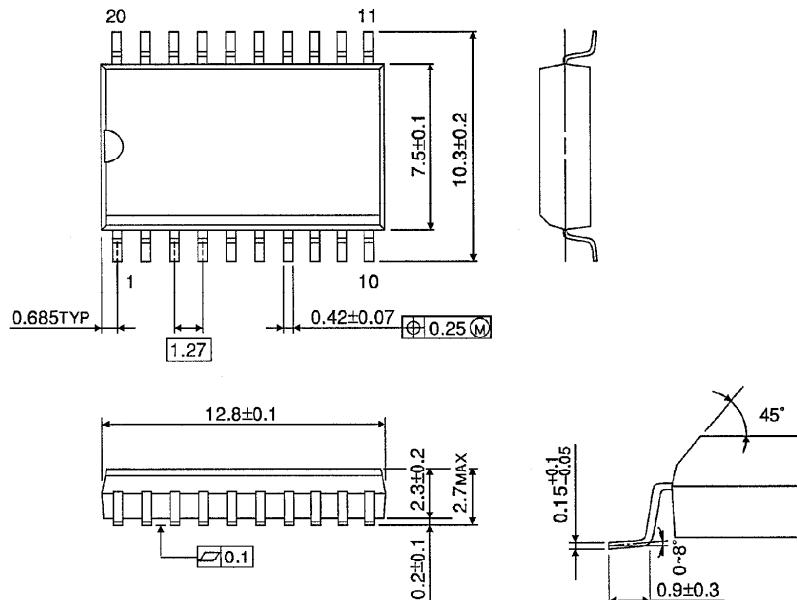
Unit in mm



Weight: 0.22g (TYP.)

SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300)

Unit in mm



Weight: 0.46g (TYP.)