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Product Brief
July 2001

TCLD0110G 10 Gbits/s Clocked Laser Driver

Features

- Internal optional data retiming latch to minimize output data pattern dependent jitter.
- 100 mA current drive capability (20 Ω load).
- Patent pending active termination output buffer to reduce power dissipation.
- Differential data and clock inputs.
- Single –5.2 V power supply.
- 25 ps rise and fall times.
- 2.0 ps rms jitter.
- Available in die form.
- Clock disable mode for data feed through.
- Laser shutdown mode.

Applications

- Optical transmitters.
- Digital video transmission.
- SONET/SDH test equipment.
- SONET/SDH OC-192/STM-64 transmission systems.
- 10.7 Gbits/s and 12.5 Gbits/s forward error correction (FEC).
- 10G Ethernet 10.3125 Gbits/s.

Functional Description

The TCLD0110G is intended to drive direct modulated lasers at speeds up to 12.5 Gbits/s. The driver consists of an input level translator and limiting amplifier, followed by a pulse-width control circuit and dual output buffers with adjustable modulation current. The TCLD0110G also contains an adjustable bias current generator that can supply up to 100 mA of laser bias current.

The two output buffers can be combined to drive up to 100 mA into a 20 Ω to 25 Ω load. Alternatively, one buffer can be used to drive up to 50 mA into a 40 Ω to 50 Ω load. In the latter case, the unused output buffer is disabled to save power.

Each output buffer provides an active 50 Ω back termination that can absorb reflections and thus minimize jitter and overshoot. An internal operational amplifier is used to track the voltage drop across the laser and to allow dc coupling to the laser without excess loading of the laser bias circuit.

On-die sense resistors allow monitoring of both modulation and bias currents and can be employed as part of an external control loop.

For applications using an unregualted power supply, a connection is avaliable for an external 2.5 V shunt voltage reference used to stabilize operation overtemperature and power supply voltage range.

A selectable internal data retiming latch is integrated into this device. When an input clock is available, the internal latch can be used to eliminate pattern-dependent jitter on the data input. If no clock is available, the latch is disabled and the input signal bypasses this circuit.

Functional Diagram

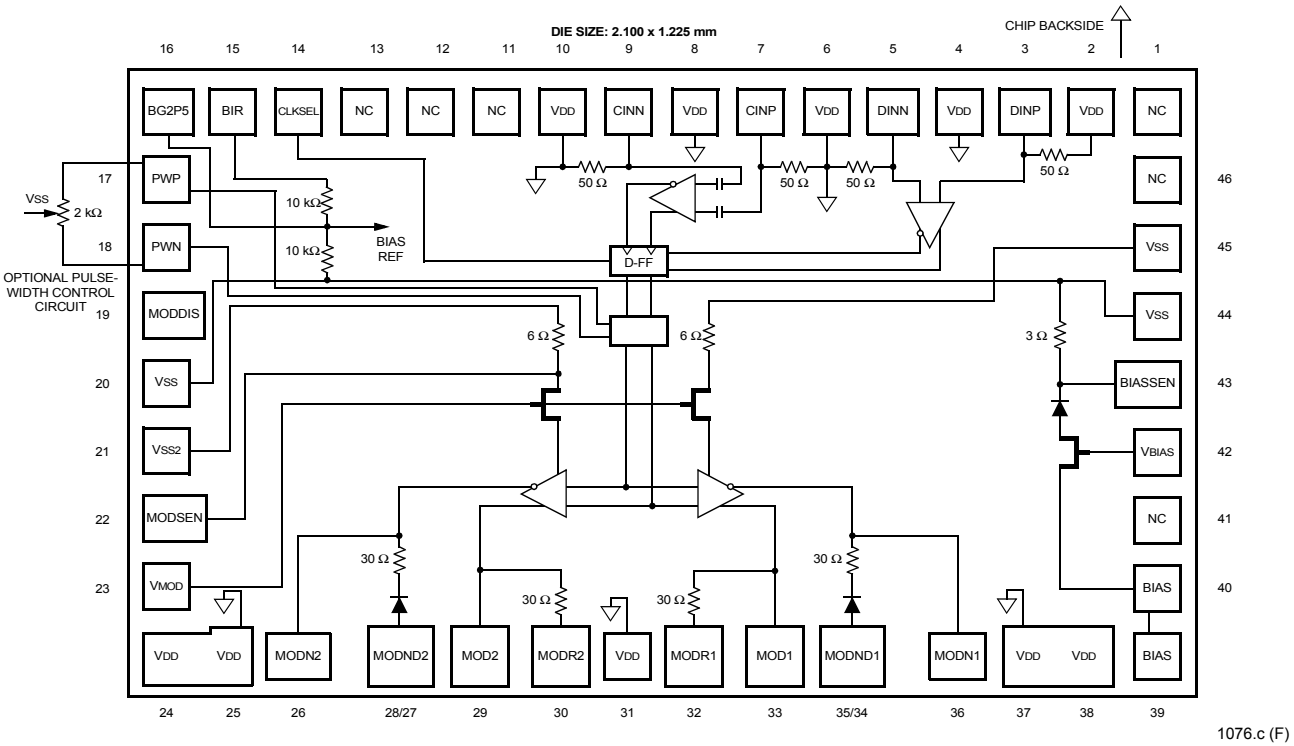

Figure 1. TCLD Die Functional Diagram and Pad Configuration

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