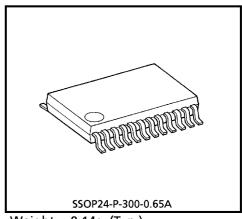
TOSHIBA TC74LCX652FS

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74LCX652FS

LOW VOLTAGE OCTAL BUS TRANSCEIVER / REGISTER WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX652 is a high parformance CMOS OCTAL BUS TRANSCEIVER/REGISTER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. This device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs. This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. All inputs are equipped with protection circuits against static discharge.



Weight: 0.14g (Typ.)

FEATURES

Low voltage operation : $V_{CC} = 2.0 \sim 3.6V$

High speed operation : $t_{pd} = 7.0$ ns (Max.) ($V_{CC} = 3.0 \sim 3.6$ V) Output current : $|I_{OH}|/I_{OL} = 24mA$ (Min.) ($V_{CC} = 3.0V$)

Latch-up performance : ± 500mA

Available in SSOP.

Bidirectional interface between 5V and 3.3V signals.

Power down protection is provided on all inputs and outputs.

Pin and function compatible with the 74 series (74AC/F/ALS/LS etc.) 652 type.

(Note) Do not apply a signal to any bus terminal when it is in the output mode. Damage may

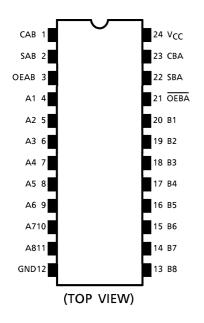
All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

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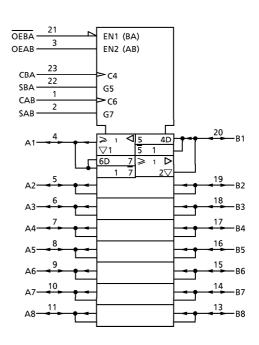
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PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

	CC	ONTRO	L INPU	ΓS		BUS		FUNCTION
OEAB	OEBA	CAB	CBA	SAB	SBA	Α	В	FUNCTION
	L H	V*	X*	Х	х	INPUT	INPUT	The output functions of A and B Busses are
		^	^	^		Z	Z	disabled.
L								Both A and B Busses are used as inputs to
				X	Х	X	X	the internal flip-flops. Data on the Bus will
						INDUT	CUEDUE	be stored on the rising edge of the Clock.
		X*	Х*		Х	INPUT L	OUTPUT	The data on the A bus are displayed on the
		Χ"	Χ"	L	X	H	H	B bus.
								The data on the A bus are displayed on the
		_	X*	L	Х	L	L	B Bus, and are stored into the A storage
Н	н		χ		X	Н	Н	flip-flops on the rising edge of CAB.
''		Х*	Х*	H	Х	х	Qn	The data in the A storage flop-flops are
							————	displayed on the B Bus.
			X*	н	х	L	L	The data on the A Bus are stored into the
								A storage flip-flops on the rising edge of CAB, and the stored data propagate directly
						Н	н	onto the B Bus.
			X*	х	L	OUTPUT	INPUT	The data on the D. Due are displayed on the
		X*				L	L	The data on the B Bus are displayed on the A bus.
						Н Н		A bus.
		X*		х		L	L	The data on the B Bus are displayed on the
					L	Н	Н	A Bus, and are stored into the B storage
L	L					''	''	flip-flops on the rising edge of CBA.
		X*	Х*	Х	Н	Qn X		The data in the B storage flip-flops are displayed on the A Bus.
							_	The data on the B Bus are stored into the
		V.±	(*	x	н	L	L	B storage flip-flops on the rising edge of
		X*				Н	Н	CBA, and the stored data propagate directly
								onto the A Bus.
			* X*	н	Н	OUTPUT	OUTPUT	The data in the A storage flop-flops are
Н	L	X*				Qn	Qn	displayed on the B Bus, and the data in the
								B storage flop-flops are displayed on the A.

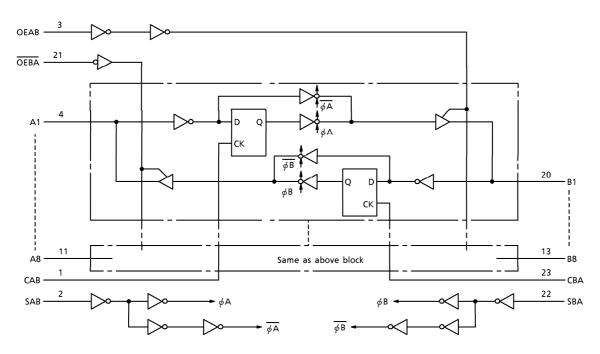
X : Don't care

Z : High Impedance

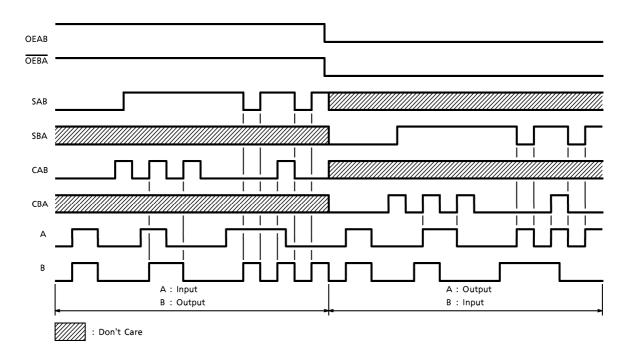
Qn : The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

* The clocks are not internally gated with either OEAB or OEBA. Therefore, data on the A and / or B Busses may be clocked into the storage flip-flops at any time.

SYSTEM DIAGRAM



TIMING CHART



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	Vcc	-0.5~7.0	V
DC Input Voltage (CAB, CBA, SAB, SBA, OEAB, OEBA)	VIN	- 0.5~7.0	V
DC Bus I/O Voltage	V _{I/O}	-0.5~7.0 (Note 1) -0.5~V _{CC} +0.5 (Note 2)	V
Input Diode Current	Ικ	– 50	mA
Output Diode Current	loк	± 50 (Note 3)	mA
DC Output Current	IOUT	± 50	mA
Power Dissipation	PD	180	mW
DC V _{CC} /Ground Current	ICC / IGND	± 100	mA
Storage Temperature	T _{stg}	−65~150	°C

(Note 1) Off-State

(Note 2) High or Low State. IOUT absolute maximum rating must be observed.

(Note 3) V_{OUT}<GND, V_{OUT}>V_{CC}

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT	
Supply Voltage	V	2.0~3.6	V	
Supply Voltage	VCC	1.5~3.6 (Note 4)	, v	
Input Voltage (CAB, CBA, SAB, SBA, OEAB, OEBA)	VIN	0~5.5	>	
Bus I/O Voltage	\/	0~5.5 (Note 5)	V	
Bus 170 Voltage	V _I /O	0~ V _{CC} (Note 6)	V	
Output Current	la/la.	± 24 (Note 7)	mA	
Output Current	IOH/IOL	± 12 (Note 8)		
Operating Temperature	T _{opr}	- 40∼85	°C	
Input Rise And Fall Time	dt/dv	0~10 (Note 9)	ns / V	

(Note 4) Data Retention Only.

(Note 5) Off-State

(Note 6) High or Low State.

(Note 7) $V_{CC} = 3.0 \sim 3.6V$ (Note 8) $V_{CC} = 2.7 \sim 3.0V$

(Note 9) $V_{IN} = 0.8 \sim 2.0 \text{V}$, $V_{CC} = 3.0 \text{V}$

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = $-40 \sim 85$ °C)

PARAMETER		SYMBOL	TEST CON	TEST CONDITION		MIN.	MAX.	UNIT
Input	"H" Level	V_{IH}				2.0	_	V
Voltage	"L" Level	V _{IL}			2.7~3.6	_	0.8	V
				I _{OH} = -100μA	2.7~3.6	V _{CC} - 0.2	_	
	"H" Level	VOH	VIN = VIH or VIL	$I_{OH} = -12mA$	2.7	2.2	_	
044				I _{OH} = - 18mA	3.0	2.4	_	V
Output				$I_{OH} = -24mA$	3.0	2.2	_	
Voltage	"L" Level	VoL	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100μA	2.7~3.6	_	0.2	
				I _{OL} = 12mA	2.7	_	0.4	
				I _{OL} = 16mA	3.0	_	0.4	
				I _{OL} = 24mA	3.0	_	0.55	
Input Leaka	ge Current	IN	V _{IN} = 0~5.5V		2.7~3.6	_	± 5.0	μΑ
	3-State Output Off-State Current		$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0 \sim 5.5V$		2.7~3.6	_	± 5.0	μ A
Power Off Leakage Current		l _{OFF}	V _{IN} / V _{OUT} = 5.5V		0		10.0	μΑ
Quiescent Supply		Land	V _{IN} = V _{CC} or GND		2.7~3.6	_	10.0	
Current		lcc	$V_{IN} / V_{OUT} = 3.6 \sim 5.$	5V	2.7~3.6	_	± 10.0	
Increase In I _{CC} Per Input		ΔΙCC	V _{IH} = V _{CC} - 0.6V		2.7~3.6		500	μΑ

AC characteristic ($Ta = -40 \sim 85$ °C)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	MIN.	MAX.	UNIT
Maximum Clock Frequency	fMAX	(Fig.1, 2)	2.7 3.3 ± 0.3	— 150		MHz
Propagation Delay Time (An, Bn-Bn, An)	t _{pLH}	(Fig.1, 2)	2.7 3.3 ± 0.3	— 1.5	8.0 7.0	ns
Propagation Delay Time	t _{pLH}	(Fig.1, 5)	2.7	_	9.5	ns
(CAB, CBA-Bn, An)	t _{pHL}	(1.3.1)	3.3 ± 0.3	1.5	8.5	
Propagation Delay Time	t _{pLH}	t _{pLH} (Fig.1, 2)	2.7	_	9.5	nc
(SAB, SBA-Bn, An)			3.3 ± 0.3	1.5	8.5	ns
Output Enable Time	t _{pZL}	(Fig.1, 3, 4)	2.7	_	9.5	ns
(OEAB, OEBA-An, Bn)	t _p ZH	(11g.17 37 ¬)	3.3 ± 0.3	1.5	8.5	113
Output Disable Time	t _{pLZ}	^t pLZ (Fig.1, 3, 4)	2.7	_	9.5	ns
(OEAB, OEBA-An, Bn)	t _{pHZ}	(Fig. 1, 3, 4)	3.3 ± 0.3	1.5	8.5	115
Minimum Pulse Width	t _W (H) t _W (L)	/F' - 4 - F\	2.7	3.3	_	ns
Iviiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiii		(Fig.1, 5)	3.3 ± 0.3	3.3	_	
Minimum Cat up Time		/F: 4 F)	2.7	2.5	_	
Minimum Set-up Time	t _s	(Fig.1, 5)	3.3 ± 0.3	2.5	_	ns
Minimum Hold Time	4.	/F:- 1 F)	2.7	1.5	_	nc
Minimum Hold Time	^t h	(Fig.1, 5)	3.3 ± 0.3	1.5	_	ns
Output To Output	t _{osLH}	/Ninto 10\	2.7	_	_	ns
Skew	t _{osHL}	(Note 10)	3.3 ± 0.3	_	1.0	ns

(Note 10) Parameter guaranteed by design. $(t_{OSLH} = |t_{pLHm} - t_{pLHn}|, \ t_{OSHL} = |t_{pHLm} - t_{pHLn}|)$

DYNAMIC SWITCHING CHARACTERISTICS (Ta = 25°C, Input $t_f = t_f = 2.5$ ns, $C_L = 50$ pF, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	$V_{IH} = 3.3V$, $V_{IL} = 0V$ (Note 11)	3.3	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OL} V	$V_{IH} = 3.3V$, $V_{IL} = 0V$ (Note 11)	3.3	0.8	V

(Note 11) Characterized with 7 outputs switching from High-to-Low or Low-to- High. The remaining output is measured in the Low state.

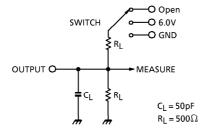
CAPACITIVE CHARACTERISTICS (Ta = 25°C)

PARAMETER SYMBOL		TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Input Capacitance C _{IN}		OEAB, OEBA, CAB, CBA, SAB, SBA	3.3 ± 0.3	7	pF
Bus Input Capacitance C _{I/O}		An, Bn	3.3 ± 0.3	8	рF
Power Dissipation Capacitance	C _{PD}	f _{IN} = 10MHz (Note 12)	3.3 ± 0.3	25	pF

(Note 12) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation : I_{CC} (opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$ (per bit)

TEST CIRCUIT

Fig.1



PARAMETER	SWITCH
t _{pLH} , t _{pHL}	Open
t _{pLZ} , t _{pZL}	6.0V
^t pHZ ^{, t} pZH	GND
tw, ts, th, fMAX	Open

AC WAVEFORM

Fig.2 t_{pLH}, t_{pHL}

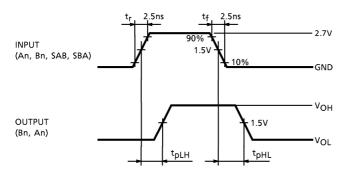


Fig.3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

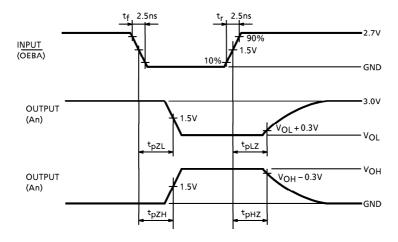


Fig.4 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

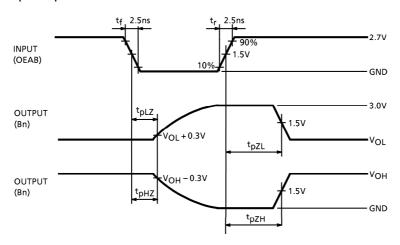
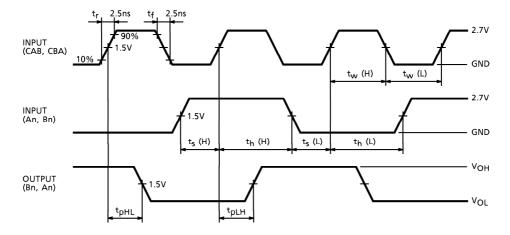
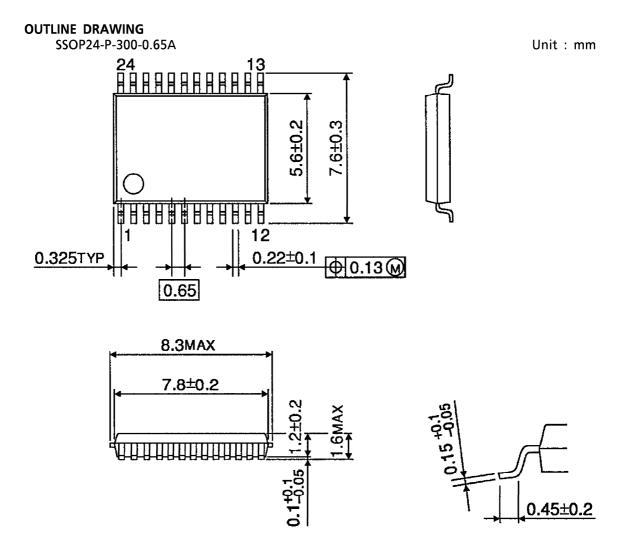


Fig.5 t_{pLH} , t_{pHL} , t_{w} , t_{s} , t_{h}





Weight: 0.14g (Typ.)