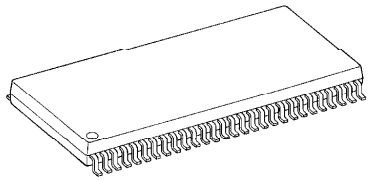
ADVANCE INFORMATION

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCX16823FT

LOW-VOLTAGE 18-BIT D-TYPE FLIP-FLOP WITH 3.6V TOLERANT INPUTS AND OUTPUTS

The TC74VCX16823FT is a high performance CMOS 18-bit D-TYPE FLIP-FLOP. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
It is also designed with over voltage tolerant inputs and outputs up to 3.6V.
The TC74VCX16823FT can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ($\overline{CKEN}$) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CKEN}$ high disables the clock buffer, thus latching the outputs. Taking the clear ($\overline{CLR}$) input low causes the Q outputs to go low independently of the clock.
When the $\overline{OE}$ input is high, the outputs are in a high impedance state. This device is designed to be used with 3 – state memory address drivers, etc.
All inputs are equipped with protection circuits against static discharge.



TSSOP56-P-0061-0.50

Weight : 0.25g (Typ.)

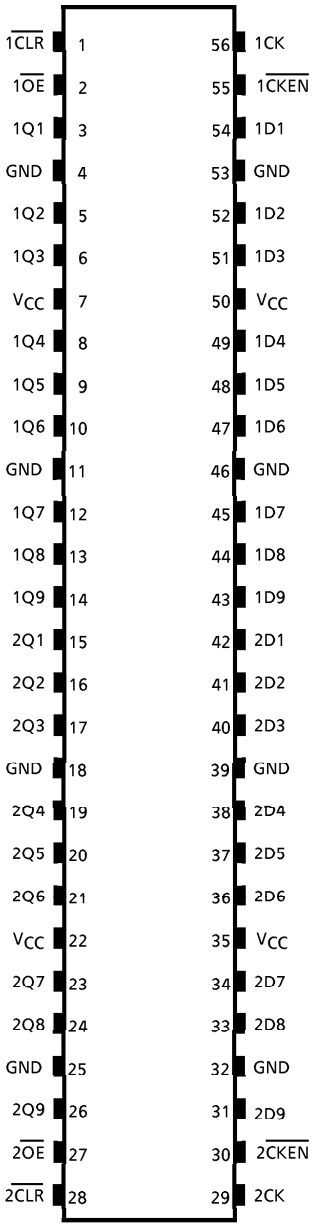
PRELIMINARY

FEATURES

- Low Voltage Operation : V_{CC} = 1.8 ~ 3.6V
- High Speed Operation : t_{pd} = TBD (max.) at V_{CC} = 3.0~3.6V
  : t_{pd} = TBD (max.) at V_{CC} = 2.3~2.7V
  : t_{pd} = TBD (max.) at V_{CC} = 1.8V
- 3.6V Tolerant inputs and outputs.
- Output Current : I_{OH} / I_{OL} = ±24mA (min.) at V_{CC} = 3.0V
  : I_{OH} / I_{OL} = ±18mA (min.) at V_{CC} = 2.3V
  : I_{OH} / I_{OL} = ±6mA (min.) at V_{CC} = 1.8V
- Latch-up Performance : ±300mA
- ESD Performance : Human Body Model > ±2000V
  : Machine Model > ±200V
- Package : TSSOP
  (Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.

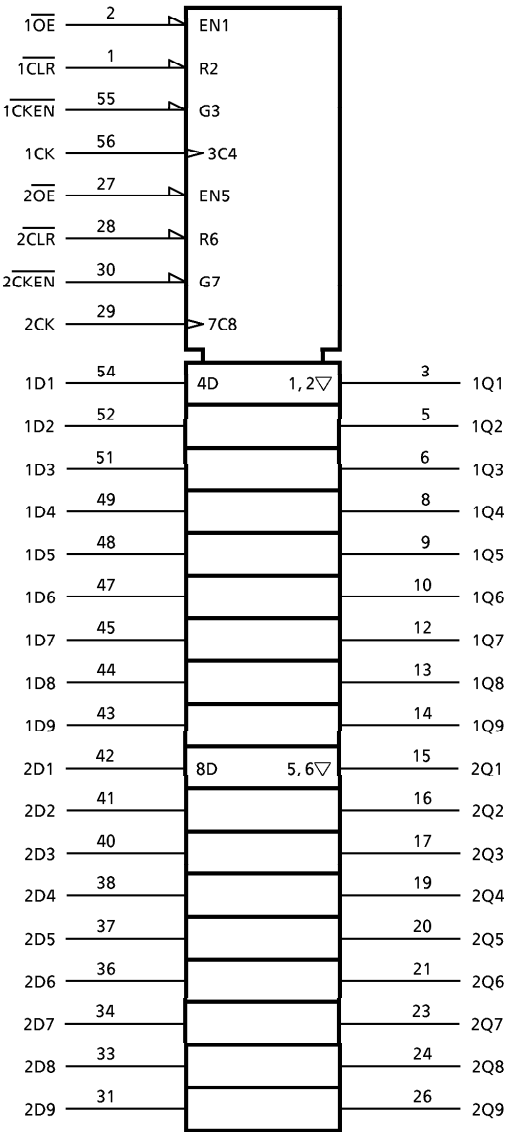
961001EBA2

PIN ASSIGNMENT



(TOP VIEW)

SYMBOL



TRUTH TABLE (each 9-bit flip flop)

INPUTS					OUTPUTS
$\overline{OE}$	$\overline{CLR}$	$\overline{CKEN}$	CK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	↓	X	Q0
L	H	H	X	X	Q0
H	X	X	X	X	Z

SYSTEM DIAGRAM