

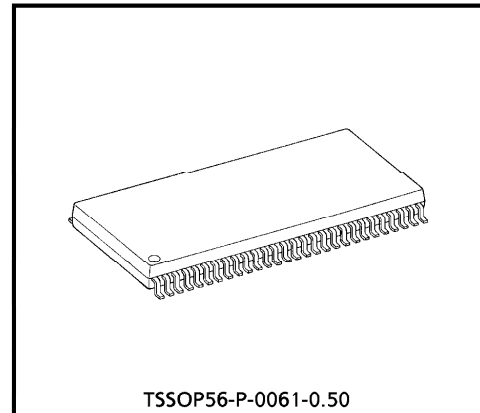
TC74VCX16823FT**LOW-VOLTAGE 18-BIT D-TYPE FLIP-FLOP
WITH 3.6V TOLERANT INPUTS AND OUTPUTS**

The TC74VCX16823FT is a high performance CMOS 18-bit D-TYPE FLIP-FLOP. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. It is also designed with over voltage tolerant inputs and outputs up to 3.6V.

The TC74VCX16823FT can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ($\overline{\text{CKEN}}$) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CKEN}}$ high disables the clock buffer, thus latching the outputs. Taking the clear ($\overline{\text{CLR}}$) input low causes the Q outputs to go low independently of the clock.

When the $\overline{\text{OE}}$ input is high, the outputs are in a high impedance state. This device is designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge.



TSSOP56-P-0061-0.50

Weight : 0.25g (Typ.)

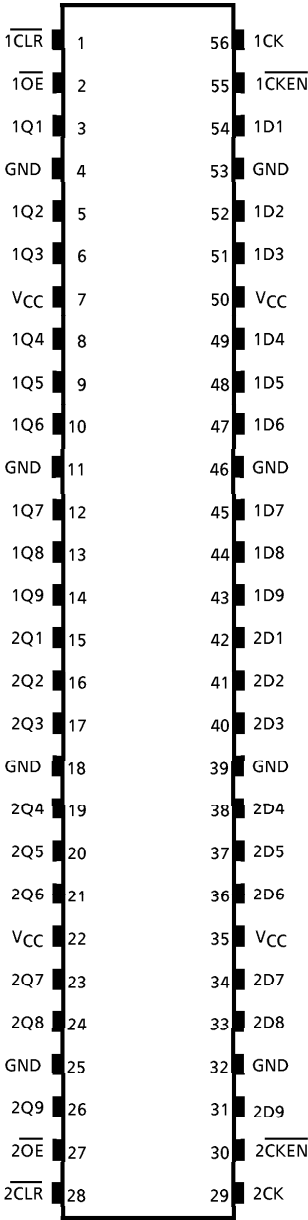
FEATURES

- Low Voltage Operation : $V_{CC} = 1.8 \sim 3.6V$
- High Speed Operation : $t_{pd} = \text{TBD (max.) at } V_{CC} = 3.0 \sim 3.6V$
 $t_{pd} = \text{TBD (max.) at } V_{CC} = 2.3 \sim 2.7V$
 $t_{pd} = \text{TBD (max.) at } V_{CC} = 1.8V$
- 3.6V Tolerant inputs and outputs.
- Output Current : $I_{OH} / I_{OL} = \pm 24mA \text{ (min.) at } V_{CC} = 3.0V$
 $I_{OH} / I_{OL} = \pm 18mA \text{ (min.) at } V_{CC} = 2.3V$
 $I_{OH} / I_{OL} = \pm 6mA \text{ (min.) at } V_{CC} = 1.8V$
- Latch-up Performance : $\pm 300mA$
- ESD Performance : Human Body Model $> \pm 2000V$
Machine Model $> \pm 200V$
- Package : TSSOP
(Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.

961001EBA2

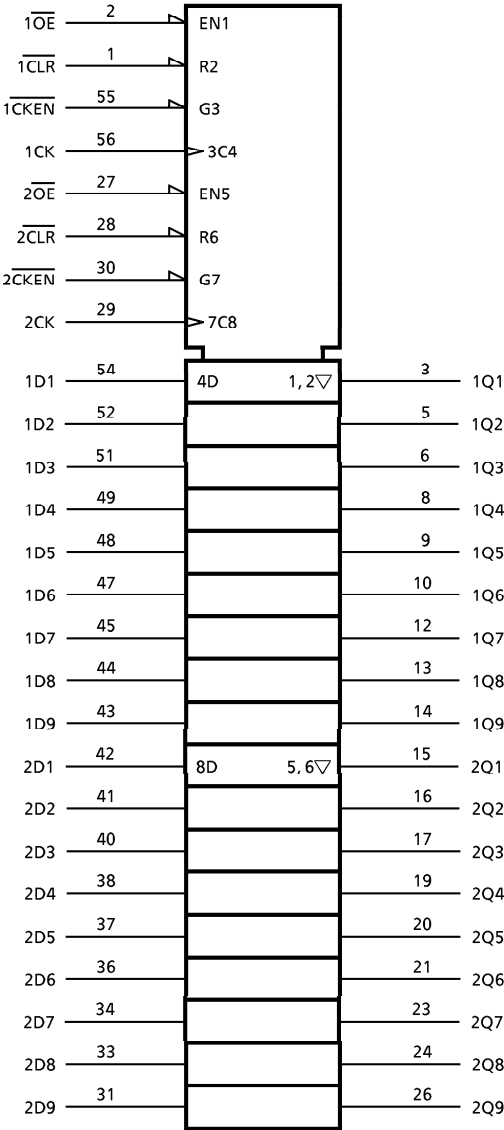
● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

PIN ASSIGNMENT



(TOP VIEW)

SYMBOL



PRELIMINARY

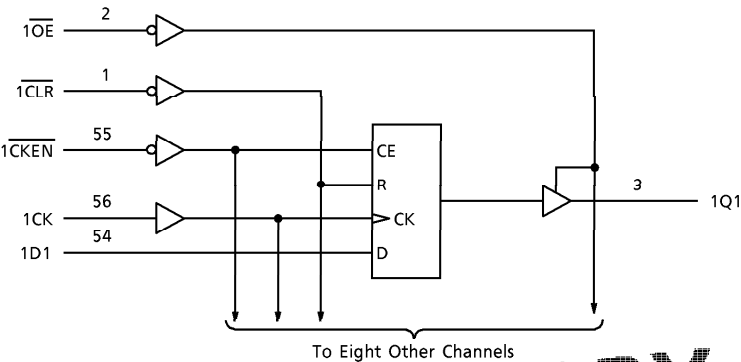
961001EBA2'

● The products described in this document are subject to foreign exchange and foreign trade control laws.
● The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
● The information contained herein is subject to change without notice.

TRUTH TABLE (each 9-bit flip flop)

INPUTS					OUTPUTS Q
OE	CLR	CKEN	CK	D	
L	L	X	X	X	L
L	H	L		H	H
L	H	L		L	L
L	H	L		X	Q0
L	H	H	X	X	Q0
H	X	X	X	X	Z

SYSTEM DIAGRAM



PRELIMINARY

