

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCX16245FT**LOW-VOLTAGE 16-BIT BUS TRANSCEIVER
WITH 3.6V TOLERANT INPUTS AND OUTPUTS**

The TC74VCX16245FT is a high performance CMOS 16-bit BUS TRANSCEIVER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

It is also designed with over voltage tolerant inputs and outputs up to 3.6V.

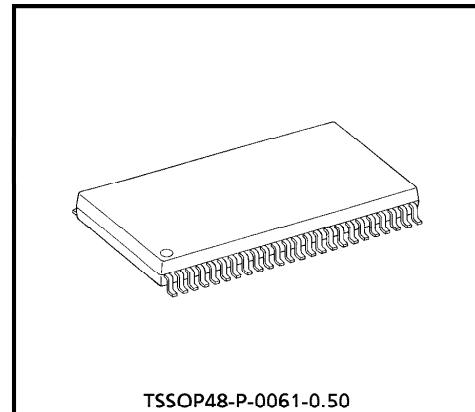
This 16bit bus transceiver is controlled by direction control (DIR) inputs and output enable (\overline{OE}) inputs which are common to each byte. It can be used as two 8-bit transceivers or one 16-bit transceiver. The direction of data transmission is determined by the level of the DIR inputs. The \overline{OE} inputs can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

FEATURES

- Low Voltage Operation : $V_{CC} = 1.8 \sim 3.6V$
- High Speed Operation : $t_{pd} = 2.5ns$ (max.) at $V_{CC} = 3.0 \sim 3.6V$
 : $t_{pd} = 3.2ns$ (max.) at $V_{CC} = 2.3 \sim 2.7V$
 : $t_{pd} = 5.7ns$ (max.) at $V_{CC} = 1.8V$
- 3.6V Tolerant inputs and outputs.
- Output Current : $I_{OH}/I_{OL} = \pm 24mA$ (min.) at $V_{CC} = 3.0V$
 : $I_{OH}/I_{OL} = \pm 18mA$ (min.) at $V_{CC} = 2.3V$
 : $I_{OH}/I_{OL} = \pm 6mA$ (min.) at $V_{CC} = 1.8V$
- Latch-up Performance : $\pm 300mA$
- ESD Performance : Human Body Model $> \pm 2000V$
 : Machine Model $> \pm 200V$
- Package : TSSOP (Thin Shrink Small Outline Package)
- Bidirectional interface between 2.5V and 3.3V signals.
- Power Down Protection is provided on all inputs and outputs

- Note 1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
 2) All floating (high impedance) bus terminal must have their input level fixed by means of pull up or pull down resistors.



TSSOP48-P-0061-0.50

Weight : 0.25g (Typ.)

PIN CONNECTION

1DIR	1	\overline{OE}	48
1B1	2	1A1	47
1B2	3	1A2	46
GND	4	GND	45
1B3	5	1A3	44
1B4	6	1A4	43
V_{CC}	7	V_{CC}	42
1B5	8	1A5	41
1B6	9	1A6	40
GND	10	GND	39
1B7	11	1A7	38
1B8	12	1A8	37
2B1	13	2A1	36
2B2	14	2A2	35
GND	15	GND	34
2B3	16	2A3	33
2B4	17	2A4	32
V_{CC}	18	V_{CC}	31
2B5	19	2A5	30
2B6	20	2A6	29
GND	21	GND	28
2B7	22	2A7	27
2B8	23	2A8	26
2DIR	24	\overline{OE}	25

(TOP VIEW)

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TRUTH TABLE

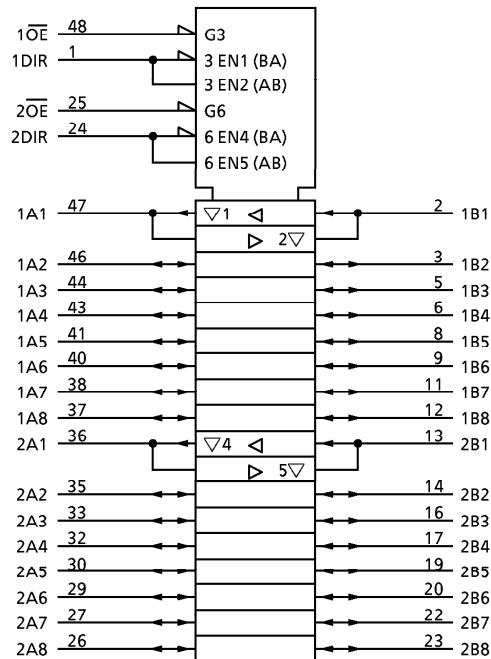
INPUT		FUNCTION		OUTPUT
1OE	1DIR	BUS 1A1-1A8	BUS 1B1-1B8	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	High Impedance		Z

INPUT		FUNCTION		OUTPUT
2OE	2DIR	BUS 2A1-2A8	BUS 2B1-2B8	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	High Impedance		Z

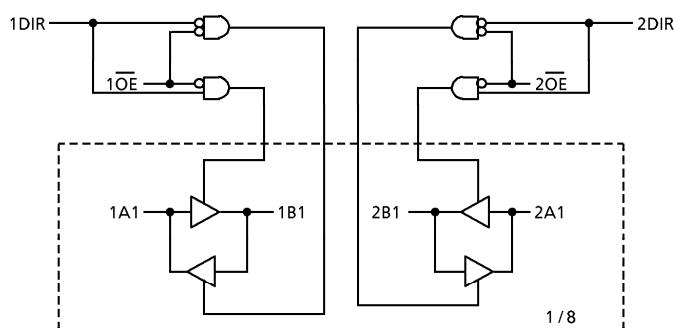
X : Don't Care

Z : High impedance

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



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MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	-0.5~4.6	V
DC Input Voltage (DIR, OE)	V_{IN}	-0.5~4.6	V
DC Bus I/O Voltage	$V_{I/O}$	-0.5~4.6 (Note 1)	V
		-0.5~ V_{CC} +0.5 (Note 2)	
Input Diode Current	I_{IK}	-50	mA
Output Diode Current	I_{OK}	± 50 (Note 3)	mA
DC Output Current	I_{OUT}	± 50	mA
Power Dissipation	P_D	400	mW
DC V_{CC} / Ground Current Per Supply Pin	I_{CC} / I_{GND}	± 100	mA
Storage Temperature	T_{stg}	-65~150	°C

(Note 1) Off-State

(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.(Note 3) $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	1.8~3.6	V
		1.2~3.6 (Note 4)	
Input Voltage (DIR, OE)	V_{IN}	-0.3~3.6	V
Bus I/O Voltage	$V_{I/O}$	0~3.6 (Note 5)	V
		0~ V_{CC} (Note 6)	
Output Current	I_{OH} / I_{OL}	± 24 (Note 7)	mA
		± 18 (Note 8)	
		± 6 (Note 9)	
Operating Temperature	T_{opr}	-40~85	°C
Input Rise And Fall Time	dt/dv	0~10 (Note 10)	ns/V

(Note 4) Data Retention Only

(Note 5) Off-State

(Note 6) High or Low State

(Note 7) $V_{CC} = 3.0 \sim 3.6V$ (Note 8) $V_{CC} = 2.3 \sim 2.7V$ (Note 9) $V_{CC} = 1.8V$ (Note 10) $V_{IN} = 0.8 \sim 2.0V$, $V_{CC} = 3.0V$

ELECTRICAL CHARACTERISTICSDC characteristics ($T_a = -40\sim85^\circ C$, $2.7V < V_{CC} \leq 3.6V$)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN.	MAX.	UNIT	
Input Voltage	"H" Level	V_{IH}			2.7~3.6	2.0	—	V	
	"L" Level	V_{IL}			2.7~3.6	—	0.8	V	
Output Voltage	"H" Level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100\mu A$	2.7~3.6	$V_{CC} - 0.2$	—	V	
				$I_{OH} = -12mA$	2.7	2.2	—		
				$I_{OH} = -18mA$	3.0	2.4	—		
				$I_{OH} = -24mA$	3.0	2.2	—		
	"L" Level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100\mu A$	2.7~3.6	—	0.2	V	
				$I_{OL} = 12mA$	2.7	—	0.4		
				$I_{OL} = 18mA$	3.0	—	0.4		
				$I_{OL} = 24mA$	3.0	—	0.55		
Input Leakage Current	I_{IN}	$V_{IN} = 0\sim 3.6V$		2.7~3.6	—	± 5.0	μA		
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0\sim 3.6V$		2.7~3.6	—	± 10.0	μA		
Power Off Leakage Current	I_{OFF}	$V_{IN}, V_{OUT} = 0\sim 3.6V$		0	—	10.0	μA		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		2.7~3.6	—	20.0	μA		
		$V_{CC} \leq (V_{IN}, V_{OUT}) \leq 3.6V$		2.7~3.6	—	± 20.0			
Increase In I_{CC} Per Input	ΔI_{CC}	$V_{IH} = V_{CC} - 0.6V$		2.7~3.6	—	750	μA		

ELECTRICAL CHARACTERISTICSDC characteristics ($T_a = -40\sim85^\circ C$, $2.3V \leq V_{CC} \leq 2.7V$)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN.	MAX.	UNIT	
Input Voltage	"H" Level	V_{IH}			2.3~2.7	1.6	—	V	
	"L" Level	V_{IL}			2.3~2.7	—	0.7	V	
Output Voltage	"H" Level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100\mu A$	2.3~2.7	$V_{CC} - 0.2$	—	V	
				$I_{OH} = -6mA$	2.3	2.0	—		
				$I_{OH} = -12mA$	2.3	1.8	—		
				$I_{OH} = -18mA$	2.3	1.7	—		
	"L" Level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100\mu A$	2.3~2.7	—	0.2	V	
				$I_{OL} = 12mA$	2.3	—	0.4		
				$I_{OL} = 18mA$	2.3	—	0.6		
Input Leakage Current	I_{IN}	$V_{IN} = 0\sim 3.6V$		2.3~2.7	—	± 5.0	μA		
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0\sim 3.6V$		2.3~2.7	—	± 10.0	μA		
Power Off Leakage Current	I_{OFF}	$V_{IN}, V_{OUT} = 0\sim 3.6V$		0	—	10.0	μA		
Quiescent Supply Current		I_{CC}	$V_{IN} = V_{CC}$ or GND	2.3~2.7	—	20.0	μA		
			$V_{CC} \leq (V_{IN}, V_{OUT}) \leq 3.6V_{CC}$	2.3~2.7	—	± 20.0			

ELECTRICAL CHARACTERISTICSDC characteristics ($T_a = -40\sim85^\circ C$, $1.8V \leq V_{CC} < 2.3V$)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN.	MAX.	UNIT
Input Voltage	"H" Level	V_{IH}			1.8~2.3	$0.7 \times V_{CC}$	—	V
	"L" Level	V_{IL}			1.8~2.3	—	$0.2 \times V_{CC}$	V
Output Voltage	"H" Level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100\mu A$	1.8	$V_{CC} - 0.2$	—	V
	"L" Level	V_{OL}		$I_{OL} = 100\mu A$	1.8	1.4	—	V
Input Leakage Current		I_{IN}	$V_{IN} = 0\sim 3.6V$		1.8	—	± 5.0	μA
3-State Output Off-State Current		I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0\sim 3.6V$		1.8	—	± 10.0	μA
Power Off Leakage Current		I_{OFF}	$V_{IN}, V_{OUT} = 0\sim 3.6V$		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	$V_{IN} = V_{CC}$ or GND $V_{CC} \leq (V_{IN}, V_{OUT}) \leq 3.6V$		1.8	—	20.0	μA
					1.8	—	± 20.0	

AC characteristics ($T_a = -40\sim85^\circ C$, Input $t_r = t_f = 2.0\text{ns}$, $C_L = 30\text{pF}$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	MIN.	MAX.	UNIT
				1.8	1.5	5.7	ns
Propagation Delay Time	t_{pLH} t_{pHL}	(Fig.1, 2)		2.5 ± 0.2	1.0	3.2	
				3.3 ± 0.3	0.8	2.5	
				1.8	1.5	7.5	
3-State Output Enable Time	t_{pZL} t_{pZH}	(Fig.1, 3)		2.5 ± 0.2	1.0	4.9	ns
				3.3 ± 0.3	0.8	3.8	
				1.8	1.5	5.5	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	(Fig.1, 3)		2.5 ± 0.2	1.0	4.2	ns
				3.3 ± 0.3	0.8	3.7	
				1.8	—	0.5	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 11)		2.5 ± 0.2	—	0.5	ns
				3.3 ± 0.3	—	0.5	
				1.8	—	0.5	

For $C_L = 50\text{pF}$, add approximately 300ps to the AC maximum specification.

(Note 11) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHm} - t_{pHn}|)$$

Dynamic switching characteristics ($T_a = 25^\circ\text{C}$, Input $t_r = t_f = 2.0\text{ns}$, $C_L = 30\text{pF}$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(\text{V})$	TYP.	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$V_{IH} = 1.8\text{V}$, $V_{IL} = 0\text{V}$ (Note 12)	1.8	0.25	V
		$V_{IH} = 2.5\text{V}$, $V_{IL} = 0\text{V}$ (Note 12)	2.5	0.6	
		$V_{IH} = 3.3\text{V}$, $V_{IL} = 0\text{V}$ (Note 12)	3.3	0.8	
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	$V_{IH} = 1.8\text{V}$, $V_{IL} = 0\text{V}$ (Note 12)	1.8	-0.25	V
		$V_{IH} = 2.5\text{V}$, $V_{IL} = 0\text{V}$ (Note 12)	2.5	-0.6	
		$V_{IH} = 3.3\text{V}$, $V_{IL} = 0\text{V}$ (Note 12)	3.3	-0.8	
Quiet Output Minimum Dynamic V_{OH}	V_{OHV}	$V_{IH} = 1.8\text{V}$, $V_{IL} = 0\text{V}$ (Note 12)	1.8	1.5	V
		$V_{IH} = 2.5\text{V}$, $V_{IL} = 0\text{V}$ (Note 12)	2.5	1.9	
		$V_{IH} = 3.3\text{V}$, $V_{IL} = 0\text{V}$ (Note 12)	3.3	2.2	

(Note 12) Parameter guaranteed by design.

Capacitive characteristics ($T_a = 25^\circ\text{C}$)

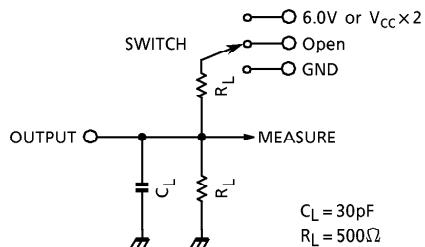
PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(\text{V})$	TYP.	UNIT
Input Capacitance	C_{IN}	DIR, \overline{OE}	1.8, 2.5, 3.3	6	pF
Bus I/O Capacitance	$C_{I/O}$	An, Bn	1.8, 2.5, 3.3	7	pF
Power Dissipation Capacitance	C_{PD}	$f_{IN} = 10\text{MHz}$ (Note 13)	1.8, 2.5, 3.3	20	pF

(Note 13) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

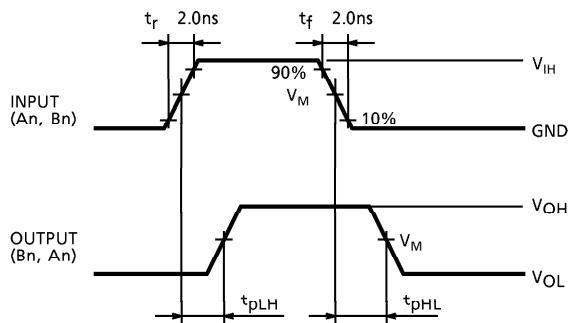
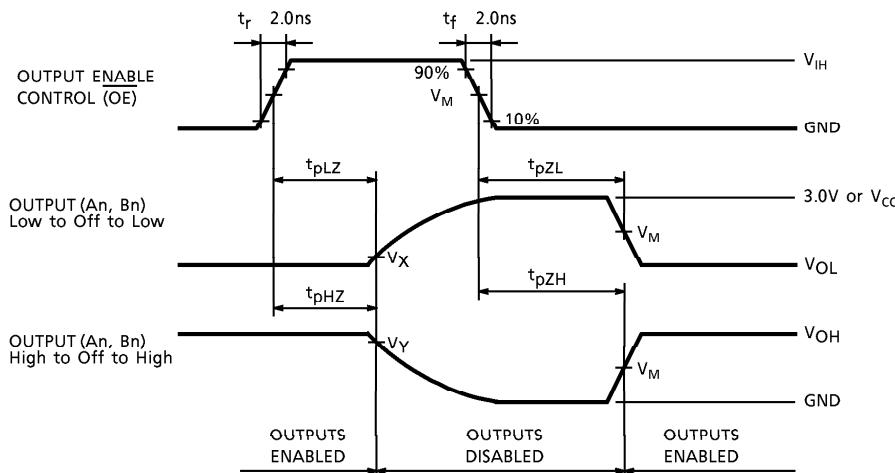
$$I_{CC(\text{opr.})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 16 \text{ (per bit)}$$

Fig.1 Test circuit



PARAMETER	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PLZ}, t_{PZL}	6.0V @ $V_{CC} = 3.3 \pm 0.3\text{V}$ V_{CCX2} @ $V_{CC} = 2.5 \pm 0.2\text{V}$ @ $V_{CC} = 1.8\text{V}$
t_{PHZ}, t_{PZH}	GND

AC WAVEFORM

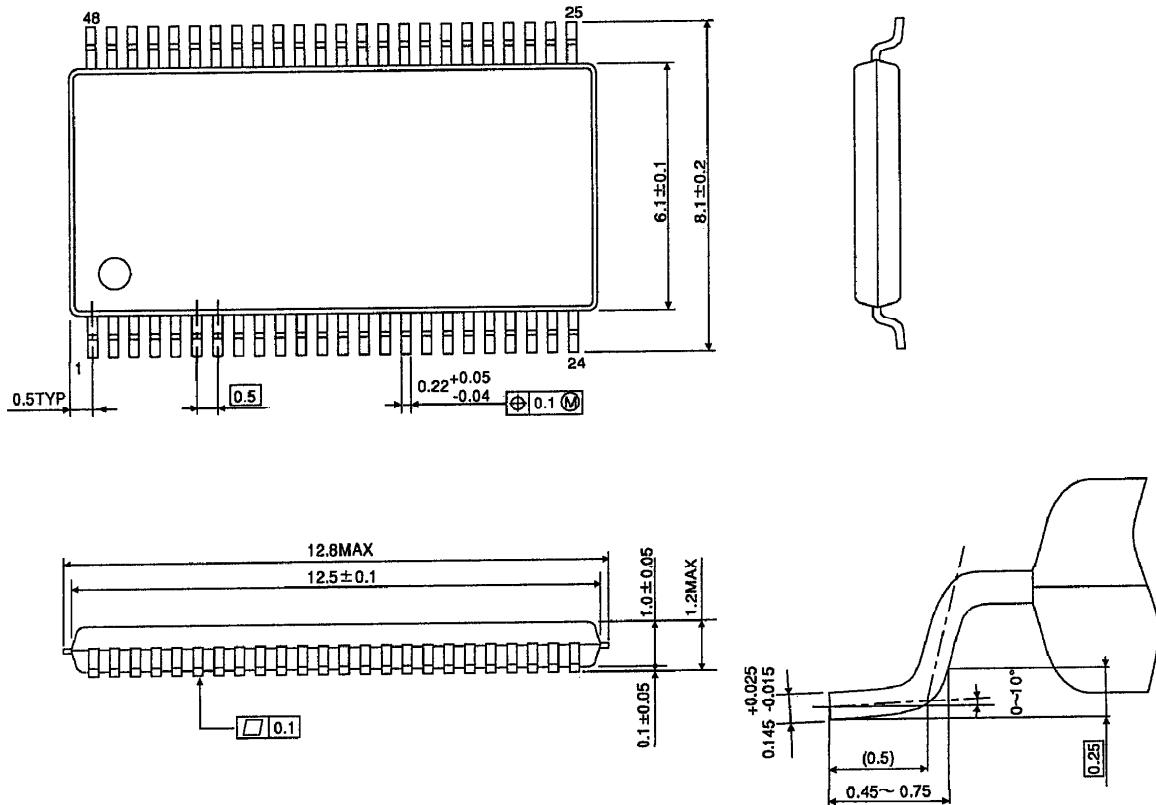
Fig.2 t_{PLH}, t_{PHL} Fig.3 $t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}$ 

SYMBOL	V_{CC}		
	$3.3 \pm 0.3\text{V}$	$2.5 \pm 0.2\text{V}$	1.8V
V_{IH}	2.7V	V_{CC}	V_{CC}
V_M	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.15\text{V}$	$V_{OL} + 0.15\text{V}$
V_Y	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.15\text{V}$	$V_{OH} - 0.15\text{V}$

OUTLINE DRAWING

TSSOP48-P-0061-0.50

Unit : mm



Weight : 0.25g (Typ.)