

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

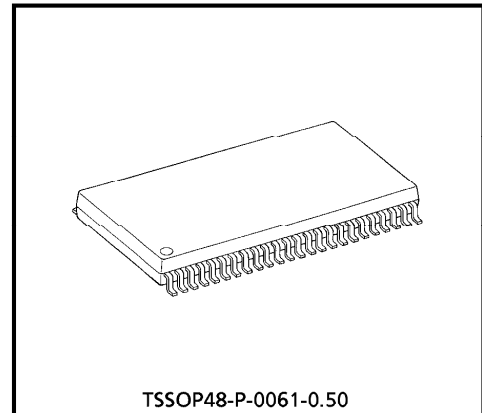
TC74VCX162374FT**LOW-VOLTAGE 16-BIT D-TYPE FLIP-FLOP
WITH 3.6V TOLERANT INPUTS AND OUTPUTS**

The TC74VCX162374FT is a high performance CMOS 16-bit D-TYPE FLIP FLOP. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. It is also designed with over voltage tolerant inputs and outputs up to 3.6V.

This 16-bit D-type flip-flop is controlled by a clock input (CK) and a output enable input (OE) which are common to each byte. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. When the $\overline{OE}$ input is high, the outputs are in a high impedance state.

The 26- Ω series resistor helps reducing output overshoot and undershoot without external resistor.

All inputs are equipped with protection circuits against static discharge.



Weight : 0.25g (Typ.)

FEATURES

- 26- Ω Series Resistors on Outputs.
- Low Voltage Operation : $V_{CC} = 1.8 \sim 3.6V$
- High Speed Operation : $t_{pd} = 3.4ns$ (max.) at $V_{CC} = 3.0 \sim 3.6V$
 $t_{pd} = 4.8ns$ (max.) at $V_{CC} = 2.3 \sim 2.7V$
 $t_{pd} = 6.0ns$ (max.) at $V_{CC} = 1.8V$
- 3.6V Tolerant inputs and outputs.
- Output Current : $I_{OH}/I_{OL} = \pm 12mA$ (min.) at $V_{CC} = 3.0V$
 $I_{OH}/I_{OL} = \pm 8mA$ (min.) at $V_{CC} = 2.3V$
 $I_{OH}/I_{OL} = \pm 4mA$ (min.) at $V_{CC} = 1.8V$
- Latch-up Performance : $\pm 300mA$
- ESD Performance : Human Body Model $> \pm 2000V$
Machine Model $> \pm 200V$
- Package : TSSOP
(Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.

PIN CONNECTION

$\overline{1OE}$	1	48	1CK
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	4	45	GND
1Q3	5	44	1D3
1Q4	6	43	1D4
VCC	7	42	VCC
1Q5	8	41	1D5
1Q6	9	40	1D6
GND	10	39	GND
1Q7	11	38	1D7
1Q8	12	37	1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	16	33	2D3
2Q4	17	32	2D4
VCC	18	31	VCC
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	GND
2Q7	22	27	2D7
2Q8	23	26	2D8
$\overline{2OE}$	24	25	2CK

(TOP VIEW)

961001EBA2

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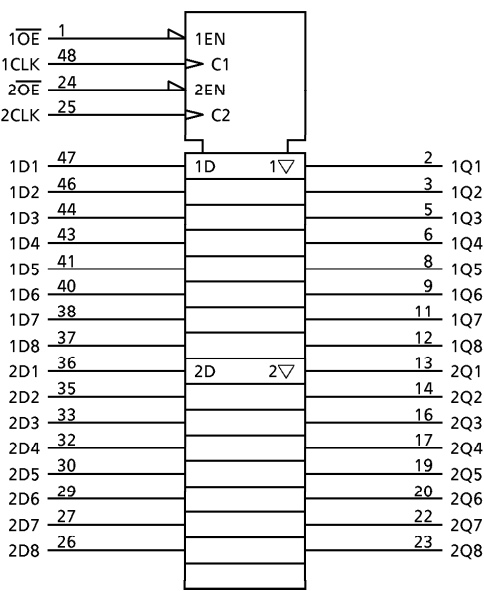
TRUTH TABLE

INPUT			OUTPUT
1OE	1CK	1D1-1D8	1Q1-1Q8
H	X	X	Z
L		X	Qn
L		L	L
L		H	H

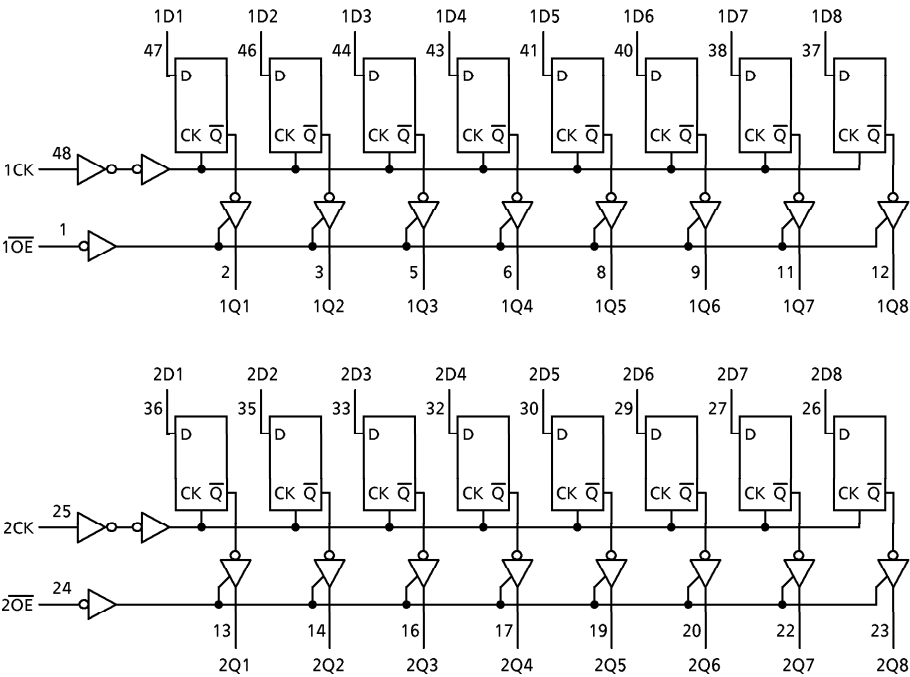
INPUT			OUTPUT
2OE	2CK	2D1-2D8	2Q1-2Q8
H	X	X	Z
L		X	Qn
L		L	L
L		H	H

X : Don't Care
Z : High impedance
Qn : No change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



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MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	$-0.5 \sim 4.6$	V
DC Input Voltage	V_{IN}	$-0.5 \sim 4.6$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim 4.6$ (Note 1)	V
		$-0.5 \sim V_{CC} + 0.5$ (Note 2)	
Input Diode Current	I_{IK}	-50	mA
Output Diode Current	I_{OK}	± 50 (Note 3)	mA
DC Output Current	I_{OUT}	± 50	mA
Power Dissipation	P_D	400	mW
DC V_{CC} / Ground Current Per Supply Pin	I_{CC} / I_{GND}	± 100	mA
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

(Note 1) Off-State

(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.(Note 3) $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	1.8~3.6	V
		1.2~3.6 (Note 4)	
Input Voltage	V_{IN}	$-0.3 \sim 3.6$	V
Output Voltage	V_{OUT}	0~3.6 (Note 5)	V
		0~ V_{CC} (Note 6)	
Output Current	I_{OH} / I_{OL}	± 12 (Note 7)	mA
		± 8 (Note 8)	
		± 4 (Note 9)	
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise And Fall Time	dt / dv	0~10 (Note 10)	ns / V

(Note 4) Data Retention Only

(Note 5) Off-State

(Note 6) High or Low State

(Note 7) $V_{CC} = 3.0 \sim 3.6V$ (Note 8) $V_{CC} = 2.3 \sim 2.7V$ (Note 9) $V_{CC} = 1.8V$ (Note 10) $V_{IN} = 0.8 \sim 2.0V$, $V_{CC} = 3.0V$

ELECTRICAL CHARACTERISTICS

DC characteristics ($T_a = -40 \sim 85^\circ\text{C}$, $2.7\text{V} < V_{CC} \leq 3.6\text{V}$)

PARAMETER		SYMBOL	TEST CONDITION		V _{CC} (V)	MIN.	MAX.	UNIT
Input Voltage	"H" Level	V _{IH}			2.7~3.6	2.0	—	V
	"L" Level	V _{IL}			2.7~3.6	—	0.8	V
Output Voltage	"H" Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 100μA	2.7~3.6	V _{CC} - 0.2	—	V
				I _{OH} = - 6mA	2.7	2.2	—	
				I _{OH} = - 8mA	3.0	2.4	—	
				I _{OH} = - 12mA	3.0	2.2	—	
	"L" Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100μA	2.7~3.6	—	0.2	V
				I _{OL} = 6mA	2.7	—	0.4	
				I _{OL} = 8mA	3.0	—	0.55	
				I _{OL} = 12mA	3.0	—	0.8	
Input Leakage Current		I _{IN}	V _{IN} = 0~3.6V	2.7~3.6	—	± 5.0	μA	
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~3.6V	2.7~3.6	—	± 10.0	μA	
Power Off Leakage Current		I _{OFF}	V _{IN} , V _{OUT} = 0~3.6V	0	—	10.0	μA	
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND	2.7~3.6	—	20.0	μA	
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6V	2.7~3.6	—	± 20.0		
Increase In I _{CC} Per Input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6V	2.7~3.6	—	750	μA	

ELECTRICAL CHARACTERISTICS

DC characteristics ($T_a = -40 \sim 85^\circ\text{C}$, $2.3\text{V} \leq V_{CC} \leq 2.7\text{V}$)

PARAMETER		SYMBOL	TEST CONDITION		V _{CC} (V)	MIN.	MAX.	UNIT
Input Voltage	“H” Level	V _{IH}			2.3~2.7	1.6	—	V
	“L” Level	V _{IL}			2.3~2.7	—	0.7	V
Output Voltage	“H” Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 100μA	2.3~2.7	V _{CC} - 0.2	—	V
				I _{OH} = - 4mA	2.3	2.0	—	
				I _{OH} = - 6mA	2.3	1.8	—	
				I _{OH} = - 8mA	2.3	1.7	—	
	“L” Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100μA	2.3~2.7	—	0.2	V
				I _{OL} = 6mA	2.3	—	0.4	
				I _{OL} = 8mA	2.3	—	0.6	
Input Leakage Current		I _{IN}	V _{IN} = 0~3.6V	2.3~2.7	—	± 5.0	μA	
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~3.6V	2.3~2.7	—	± 10.0	μA	
Power Off Leakage Current		I _{OFF}	V _{IN} , V _{OUT} = 0~3.6V	0	—	10.0	μA	
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND	2.3~2.7	—	20.0	μA	
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6V _{CC}	2.3~2.7	—	± 20.0		

ELECTRICAL CHARACTERISTICS

DC characteristics ($T_a = -40 \sim 85^\circ\text{C}$, $1.8\text{V} \leq V_{CC} < 2.3\text{V}$)

PARAMETER		SYMBOL	TEST CONDITION		V _{CC} (V)	MIN.	MAX.	UNIT
Input Voltage	“H” Level	V _{IH}			1.8~2.3	0.7× V _{CC}	—	V
	“L” Level	V _{IL}			1.8~2.3	—	0.2× V _{CC}	V
Output Voltage	“H” Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 100μA	1.8	V _{CC} - 0.2	—	V
				I _{OH} = - 4mA	1.8	1.4	—	
	“L” Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100μA	1.8	—	0.2	V
				I _{OL} = 4mA	1.8	—	0.3	
Input Leakage Current		I _{IN}	V _{IN} = 0~3.6V		1.8	—	± 5.0	μA
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~3.6V		1.8	—	± 10.0	μA
Power Off Leakage Current		I _{OFF}	V _{IN} , V _{OUT} = 0~3.6V		0	—	10.0	μA
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND		1.8	—	20.0	μA
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6V		1.8	—	± 20.0	

AC characteristics ($T_a = -40 \sim 85^\circ\text{C}$, Input $t_r = t_f = 2.0\text{ns}$, $C_L = 30\text{pF}$, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	MIN.	MAX.	UNIT
Maximum Clock Frequency	f_{MAX}	(Fig.1, 2)	1.8	125	—	MHz
			2.5 ± 0.2	200	—	
			3.3 ± 0.3	250	—	
Propagation Delay Time (CK-Q)	t_{pLH} t_{pHL}	(Fig.1, 2)	1.8	1.5	6.0	ns
			2.5 ± 0.2	1.0	4.8	
			3.3 ± 0.3	0.8	3.4	
3-State Output Enable Time	t_{pZL} t_{pZH}	(Fig.1, 3)	1.8	1.5	7.6	ns
			2.5 ± 0.2	1.0	5.4	
			3.3 ± 0.3	0.8	3.9	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	(Fig.1, 3)	1.8	1.5	5.3	ns
			2.5 ± 0.2	1.0	4.4	
			3.3 ± 0.3	0.8	4.0	
Minimum Pulse Width (CK)	$t_{\text{w}}(\text{H})$ $t_{\text{w}}(\text{L})$	(Fig.1, 2)	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum Set-up Time	t_{s}	(Fig.1, 2)	1.8	1.0	—	ns
			2.5 ± 0.2	1.0	—	
			3.3 ± 0.3	1.0	—	
Minimum Hold Time	t_{h}	(Fig.1, 2)	1.8	3.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 11)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

For $C_L = 50\text{pF}$, add approximately 300ps to the AC maximum specification.

(Note 11) Parameter guaranteed by design.

($t_{\text{osLH}} = |t_{\text{pLHm}} - t_{\text{pLHn}}|$, $t_{\text{osHL}} = |t_{\text{pHLm}} - t_{\text{pHLn}}|$)

Dynamic switching characteristics (Ta = 25°C, Input $t_r = t_f = 2.0\text{ns}$, $C_L = 30\text{pF}$)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	V _{IH} = 1.8V, V _{IL} = 0V (Note 12)	1.8	0.15	V
		V _{IH} = 2.5V, V _{IL} = 0V (Note 12)	2.5	0.25	
		V _{IH} = 3.3V, V _{IL} = 0V (Note 12)	3.3	0.35	
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	V _{IH} = 1.8V, V _{IL} = 0V (Note 12)	1.8	-0.15	V
		V _{IH} = 2.5V, V _{IL} = 0V (Note 12)	2.5	-0.25	
		V _{IH} = 3.3V, V _{IL} = 0V (Note 12)	3.3	-0.35	
Quiet Output Minimum Dynamic V _{OH}	V _{OHV}	V _{IH} = 1.8V, V _{IL} = 0V (Note 12)	1.8	1.55	V
		V _{IH} = 2.5V, V _{IL} = 0V (Note 12)	2.5	2.05	
		V _{IH} = 3.3V, V _{IL} = 0V (Note 12)	3.3	2.65	

(Note 12) Parameter guaranteed by design.

Capacitive characteristics (Ta = 25°C)

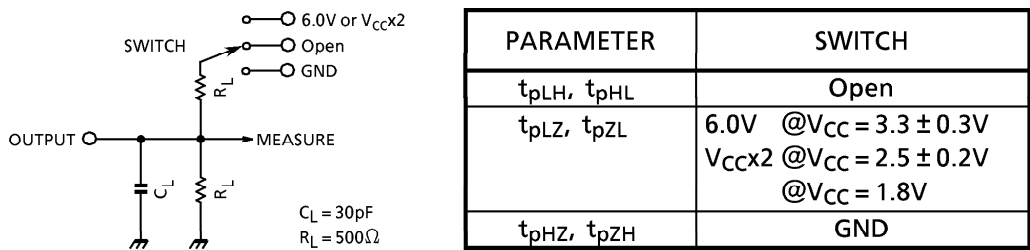
PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Input Capacitance	C _{IN}		1.8, 2.5, 3.3	6	pF
Output Capacitance	C _O		1.8, 2.5, 3.3	7	pF
Power Dissipation Capacitance	C _{PD}	f _{IN} = 10MHz (Note 13)	1.8, 2.5, 3.3	20	pF

(Note 13) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

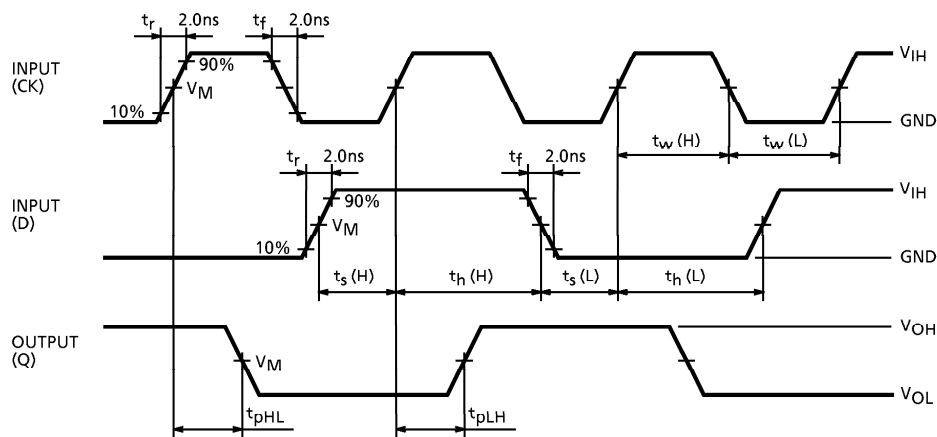
$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 16 \text{ (per bit)}$$

Fig.1 Test circuit



AC WAVEFORM

Fig.2 $t_{pLH}, t_{pHL}, t_w, t_s, t_h$



Timing diagram for the 74VHC125 1-to-3-state buffer. The diagram shows the relationship between the OUTPUT ENABLE (OE) signal and the OUTPUT (Q) signals during transitions between enabled and disabled states.

Signals and Levels:

- OUTPUT ENABLE (OE):** Transitions between V_{IH} and GND.
- OUTPUT (Q) Low to Off to Low:** Transitions between V_{OL} and V_{XX} (high-impedance state).
- OUTPUT (Q) High to Off to High:** Transitions between V_{OH} and V_{YY} (high-impedance state).

Timing Parameters:

- t_r : Rise time of OE signal (2.0ns).
- t_f : Fall time of OE signal (2.0ns).
- t_{pLZ} : Propagation delay from OE falling edge to output Q going low.
- t_{pZL} : Propagation delay from OE rising edge to output Q going low.
- t_{pHZ} : Propagation delay from OE falling edge to output Q going high.
- t_{pZH} : Propagation delay from OE rising edge to output Q going high.

Output Voltage Levels:

- V_{XX} : Output voltage during low-to-off transition.
- V_{YY} : Output voltage during high-to-off transition.
- V_M : Output voltage during off-to-low and off-to-high transitions.
- V_{OH} : Output voltage during high-to-off transition.
- V_{OL} : Output voltage during low-to-off transition.

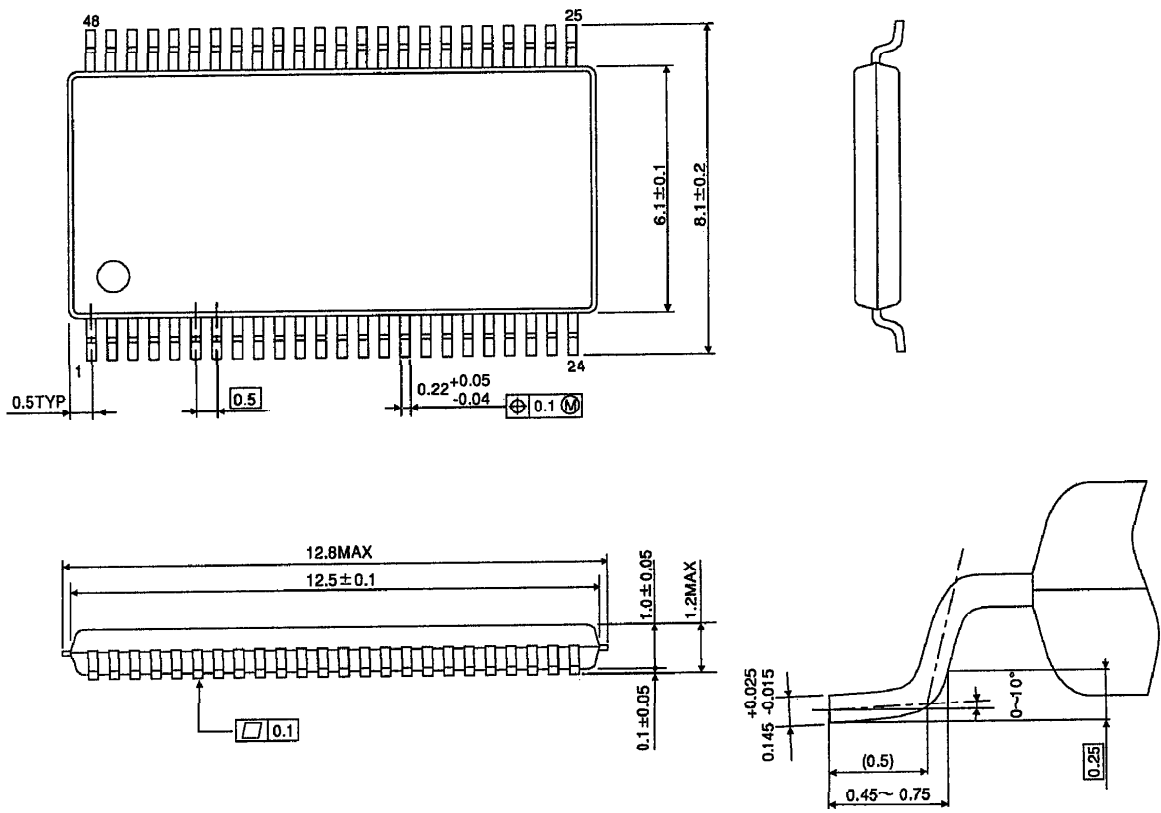
Regions:

- OUTPUTS ENABLED:** Initial state where both outputs are active.
- OUTPUTS DISABLED:** State where both outputs are in high-impedance.
- OUTPUTS ENABLED:** Final state where both outputs are active again.

SYMBOL	V _{CC}		
	3.3 ± 0.3V	2.5 ± 0.2V	1.8V
V _{IH}	2.7V	V _{CC}	V _{CC}
V _M	1.5V	V _{CC} / 2	V _{CC} / 2
V _X	V _{OL} + 0.3V	V _{OL} + 0.15V	V _{OL} + 0.15V
V _Y	V _{OH} - 0.3V	V _{OH} - 0.15V	V _{OH} - 0.15V

OUTLINE DRAWING
TSSOP48-P-0061-0.50

Unit : mm



Weight : 0.25g (Typ.)