

TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

262,144-WORD BY 16-BIT FULL CMOS STATIC RAM

DESCRIPTION

The TC55NEM216AFTN is a 4,194,304-bit static random access memory (SRAM) organized as 262,144 words by 16 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5V \pm 10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz (typ) and a minimum cycle time of 55 ns. It is automatically placed in low-power mode at 1 μ A standby current (typ) when chip enable (\overline{CE}) is asserted high. There are two control inputs. \overline{CE} is used to select the device and for data retention control, and output enable (\overline{OE}) provides fast memory access. Data byte control pin (\overline{LB} , \overline{UB}) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating extreme temperature range of -40° to 85°C , the TC55NEM216AFTN can be used in environments exhibiting extreme temperature conditions. The TC55NEM216AFTN is available in a plastic 54-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
Operating: 15 mW/MHz (typical)
- Single power supply voltage of 5 V \pm 10%
- Power down features using \overline{CE}
- Data retention supply voltage of 2.0 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of -40° to 85°C
- Standby Current (maximum): 20 μ A

- Access Times (maximum):

	TC55NEM216AFTN	
	55	70
Access Time	55 ns	70 ns
\overline{CE} Access Time	55 ns	70 ns
\overline{OE} Access Time	30 ns	35 ns

- Package:
TSOP II54-P-400-0.80 (Weight: g typ)

PIN ASSIGNMENT (TOP VIEW)

54 PIN TSOP

NC	1	54	A4
A3	2	53	A5
A2	3	52	A6
A1	4	51	A7
A0	5	50	NC
I/O16	6	49	I/O1
I/O15	7	48	I/O2
V _{DD}	8	47	V _{DD}
GND	9	46	GND
I/O14	10	45	I/O3
I/O13	11	44	I/O4
\overline{UB}	12	43	\overline{LB}
\overline{CE}	13	42	\overline{OE}
OP	14	41	OP
R/W	15	40	NC
I/O12	16	39	I/O5
I/O11	17	38	I/O6
GND	18	37	GND
V _{DD}	19	36	V _{DD}
I/O10	20	35	I/O7
I/O9	21	34	I/O8
NC	22	33	A8
A17	23	32	A9
A16	24	31	A10
A15	25	30	A11
A14	26	29	A12
A13	27	28	NC

PIN NAMES

A0~A17	Address Inputs
\overline{CE}	Chip Enable
R/W	Read/Write Control
\overline{OE}	Output Enable
\overline{LB} , \overline{UB}	Data Byte Control
I/O1~I/O16	Data Inputs/Outputs
V _{DD}	Power (+5 V)
GND	Ground
NC	No Connection
OP*	Option

*: OP pin must be open or connected to GND.

The diagram illustrates the internal architecture of a 256Kbit DRAM. Key components include:

- Memory Cell Array:** A 2,048 × 128 × 16 (4,194,304) array of memory cells.
- Row Addressing:** Consists of a Row Address Buffer, Row Address Register, and Row Address Decoder, connected to address lines A6 through A17.
- Column Addressing:** Consists of a Column Address Decoder, Column Address Register, and Column Address Buffer, connected to address lines A0 through A5 and A16.
- Sense Amp:** Receives data from the memory cell array and outputs to the Data Output Buffer.
- Data Input/Output Buffers:** Handle data transfer between the memory array and the external I/O lines (I/O0 through I/O16).
- Clock Generator:** Generates the internal clock signal (CE) from external control signals.
- Control Logic:** Uses external signals (CE, LB, UB, R/W, OE) and logic gates to manage the internal clock and data flow.

OPERATING MODE

MODE	\overline{CE}	\overline{OE}	R/W	\overline{LB}	\overline{UB}	I/O1~I/O8	I/O9~I/O16	POWER
Read	L	L	H	L	L	Output	Output	I _{DDO}
	L	L	H	H	L	High-Z	Output	I _{DDO}
	L	L	H	L	H	Output	High-Z	I _{DDO}
Write	L	*	L	L	L	Input	Input	I _{DDO}
	L	*	L	H	L	High-Z	Input	I _{DDO}
	L	*	L	L	H	Input	High-Z	I _{DDO}
Output Deselect	L	H	H	L	L	High-Z	High-Z	I _{DDO}
	L	H	H	H	L	High-Z	High-Z	I _{DDO}
	L	H	H	L	H	High-Z	High-Z	I _{DDO}
Standby	H	*	*	*	*	High-Z	High-Z	I _{DDS}
	*	*	*	H	H	High-Z	High-Z	I _{DDS}

* = don't care

H = logic high

L = logic low

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	-0.3~7.0	V
V _{IN}	Input Voltage	-0.3*~7.0	V
V _{I/O}	Input/Output Voltage	-0.5~V _{DD} + 0.5	V
P _D	Power Dissipation	0.6	W
T _{solder}	Soldering Temperature (10s)	260	°C
T _{stg}	Storage Temperature	-55~150	°C
T _{opr}	Operating Temperature	-40~85	°C

*: -2.0 V when measured at a pulse width of 20ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = -40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	—	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	-0.3*	—	0.6	V
V _{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

*: -2.0 V when measured at a pulse width of 20ns

DC CHARACTERISTICS ($T_a = -40^\circ \text{ to } 85^\circ \text{C}$, $V_{DD} = 5 \text{ V} \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT		
I _{IL}	Input Leakage Current	V _{IN} = 0 V~V _{DD}			—	—	±1.0	μA		
I _{OH}	Output High Current	V _{OH} = 2.4 V			−1.0	—	—	mA		
I _{OL}	Output Low Current	V _{OL} = 0.4 V			2.1	—	—	mA		
I _{LO}	Output Leakage Current	CE = V _{IH} or LB = UB = V _{IH} or R/W = V _{IL} or OE = V _{IH} , V _{OUT} = 0 V~V _{DD}			—	—	±1.0	μA		
I _{DDO1}	Operating Current	CE = V _{IL} and R/W = V _{IH} , LB = UB = V _{IL} , I _{OUT} = 0 mA, Other Input = V _{IH} /V _{IL}	t _{cycle}	MIN	—	—	35	mA		
				1 μs	—	8	—			
I _{DDO2}	Operating Current	CE = 0.2 V and R/W = V _{DD} − 0.2 V, LB = UB = 0.2 V, I _{OUT} = 0 mA, Other Input = V _{DD} − 0.2 V/0.2 V	t _{cycle}	MIN	—	—	30	mA		
				1 μs	—	3	—			
I _{DDS1}	Standby Current	1) CE = V _{IH} 2) LB = UB = V _{IH}			—	—	3	mA		
I _{DDS2}		1) CE = V _{DD} − 0.2 V 2) LB = UB = V _{DD} − 0.2 V, CE = 0.2 V			Ta = 25°C		—	1	μA	
					Ta = −40~40°C		—	—		3
					Ta = −40~85°C		—	—		20

CAPACITANCE ($T_a = 25^\circ \text{C}$, $f = 1 \text{ MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS(Ta = -40°C to 85°C, V_{DD} = 5 V ± 10%)**READ CYCLE**

SYMBOL	PARAMETER	TC55NEM216AFTN				UNIT
		55		70		
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	55	—	70	—	ns
t _{ACC}	Address Access Time	—	55	—	70	
t _{CO}	Chip Enable Access Time	—	55	—	70	
t _{OE}	Output Enable Access Time	—	30	—	35	
t _{BA}	Data Byte Control Access Time	—	55	—	70	
t _{COE}	Chip Enable Low to Output Active	5	—	5	—	
t _{OOE}	Output Enable Low to Output Active	0	—	0	—	
t _{BE}	Data Byte Control Low to Output Active	5	—	5	—	
t _{OD}	Chip Enable High to Output High-Z	—	25	—	30	
t _{ODO}	Output Enable High to Output High-Z	—	25	—	30	
t _{BD}	Data Byte Control High to Output High-Z	—	25	—	30	
t _{OH}	Output Data Hold Time	10	—	10	—	

WRITE CYCLE

SYMBOL	PARAMETER	TC55NEM216AFTN				UNIT
		55		70		
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	55	—	70	—	ns
t _{WP}	Write Pulse Width	40	—	50	—	
t _{CW}	Chip Enable to End of Write	45	—	55	—	
t _{BW}	Data Byte Control to End of Write	45	—	55	—	
t _{AS}	Address Setup Time	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	
t _{ODW}	R/W Low to Output High-Z	—	25	—	30	
t _{OEW}	R/W High to Output Active	0	—	0	—	
t _{DS}	Data Setup Time	25	—	30	—	
t _{DH}	Data Hold Time	0	—	0	—	

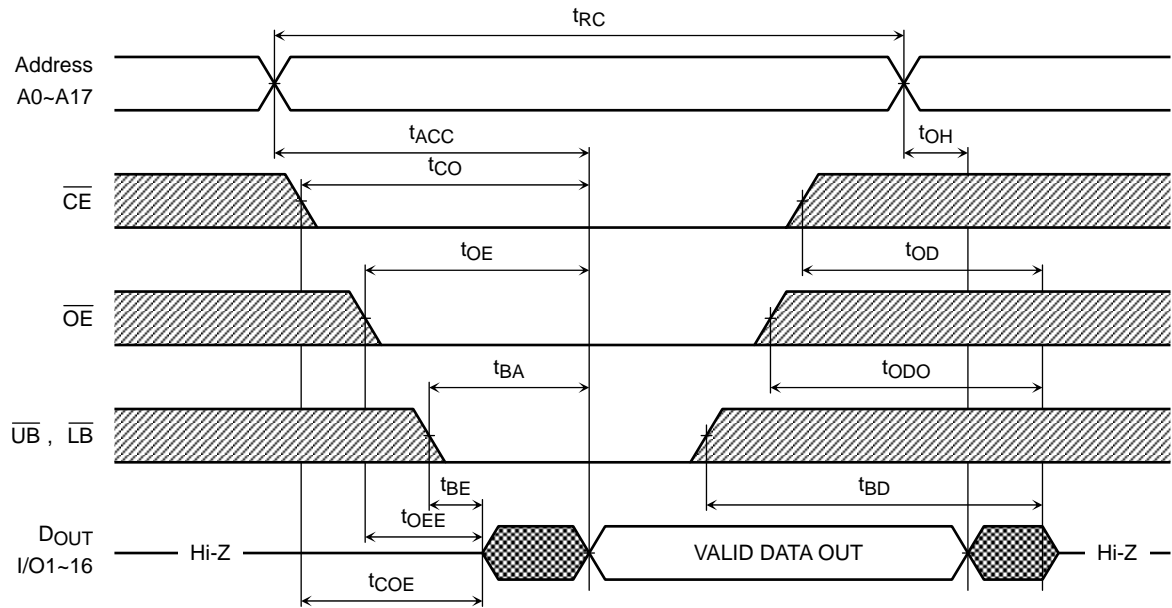
Note: t_{OD}, t_{ODO}, t_{BD} and t_{ODW} are specified in time when an output becomes high impedance, and are not judged depending on an output voltage level.

AC TEST CONDITIONS

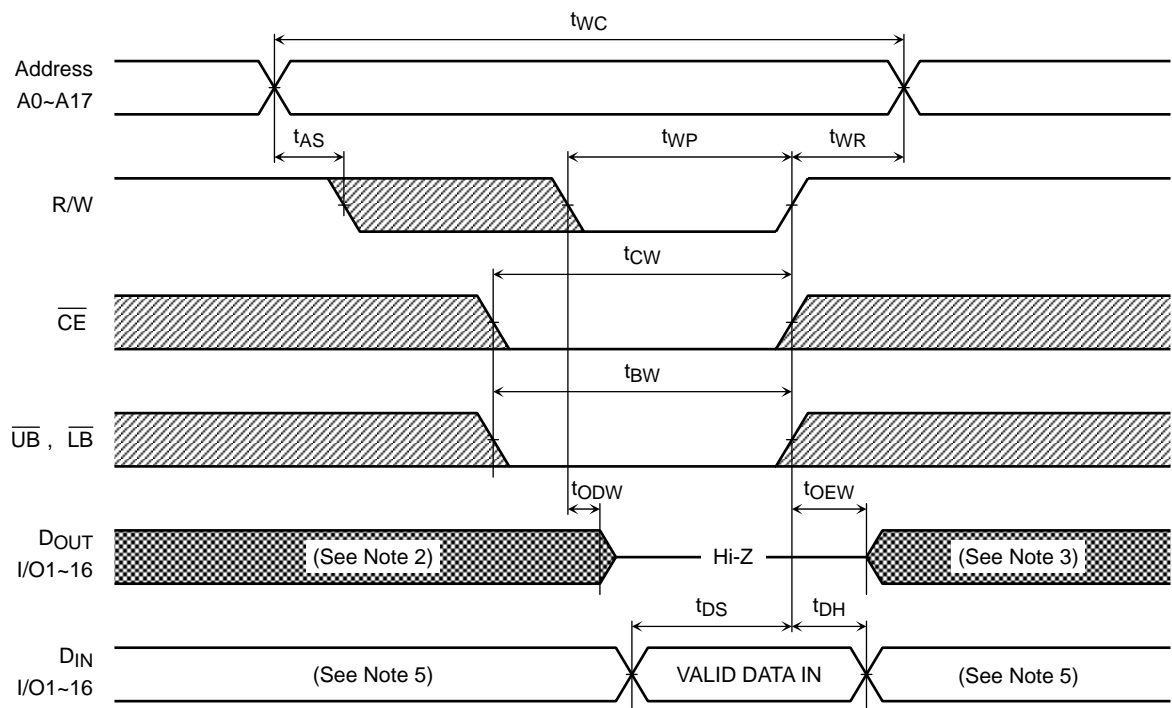
PARAMETER	TEST CONDITION
Input pulse level	0.4 V, 2.4 V
t _R , t _F	5 ns
Timing measurements	1.5 V
Reference level	1.5 V
Output load	100 pF + 1 TTL Gate

TIMING DIAGRAMS

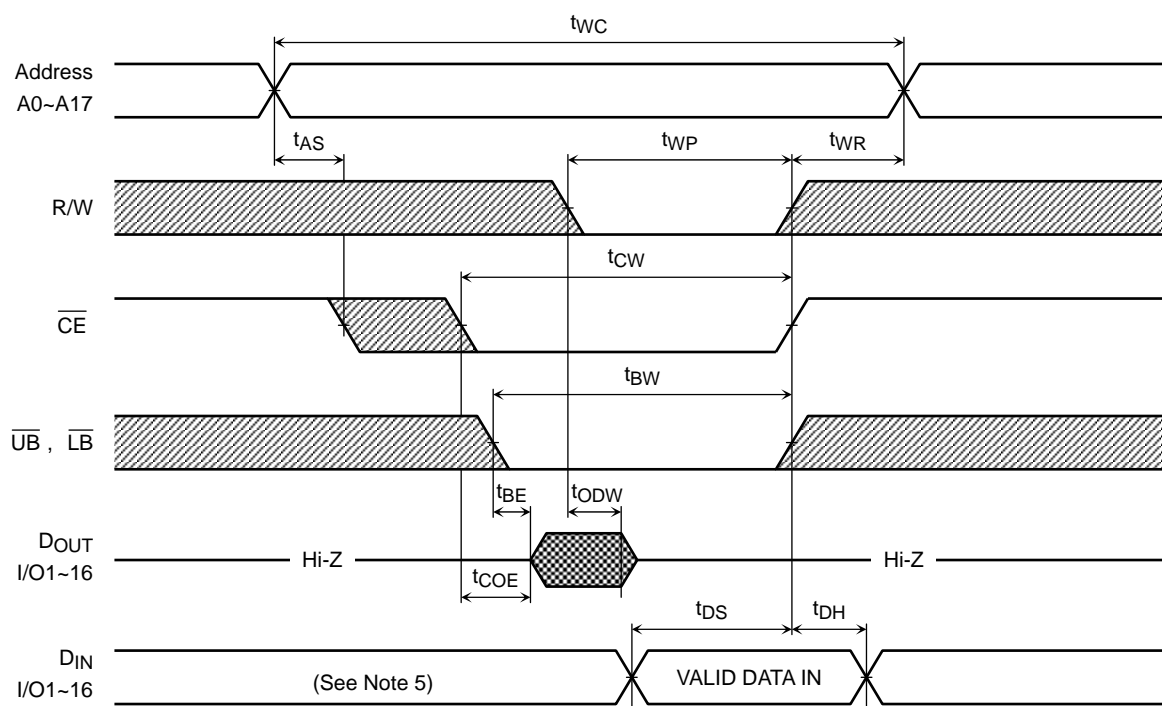
READ CYCLE (See Note 1)



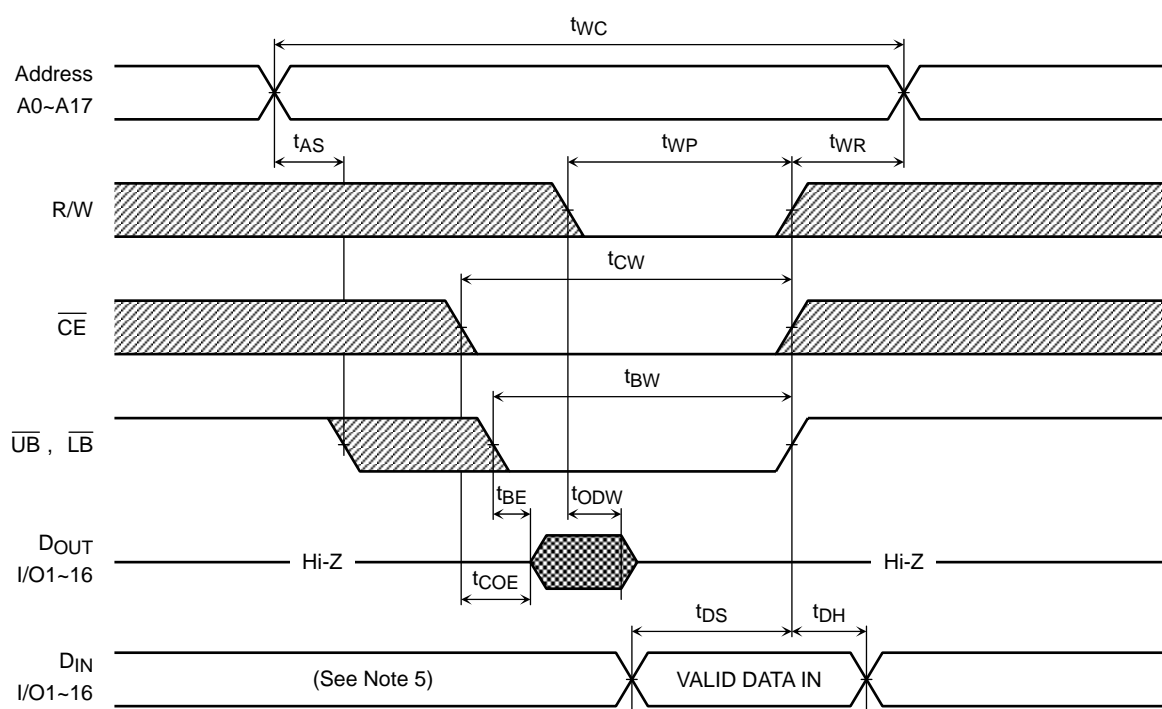
WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 ($\overline{\text{CE}}$ CONTROLLED) (See Note 4)



WRITE CYCLE 3 ($\overline{\text{UB}}$, $\overline{\text{LB}}$ CONTROLLED) (See Note 4)



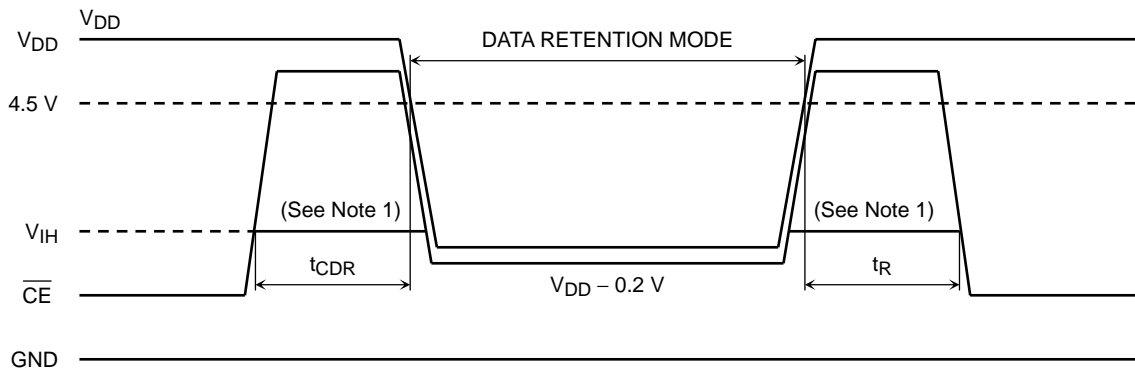
Note:

- (1) R/W remains HIGH for the read cycle.
- (2) If $\overline{\text{CE}}$ (or $\overline{\text{UB}}$ or $\overline{\text{LB}}$) goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.
- (3) If $\overline{\text{CE}}$ (or $\overline{\text{UB}}$ or $\overline{\text{LB}}$) goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
- (4) If $\overline{\text{OE}}$ is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

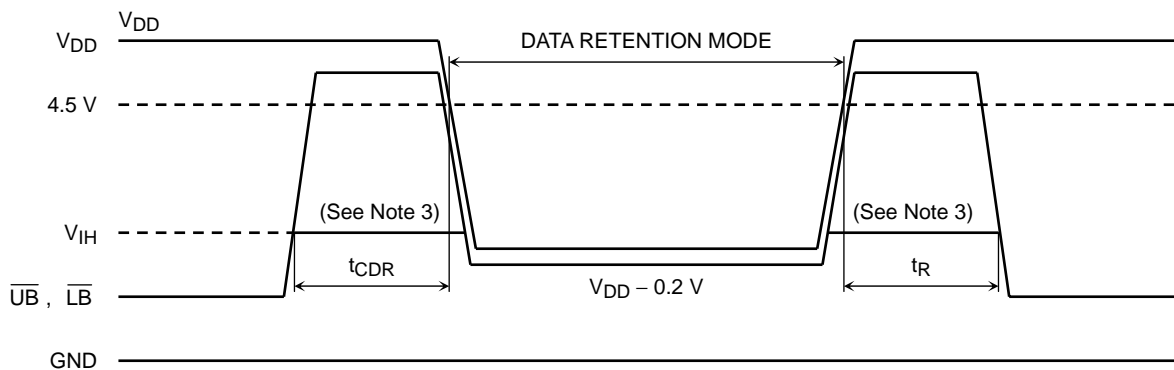
DATA RETENTION CHARACTERISTICS ($T_a = -40^\circ$ to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$T_a = -40 \sim 40^\circ\text{C}$	—	3	μA
		$T_a = -40 \sim 85^\circ\text{C}$	—	20	
t_{CDR}	Chip Deselect to Data Retention Mode Time	0	—	—	ns
t_{R}	Recovery Time	5	—	—	ms

$\overline{\text{CE}}$ CONTROLLED DATA RETENTION MODE



$\overline{\text{UB}}, \overline{\text{LB}}$ CONTROLLED DATA RETENTION MODE (See Note 2)



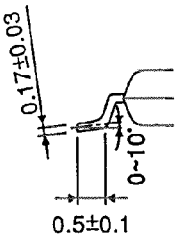
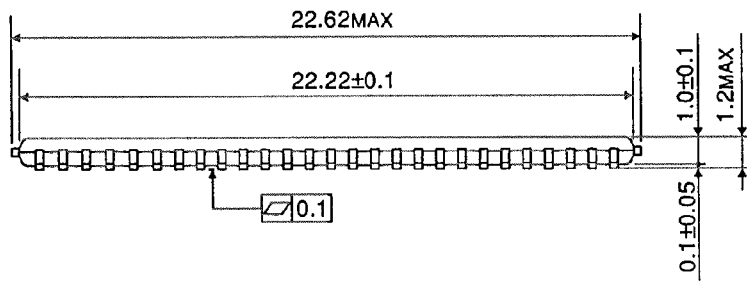
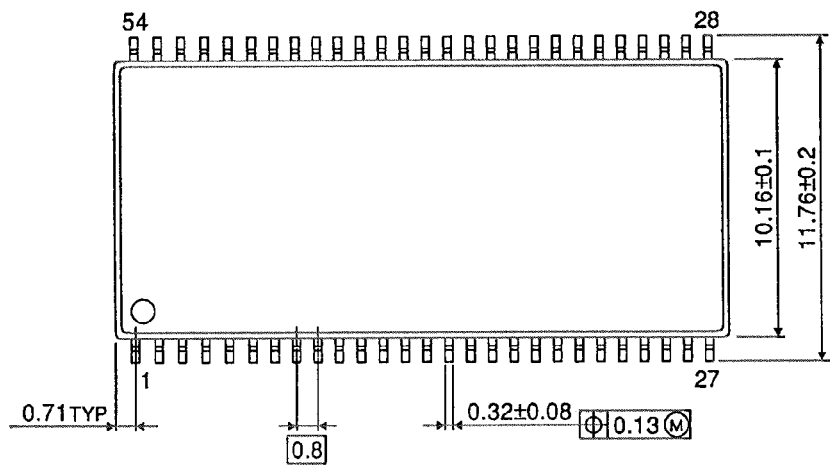
Note:

- (1) When \overline{CE} is operating at the $V_{IH}(\text{min.})$ level(2.2 V), the operating current is given by I_{DDS1} during the transition of V_{DD} from 4.5 to 2.4 V.
- (2) In \overline{UB} (or \overline{LB}) controlled data retention mode, minimum standby current mode is entered when $\overline{CE} \leq 0.2 \text{ V}$ or $\overline{CE} \geq V_{DD} - 0.2 \text{ V}$.
- (3) When \overline{UB} (or \overline{LB}) is operating at the $V_{IH}(\text{min.})$ level(2.2 V), the operating current is given by I_{DDS1} during the transition of V_{DD} from 4.5 to 2.4 V.

PACKAGE DIMENSIONS

TSOPII54-P-400-0.80

Unit: mm



Weight: g (typ)

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