

524,288 WORDS × 8 BIT STATIC RAM

**DESCRIPTION**

The TC554001AFI/AFTI/ATRI is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single  $5V \pm 10\%$  power supply. Advanced circuit technology provides both high speed and low power at an operating current of 10mA/MHz(typ) and minimum cycle time of 70 ns. It is automatically placed in low-power mode at  $2 \mu A$  standby current (typ) when chip enable ( $\overline{CE}$ ) is asserted high. There are two control inputs.  $\overline{CE}$  is used to select the device and for data retention control, and output enable ( $\overline{OE}$ ) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of  $-40^\circ$  to  $85^\circ C$ , the TC554001AFI/AFTI/ATRI can be used in environments exhibiting extreme temperature conditions. The TC554001AFI/AFTI/ATRI is available in a standard plastic 32-pin small-outline package(SOP) and normal and reverse pinout plastic 32-pin thin-small-outline package(TSOP).

**FEATURES**

- Low-power dissipation  
Operating: 55 mW/MHz (typical)
- Single power supply voltage of  $5V \pm 10\%$
- Power down features using  $\overline{CE}$
- Data retention supply voltage of 2.0 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of  $-40^\circ$  to  $85^\circ C$
- Standby Current (maximum) :

	TC554001AFI/AFTI/ATRI	
	-70, -85, -10	-75L, -85L, -10L
5.5V	200 $\mu A$	100 $\mu A$
3.0V	100 $\mu A$	50 $\mu A$

- Access Time (maximum)

	TC554001AFI/AFTI/ATRI		
	-70, -70L	-85, -85L	-10, -10L
Access Time	70 ns	85 ns	100 ns
$\overline{CE}$ Access Time	70 ns	85 ns	100 ns
$\overline{OE}$ Access Time	35 ns	45 ns	50 ns

- Package:  
SOP32-P-525-1.27 (AFI) (Weight: 1.14g typ)  
TSOP  $\Pi$  32-P-400-1.27 (AFTI) (Weight: 0.53g typ)  
TSOP  $\Pi$  32-P-400-1.27A (ATRI) (Weight: 0.53g typ)

**PIN ASSIGNMENT (TOP VIEW)**

○ 32 PIN AFI/AFTI    ○ 32 PIN ATRI

A18	1	32	$V_{DD}$	32	1	A18
A16	2	31	A15	31	2	A16
A14	3	30	A17	30	3	A14
A12	4	29	R/W	29	4	A12
A7	5	28	A13	28	5	A7
A6	6	27	A8	27	6	A6
A5	7	26	A9	26	7	A5
A4	8	25	A11	25	8	A4
A3	9	24	$\overline{OE}$	24	9	A3
A2	10	23	A10	23	10	A2
A1	11	22	$\overline{CE}$	22	11	A1
A0	12	21	I/O8	21	12	A0
I/O1	13	20	I/O7	20	13	I/O1
I/O2	14	19	I/O6	19	14	I/O2
I/O3	15	18	I/O5	18	15	I/O3
GND	16	17	I/O4	17	16	GND

**PIN NAMES**

A0 to A18	Address Inputs
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
I/O1 to I/O8	Data Input/Output
$V_{DD}$	Power (+ 5 V)
GND	Ground

000707EBA2

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

The diagram illustrates the internal architecture of a 256K DRAM. At the top center is the **MEMORY CELL ARRAY**, specified as  $2048 \times 256 \times 8$  (4194304). To its left are three vertical blocks: **ROW ADDRESS DECODER**, **ROW ADDRESS REGISTER**, and **ROW ADDRESS BUFFER**. These are connected to address lines **A0** through **A18** on the far left. A **CE** (Chip Enable) input is shown at the top right, connected to the decoder and register. Below the memory array is a stack of four blocks: **SENSE AMP**, **COLUMN ADDRESS DECODER**, **COLUMN ADDRESS REGISTER**, and **COLUMN ADDRESS BUFFER**. These are connected to address lines **A8** through **A17** at the bottom. A **CE** input is also shown at the bottom right, connected to the column address buffer. To the left of these blocks are control lines **I/O1** and **I/O8**, and a **DATA CONTROL** block. A **CLOCK GENERATOR** block is connected to the **DATA CONTROL** block and the **COLUMN ADDRESS REGISTER**. At the bottom left, there are control lines **OE** (Output Enable), **R/W** (Read/Write), and **CE** (Chip Enable), which are connected to the **DATA CONTROL** block and the **CLOCK GENERATOR**. On the far right, there are power supply lines **V<sub>DD</sub>** and **GND**. The diagram shows a complex network of data and control lines connecting all these components.

OPERATION MODE	$\overline{\text{CE}}$	$\overline{\text{OE}}$	R/W	I/O1 to I/O8	POWER
Read	L	L	H	D <sub>OUT</sub>	I <sub>DDO</sub>
Write	L	x	L	D <sub>IN</sub>	I <sub>DDO</sub>
Output Disabled	L	H	H	High-Z	I <sub>DDO</sub>
Standby	H	x	x	High-Z	I <sub>DDs</sub>

SYMBOL	RATING	VALUE	UNIT
V <sub>DD</sub>	Power Supply Voltage	– 0.3 to 7.0	V
V <sub>IN</sub>	Input Voltage	– 0.3* to 7.0	V
V <sub>I/O</sub>	Input and Output Voltage	– 0.5 to V <sub>DD</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	0.6	W
T <sub>solder</sub>	Soldering Temperature (10 s)	260	°C
T <sub>strg.</sub>	Storage Temperature	– 55 to 150	°C
T <sub>opr.</sub>	Operating Temperature	– 40 to 85	°C

**DC RECOMMENDED OPERATING CONDITIONS** ( $T_a = -40^\circ$  to  $85^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$V_{DD}$	Power Supply Voltage	4.5	5.0	5.5	V
$V_{IH}$	Input High Voltage	2.4	–	$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$-0.3^*$	–	0.6	V
$V_{DH}$	Data Retention Supply Voltage	2.0	–	5.5	V

\*  $-3.0\text{ V}$  when measured at a pulse width of 50 ns**DC CHARACTERISTICS** ( $T_a = -40^\circ$  to  $85^\circ\text{C}$ ,  $V_{DD} = 5\text{ V} \pm 10\%$ )

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT	
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V to V <sub>DD</sub>			–	–	± 1.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4 V			– 1.0	–	–	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V			2.1	–	–	mA	
I <sub>LO</sub>	Output Leakage Current	CE = V <sub>IH</sub> or R/W = V <sub>IL</sub> or OE = V <sub>IH</sub> V <sub>OUT</sub> = 0 V to V <sub>DD</sub>			–	–	± 1.0	μA	
I <sub>DDO1</sub>	Operating Current	CE = V <sub>IL</sub> and R/W = V <sub>IH</sub> I <sub>OUT</sub> = 0 mA Other Inputs = V <sub>IH</sub> /V <sub>IL</sub>		T <sub>cycle</sub>	min	–	–	70	mA
					1 μs	–	15	–	
I <sub>DDO2</sub>		CE = 0.2 V and R/W = V <sub>DD</sub> –0.2 V I <sub>OUT</sub> = 0 mA Other Inputs = V <sub>DD</sub> –0.2 V/0.2 V		T <sub>cycle</sub>	min	–	–	60	mA
					1 μs	–	10	–	
I <sub>DDS1</sub>	Standby Current	CE = V <sub>IH</sub>			–	–	3	mA	
I <sub>DDS2</sub>		CE = V <sub>DD</sub> –0.2 V V <sub>DD</sub> = 2.0 to 5.5 V	-70, -85, -10	Ta = 25°C		–	2	–	μA
				Ta = –40° to 85°C		–	–	200	
			-70L, -85L, -10L	Ta = 25°C		–	2	5	
				Ta = –40° to 85°C		–	–	100	

**CAPACITANCE** ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = \text{GND}$	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

**AC CHARACTERISTICS AND OPERATING CONDITIONS** ( $T_a = -40^\circ$  to  $85^\circ\text{C}$ ,  $V_{DD} = 5\text{V} \pm 10\%$ )

**READ CYCLE**

SYMBOL	PARAMETER	TC554001AFI/AFTI/ATRI						UNIT
		-70, -70L		-85, -85L		-10, -10L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Read Cycle Time	70	–	85	–	100	–	ns
t <sub>ACC</sub>	Address Access Time	–	70	–	85	–	100	
t <sub>CO</sub>	Chip Enable Access Time	–	70	–	85	–	100	
t <sub>OE</sub>	Output Enable Access Time	–	35	–	45	–	50	
t <sub>COE</sub>	Chip Enable Low to Output Active	5	–	5	–	5	–	
t <sub>OEE</sub>	Output Enable Low to Output Active	0	–	0	–	0	–	
t <sub>OD</sub>	Chip Enable High to Output High-Z	–	30	–	35	–	40	
t <sub>ODO</sub>	Output Enable High to Output High-Z	–	30	–	35	–	40	
t <sub>OH</sub>	Output Data Hold Time	10	–	10	–	10	–	

**WRITE CYCLE**

SYMBOL	PARAMETER	TC554001AFI/AFTI/ATRI						UNIT
		-70, -70L		-85, -85L		-10, -10L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>WC</sub>	Write Cycle Time	70	–	85	–	100	–	ns
t <sub>WP</sub>	Write Pulse Width	50	–	55	–	60	–	
t <sub>CW</sub>	Chip Enable to End of Write	60	–	70	–	80	–	
t <sub>AS</sub>	Address Setup Time	0	–	0	–	0	–	
t <sub>WR</sub>	Write Recovery Time	0	–	0	–	0	–	
t <sub>ODW</sub>	R/W Low to Output High-Z	–	30	–	35	–	40	
t <sub>OEW</sub>	R/W Hige to Output Active	0	–	0	–	0	–	
t <sub>DS</sub>	Data Setup Time	30	–	35	–	40	–	
t <sub>DH</sub>	Data Hold Time	0	–	0	–	0	–	

**AC TEST CONDITIONS**

Output Load: 100 pF + one TTL gate

Input Pulse Level: 0.4 V, 2.6 V

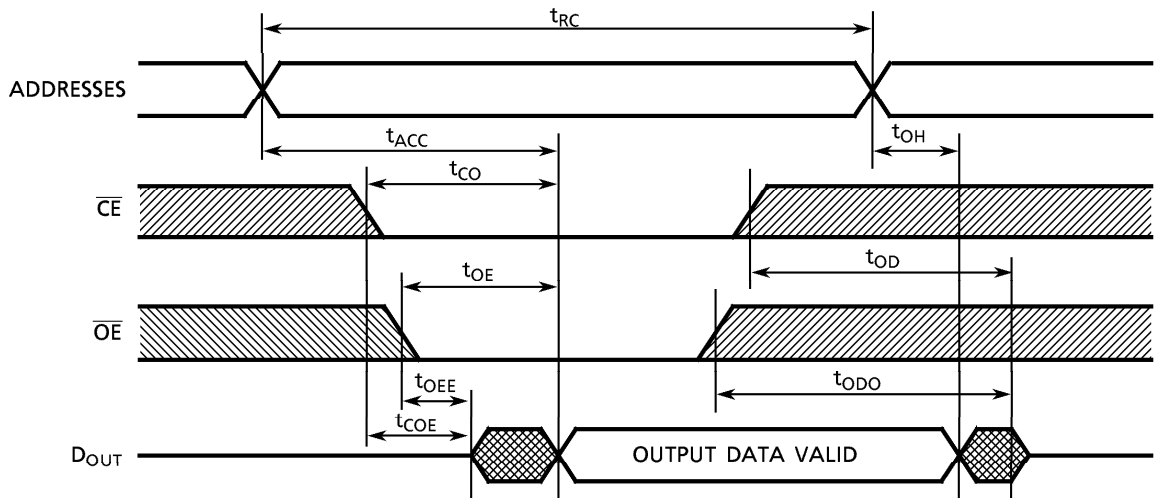
Timing Measurements: 1.5 V

Reference Level: 1.5 V

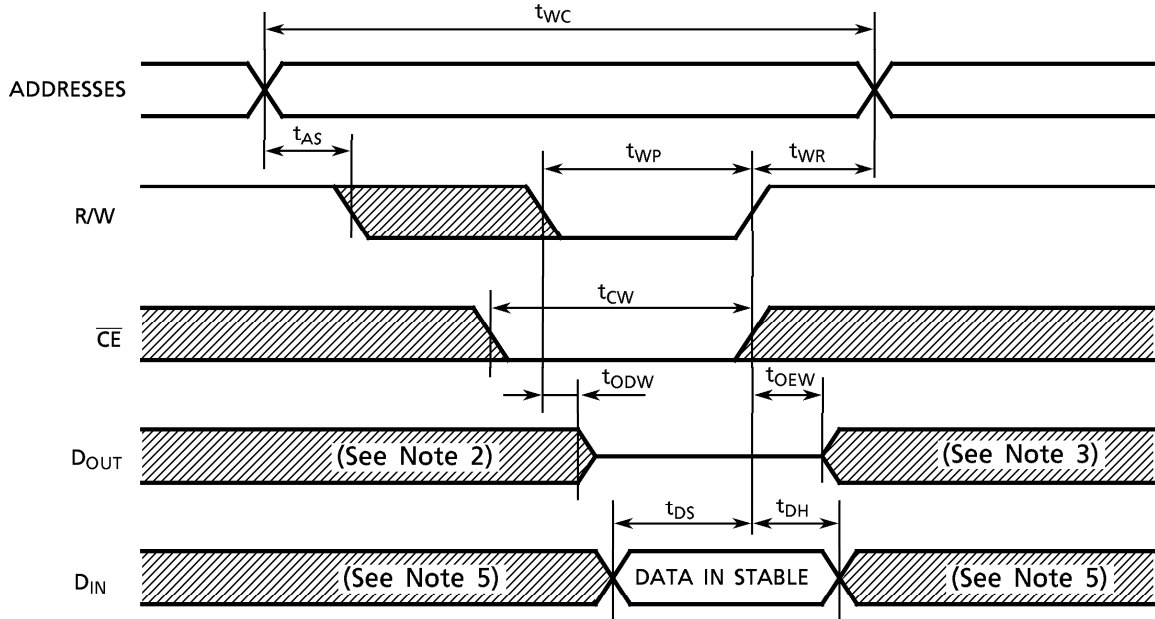
$t_r, t_F$ : 5 ns

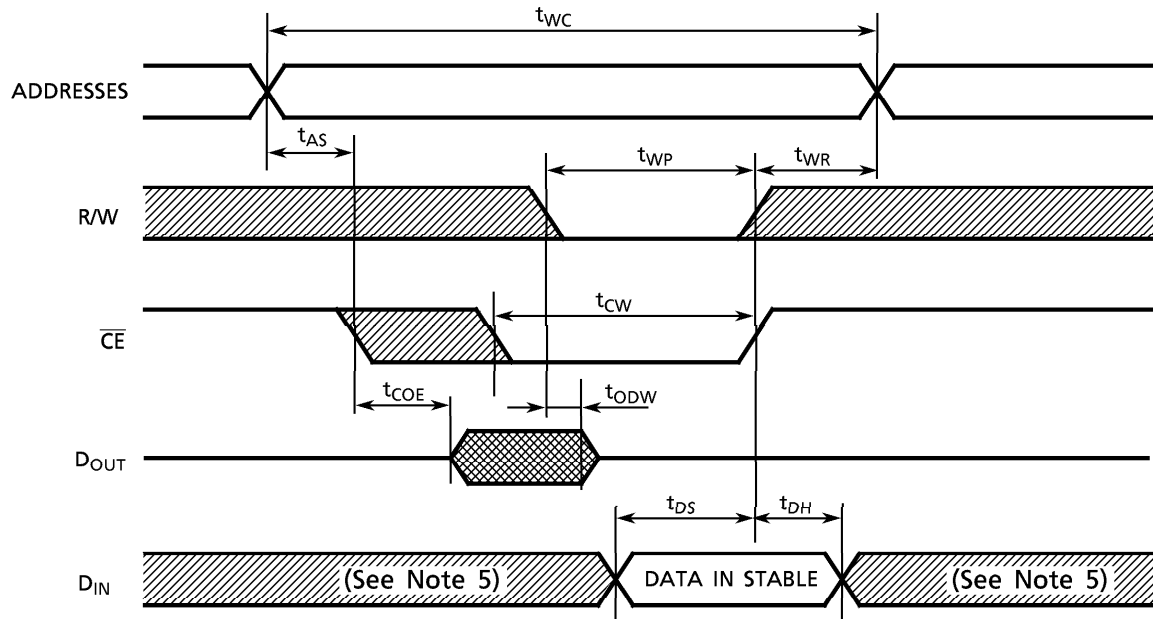
TIMING WAVEFORMS

READ CYCLE (See Note 1)



WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



**WRITE CYCLE 2 ( $\overline{\text{CE}}$  CONTROLLED)** (See Note 4)


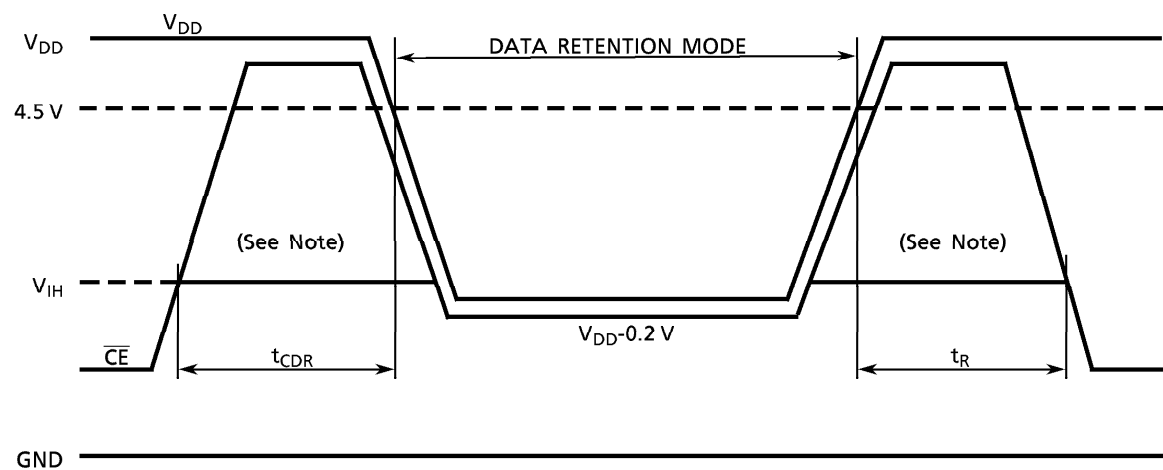
- (1) R/W remains High for Read Cycle.
- (2) If  $\overline{\text{CE}}$  goes coincident with or after R/W goes LOW, the output will remain at high impedance.
- (3) If  $\overline{\text{CE}}$  goes HIGH coincident with or before R/W goes HIGH, the output will remain at high impedance.
- (4) IF  $\overline{\text{CE}}$  is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)

SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
V <sub>DH</sub>	Data Retention Supply Voltage			2.0	–	5.5	V
I <sub>DDS2</sub>	Standby Current	-70, -85, -10	V <sub>DH</sub> = 3.0 V	–	–	100	μA
			V <sub>DH</sub> = 5.5 V	–	–	200	
		-70L, -85L, -10L	V <sub>DH</sub> = 3.0 V	–	–	50*	
			V <sub>DH</sub> = 5.5 V	–	–	100	
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode Time			0	–	–	nS
t <sub>R</sub>	Recovery Time			5	–	–	mS

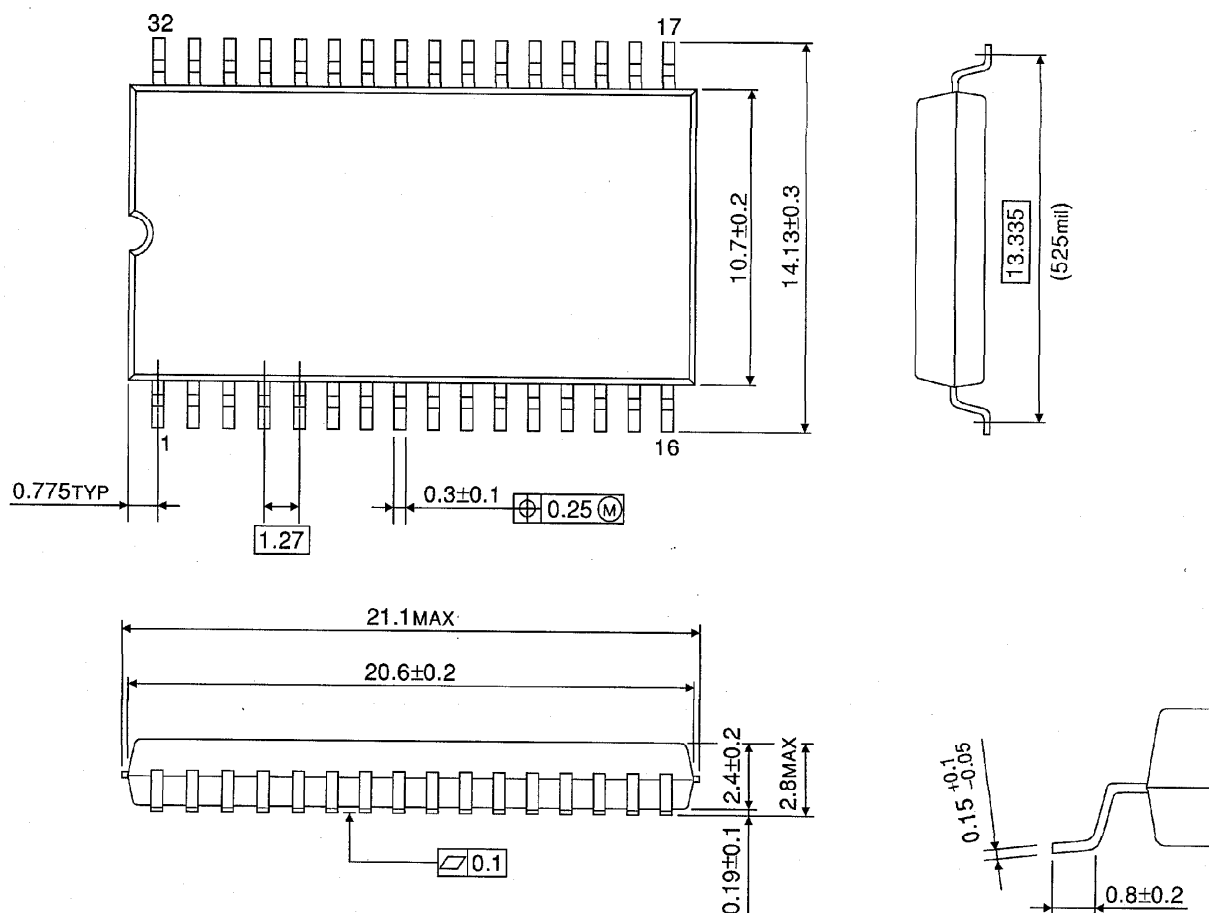
\* 5 μA (max) at Ta = -40° to 40°C

$\overline{CE}$  Controlled Data Retention Mode



Note: When  $\overline{CE}$  is operating at the  $V_{IH}$  level (2.4V), the standby current is given by  $I_{DDS1}$  during the transition of  $V_{DD}$  from 4.5 to 2.6V.

## Unit in mm

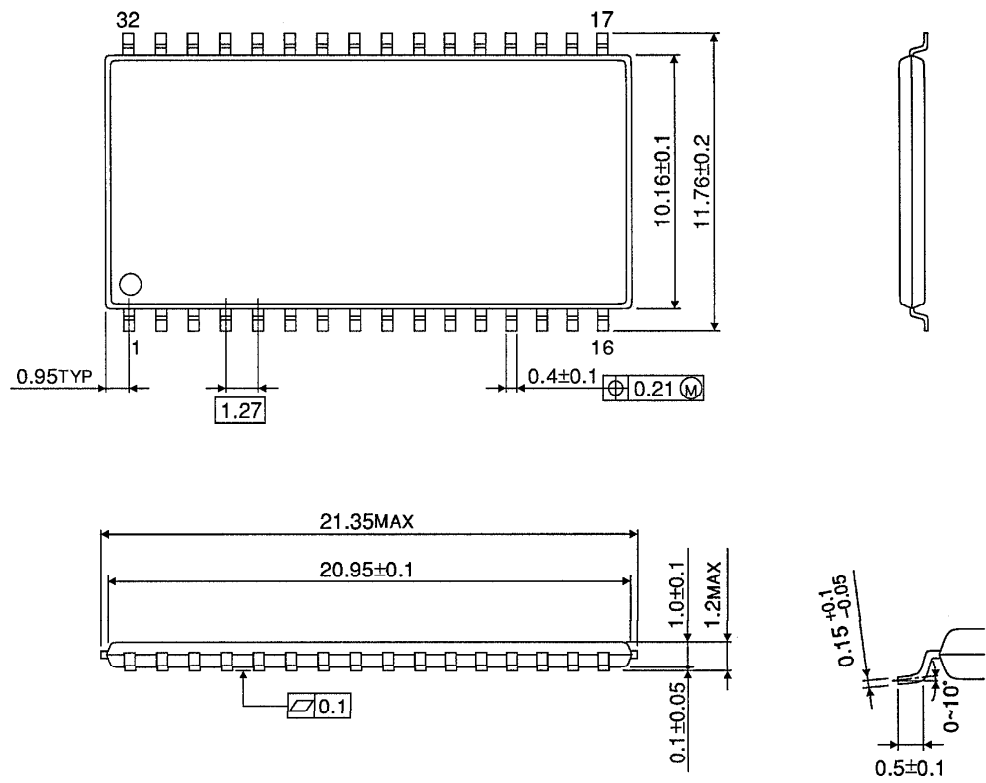


Weight: 1.14g (typ)



PACKAGE DIMENSIONS (TSOPII 32-P-400-1.27)

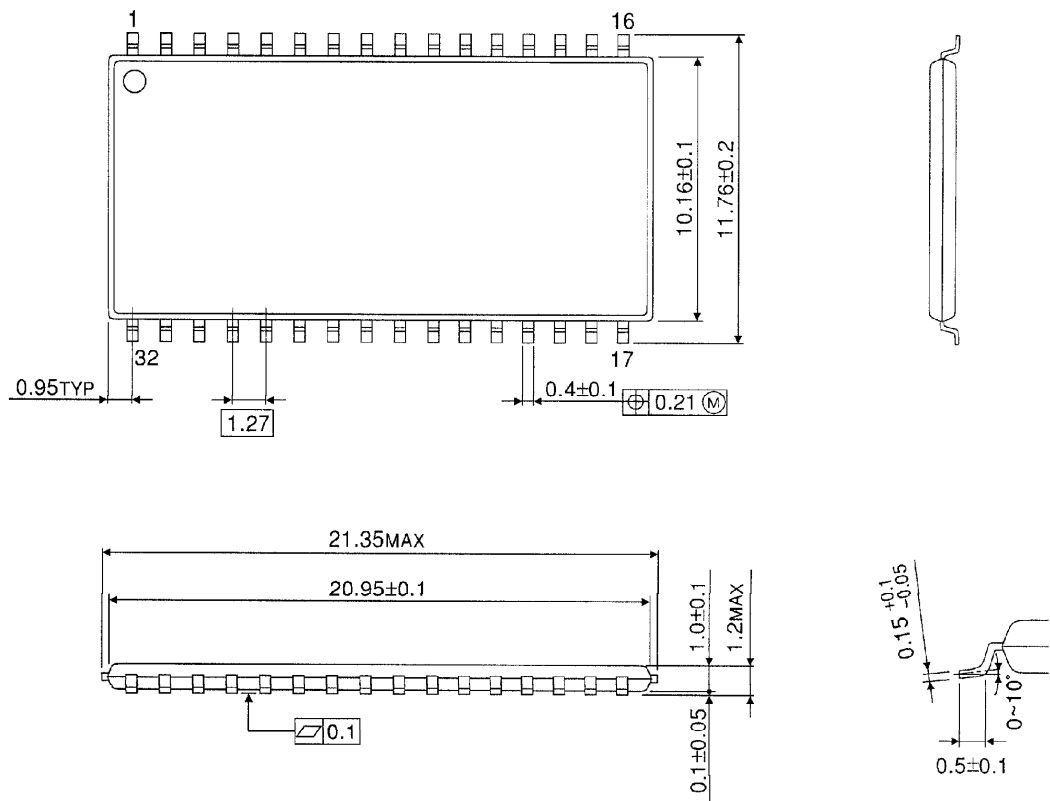
Unit in mm



Weight: 0.53g (typ)

PACKAGE DIMENSIONS (TSOPII 32-P-400-1.27A)

Unit in mm



Weight: 0.53g (typ)