

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7SET00F, TC7SET00FU

2-INPUT NAND GATE

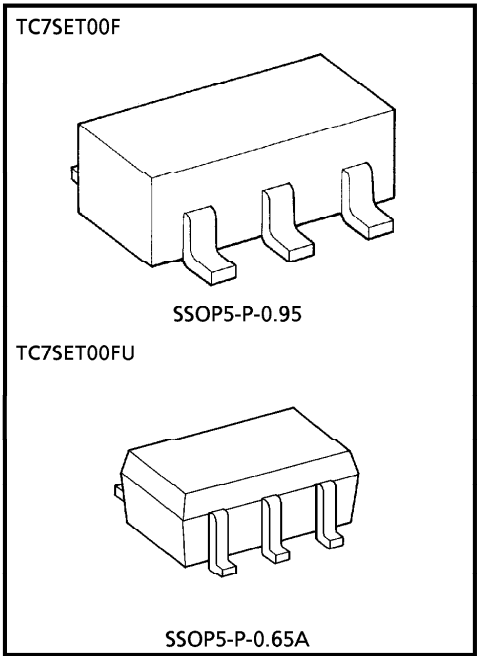
The TC7SET00 is an advanced high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The input threshold levels are compatible with TTL output voltage. This device can be used for level converter for interfacing 3V to 5V system. An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage.

FEATURES

- High Speed $t_{pd} = 5.0ns$ (Typ.) at $V_{CC} = 5V$
- Low Power Dissipation $I_{CC} = 2\mu A$ (Max.) at $T_a = 25^{\circ}C$
- Compatible with TTL outputs $V_{IL} = 0.8V$ (Max.)
 $V_{IH} = 2.0V$ (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays $t_{pLH} \approx t_{pHL}$

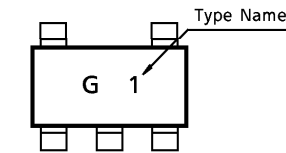
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~7.0	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} /Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	200	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature (10 s)	T_L	260	°C



Weight SSOP5-P-0.95 : 0.016g (Typ.)
SSOP5-P-0.65A : 0.006g (Typ.)

MARKING



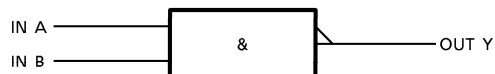
TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

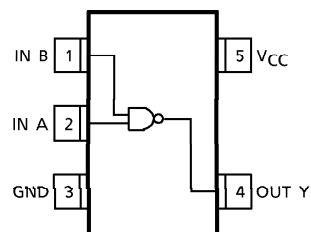
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LOGIC DIAGRAM



PIN ASSIGNMENT (TOP VIEW)



RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt/dv	0~20	ns/V

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}		4.5~5.5	2.0	—	—	2.0	—	V
Low-Level Input Voltage	V_{IL}		4.5~5.5	—	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu\text{A}$	4.5	4.4	4.5	—	4.4	V
			$I_{OH} = -8\text{mA}$	4.5	3.94	—	—	3.80	
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$	$I_{OL} = 50\mu\text{A}$	4.5	—	0.0	0.10	—	V
			$I_{OL} = 8\text{mA}$	4.5	—	—	0.36	—	
Input Leakage Current	I_{IN}	$V_{IN} = 5.5\text{V}$ or GND	0~5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	2.0	—	20.0	μA
	I_{CCT}	PER INPUT : $V_{IN} = 3.4\text{V}$ OTHER INPUT: V_{CC} or GND	5.5	—	—	1.35	—	1.50	mA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = - 40~85°C		UNIT
		VCC (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	tPLH	5.0 ± 0.5	15	—	5.0	6.9	1.0	8.0	ns
	tPHL		50	—	5.5	7.9	1.0	9.0	
Input Capacitance	CIN			—	4	10	—	10	pF
Power Dissipation Capacitance	CpD	(Note 1)		—	17	—	—	—	

(Note 1) : CpD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :
 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

INPUT EQUIVALENT CIRCUIT

