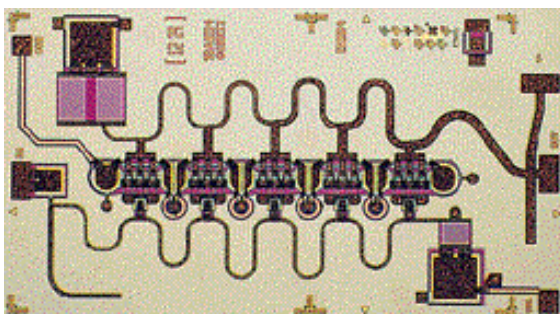


2 - 20 GHz Power Amplifier**TGA8334-SCC****Key Features and Performance**

- 2 to 20 GHz Frequency Range
- 0.4-W Output Power at 1 dB Gain Compression at Midband
- Positive Gain Slope Across Frequency
- On-Chip Input DC-Blocking Capacitor
- 1.8:1 Input SWR at Midband, 1.3:1 Output SWR at Midband
- 8 dB Gain with +/- 1 dB Flatness
- 3.1750 x 1.808 x 0.1524 mm (0.125 x 0.071 x 0.006 in.)

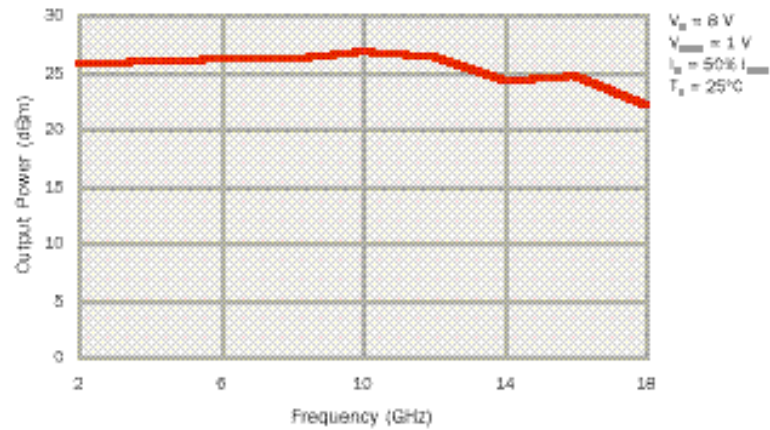
Description

The TriQuint TGA8334-SCC is a GaAs monolithic dual-gate distributed amplifier. Small-signal gain is typically 8 dB with positive gain slope across the band. Input and output return loss is typically greater than 9.7 dB. Five 600um gatewidth FETs provide more than 26 dB output power at 1 dB gain compression at midband. Ground is provided to the circuitry through vias to the backside metallization.

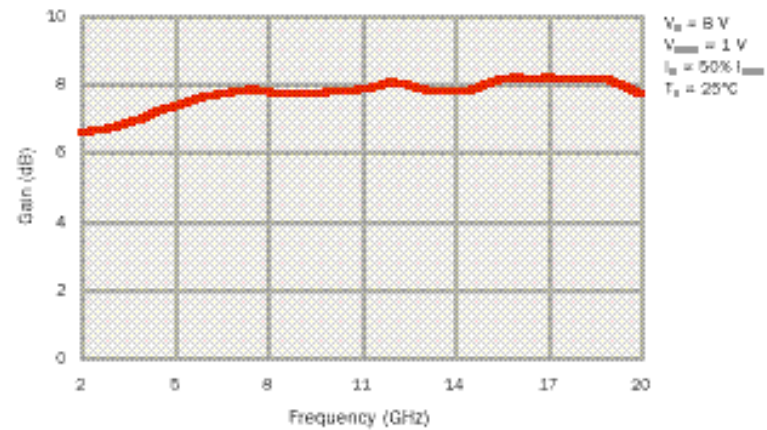
The TGA8334-SCC is directly cascadable with other broadband TriQuint GaAs amplifiers, such as the TGA8300-SCC, TGA8622-SCC, and TGA8220-SCC. This general power amplifier is suitable for a variety of wide-band applications such as distributed networks, logging stages and oscillator buffers.

Bond pad and backside metallization is gold plated for compatibility with eutectic alloy attachment methods as well as the thermocompression and thermosonic wire bonding processes. The TGA8334-SCC is supplied in chip form and is readily assembled using automated equipment.

**TYPICAL
OUTPUT POWER**
 P_{1dB}



**TYPICAL
SMALL-SIGNAL
POWER GAIN**



**TYPICAL
RETURN LOSS**

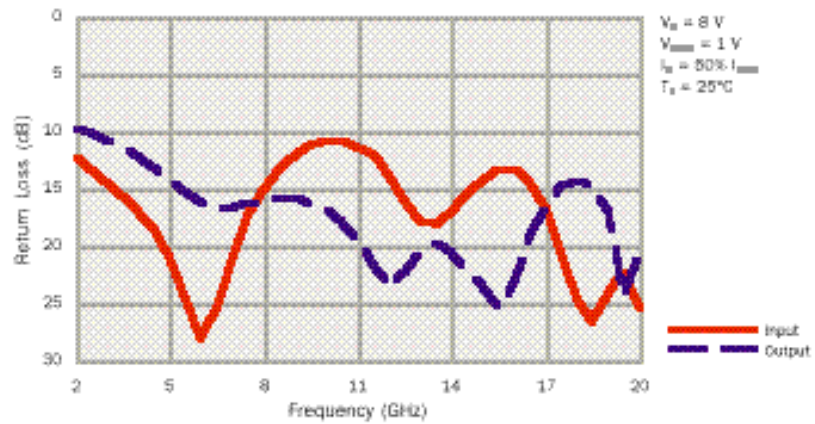


TABLE I
MAXIMUM RATINGS

SYMBOL	PARAMETER	VALUE
V^+	POSITIVE SUPPLY VOLTAGE	9V
I^+	POSITIVE SUPPLY CURRENT	I_{DSS}
V^-	NEGATIVE SUPPLY VOLTAGE	-5V to 0V
I^-	NEGATIVE SUPPLY CURRENT	-29.1mA
V_{CTRL}	GAIN CONTROL VOLTAGE RANGE	-5V to 4V
$V_{CTRL} - V^+$	GAIN CONTROL VOLTAGE RANGE WITH RESPECT TO POSITIVE SUPPLY VOLTAGE	0V to -10V
P_D	POWER DISSIPATION, AT (OR BELOW) 25°C BASE-PLATE TEMPERATURE *	7W
P_{IN}	INPUT CONTINUOUS WAVE POWER	27dBm
T_{CH}^{**}	OPERATING CHANNEL TEMPERATURE	150 °C
T_M	MOUNTING TEMPERATURE (30 SECONDS)	320 °C
T_{STG}	STORAGE TEMPERATURE	-65 to 150 °C

Ratings over channel temperature range, T_{CH} (unless otherwise noted)

Stresses beyond those listed under “Maximum Ratings” may cause permanent damage to the device.

These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “RF Specifications” is not implied. Exposure to maximum rated conditions for extended periods may affect device reliability.

*For operation above 25°C base-plate temperature, derate linearly at the rate of 15.2mW/°C.

** Operating channel temperature, T_{CH} , directly affects the device MTTF. For maximum life, it is recommended that channel temperature be maintained at the lowest possible level.

TABLE II
DC PROBE TESTS (100%)
($T_A = 25\text{ }^{\circ}\text{C} \pm 5\text{ }^{\circ}\text{C}$)

NOTES	SYMBOL	TEST CONDITIONS <u>6</u> /	LIMITS		UNITS
			MIN	MAX	
<u>2</u> /	I_{DSS}	STD	630	1170	mA
<u>2</u> /	G_m	STD	300	600	mS
<u>1</u> /, <u>3</u> /, <u>7</u> /	$ V_{P1} $	STD	2.3	4.1	V
<u>1</u> /, <u>4</u> /, <u>7</u> /	$ V_{P2} $	STD	2.3	4.1	V
<u>1</u> /, <u>2</u> /, <u>5</u> /	$ V_{BVG D} $	STD	8	30	V
<u>1</u> /, <u>2</u> /, <u>5</u> /	$ V_{BVG S} $	STD	8	30	V

- 1/ V_P , $V_{BVG D}$, and $V_{BVG S}$ are negative.
- 2/ Checked for all 5 FETs in parallel.
- 3/ Pinch off voltage for Gate-1 for all FETs in parallel.
- 4/ Pinch off voltage for Gate-2 for all FETs in parallel.
- 5/ Breakdown measurements tested at 1 mA/mm with a 35 V compliance limit.
- 6/ The measurement conditions are subject to change at the manufacture's discretion (with appropriate notification to the buyer).
- 7/ $|V_{P1}|$ and $|V_{P2}|$, alternatively, may be referred to as V_{P1} and V_{P2} , respectively.
- 8/ STD refers to Standard Test Conditions, see Table IV

TABLE III
 RF SPECIFICATIONS
 ($T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$)
 $V^+ = 8\text{V}$, $I^+ = 50\% I_{DSS}$, $V_{G2} = 1.0\text{V}$

TEST	MEASUREMENT CONDITIONS	VALUE			UNITS
		MIN	TYP	MAX	
GAIN	F = 2 – 6 GHz	4.0	8.0		dB
	F = 6 – 20 GHz	5.0	8.0		dB
GAIN FLATNESS	F = 2 – 20 GHz		±1		dB
POWER OUTPUT AT 1 dB GAIN COMPRESSION	F = 2 – 14 GHz	24	26		dBm
	F = 14 – 18 GHz	21	25		dBm
INPUT RETURN LOSS MAGNITUDE	F = 2 – 20 GHz	10	14		dB
OUTPUT RETURN LOSS MAGNITUDE	F = 2 – 18 GHz	7.4	16.5		dB
	F = 18 – 20 GHz	6.0	16.5		dB
INPUT STANDING WAVE RATIO	F = 2 GHz		1.6:1		
	F = 9 GHz		1.7:1		
	F = 18 GHz		1.1:1		
OUTPUT STANDING WAVE RATIO	F = 2 GHz		2.0:1		
	F = 9 GHz		1.4:1		
	F = 18 GHz		1.5:1		
OUTPUT THIRD- ORDER INTERCEPT POINT	F = 2 GHz		38		dBm
	F = 9 GHz		41		dBm
	F = 18 GHz		38		dBm

TABLE IV
AUTOPROBE FET PARAMETER MEASUREMENT CONDITONS

FET Parameters	Test Conditions
I_{DSS} : Maximum drain current (I _{DS}) with gate voltage (V _{GS}) at zero volts.	V _{GS} = 0.0 V, drain voltage (V _{DS}) is swept from 0.5 V up to a maximum of 3.5 V in search of the maximum value of I _{DS} ; voltage for I _{DSS} is recorded as VDSP.
G_m : Transconductance; $\frac{(I_{DSS} - IDS1)}{VG1}$	For all material types, V _{DS} is swept between 0.5 V and VDSP in search of the maximum value of I _{ds} . This maximum I _{DS} is recorded as IDS1. For Intermediate and Power material, IDS1 is measured at V _{GS} = VG1 = -0.5 V. For Low Noise, HFET and pHEMT material, V _{GS} = VG1 = -0.25 V. For LNBECOLC, use V _{GS} = VG1 = -0.10 V.
V_P : Pinch-Off Voltage; V _{GS} for I _{DS} = 0.5 mA/mm of gate width.	V _{DS} fixed at 2.0 V, V _{GS} is swept to bring I _{DS} to 0.5 mA/mm.
V_{BVGD} : Breakdown Voltage, Gate-to-Drain; gate-to-drain breakdown current (I _{BD}) = 1.0 mA/mm of gate width.	Drain fixed at ground, source not connected (floating), 1.0 mA/mm forced into gate, gate-to-drain voltage (V _{GD}) measured is V _{BVGD} and recorded as BVGD; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.
V_{BVGS} : Breakdown Voltage, Gate-to-Source; gate-to-source breakdown current (I _{BS}) = 1.0 mA/mm of gate width.	Source fixed at ground, drain not connected (floating), 1.0 mA/mm forced into gate, gate-to-source voltage (V _{GS}) measured is V _{BVGS} and recorded as BVGS; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.

TYPICAL S-PARAMETERS

Frequency (GHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂		GAIN (dB)
	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	
0.5	0.62	-67	2.156	154	0.001	42	0.36	-170	6.7
1.0	0.40	-103	2.092	143	0.001	65	0.35	171	6.4
1.5	0.30	-126	2.110	128	0.002	81	0.34	159	6.5
2.0	0.24	-146	2.132	113	0.003	80	0.33	150	6.6
2.5	0.21	-163	2.156	96	0.004	75	0.31	140	6.7
3.0	0.19	-180	2.181	80	0.005	66	0.29	133	6.8
3.5	0.16	166	2.213	63	0.006	56	0.27	126	6.9
4.0	0.14	151	2.241	47	0.007	46	0.24	120	7.0
4.5	0.12	138	2.294	30	0.008	32	0.22	116	7.2
5.0	0.09	128	2.338	12	0.009	18	0.19	115	7.4
5.5	0.06	125	2.374	-6	0.009	3	0.17	115	7.5
6.0	0.04	149	2.408	-24	0.009	-14	0.15	118	7.6
6.5	0.05	-178	2.431	-42	0.009	-27	0.15	122	7.7
7.0	0.09	-172	2.459	-61	0.009	-47	0.15	124	7.8
7.5	0.14	178	2.471	-79	0.008	-66	0.15	126	7.9
8.0	0.18	165	2.458	-98	0.008	-83	0.16	125	7.8
8.5	0.22	151	2.444	-117	0.008	-100	0.16	123	7.8
9.0	0.25	136	2.432	-135	0.009	-117	0.16	120	7.7
9.5	0.27	122	2.430	-153	0.010	-134	0.16	115	7.7
10.0	0.29	107	2.451	-172	0.011	-150	0.14	109	7.8
10.5	0.29	93	2.465	170	0.012	-165	0.13	104	7.8
11.0	0.27	81	2.470	151	0.013	176	0.11	97	7.9
11.5	0.25	69	2.492	132	0.014	155	0.08	98	7.9
12.0	0.20	59	2.532	111	0.014	133	0.07	115	8.1
12.5	0.16	57	2.521	90	0.012	107	0.08	134	8.0
13.0	0.13	64	2.471	70	0.007	89	0.09	133	7.9
13.5	0.12	74	2.446	51	0.004	89	0.10	123	7.8
14.0	0.14	80	2.447	31	0.003	133	0.09	114	7.8
14.5	0.17	83	2.457	10	0.006	134	0.08	108	7.8
15.0	0.19	71	2.507	-11	0.007	110	0.07	107	8.0
15.5	0.22	56	2.557	-34	0.007	80	0.05	124	8.2
16.0	0.21	38	2.572	-57	0.007	40	0.07	150	8.2
16.5	0.19	18	2.563	-80	0.005	1	0.11	153	8.2
17.0	0.14	-6	2.574	-104	0.006	-33	0.15	147	8.2
17.5	0.09	-26	2.562	-129	0.009	-75	0.18	137	8.2
18.0	0.06	-37	2.563	-154	0.012	-114	0.19	122	8.2
19.0	0.06	-42	2.561	151	0.015	179	0.14	93	8.2
19.5	0.08	-81	2.501	122	0.015	144	0.06	102	8.0
20.0	0.05	-103	2.430	94	0.015	108	0.10	-175	7.7

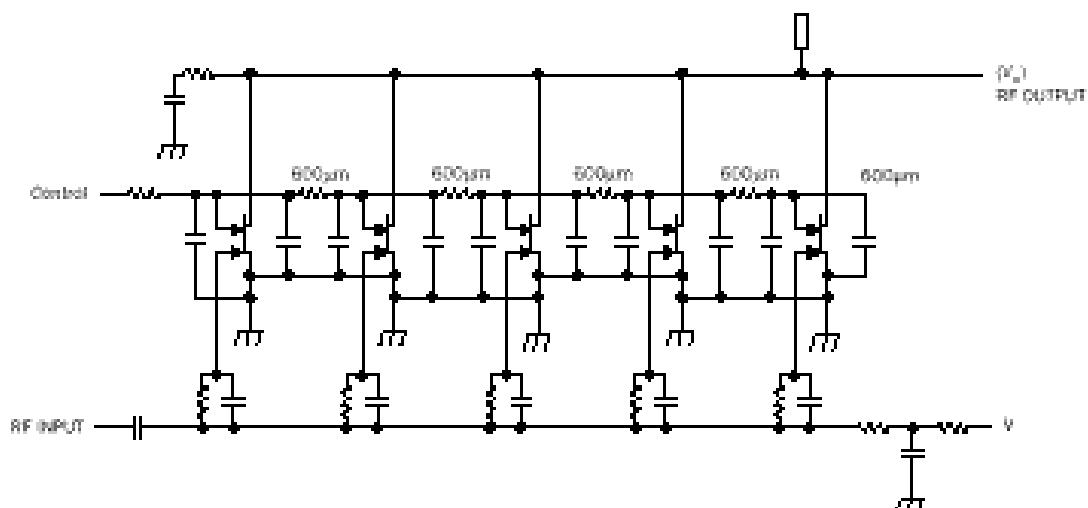
$$V_D = 8 \text{ V}, V_{CTRL} = 1 \text{ V}, I_D = 50\% I_{DSS}, T_A = 25^\circ\text{C},$$

The reference planes for S-parameter data include bond wires as specified in the "Recommended Assembly Diagram." The S-parameters are also available on floppy disk and the world wide web.

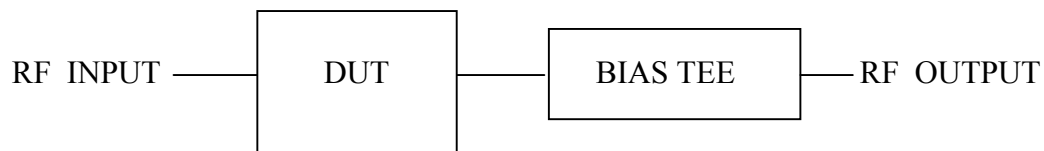
**THERMAL
INFORMATION**

PARAMETER	TEST CONDITION	NOM	UNIT
$R_{\theta JC}$ Thermal resistance (channel to backside)	$V_D = 8\text{ V}$, $I_D = 50\% I_{DSS}$, $V_{CTRL} = 1\text{ V}$	18.7	°C/W

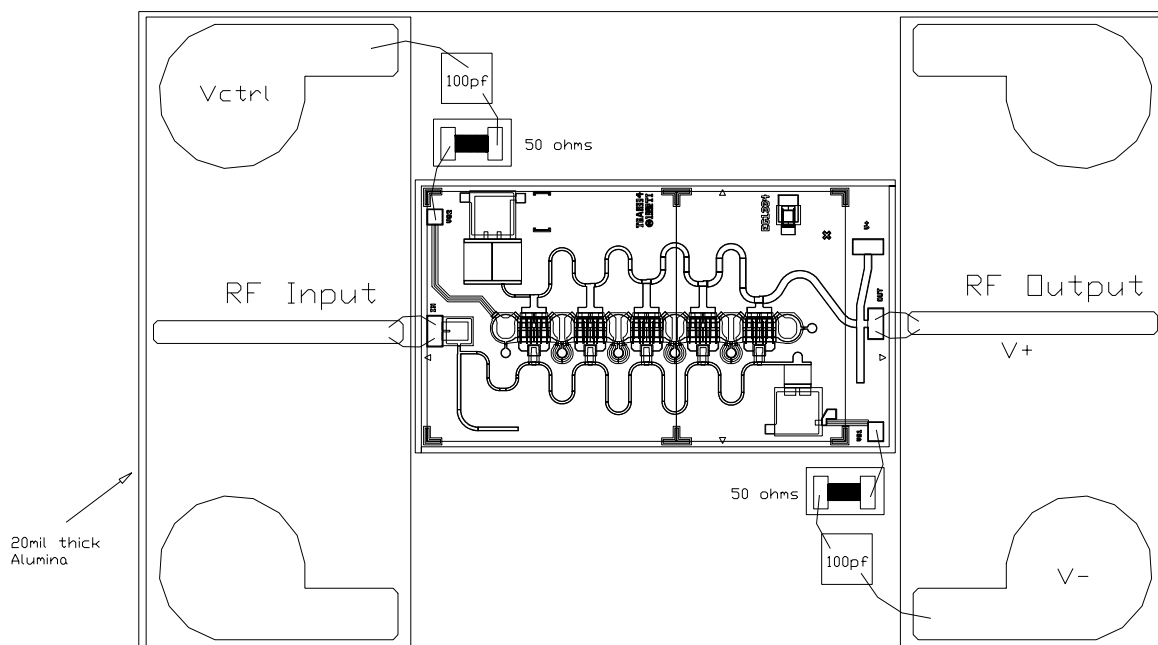
**EQUIVALENT
SCHEMATIC**



**RECOMMENDED
TEST
CONFIGURATION**



**RECOMMENDED
ASSEMBLY
DIAGRAM**



RF connections: Bond using two 1.0-mil diameter, 20 to 25-mil-length gold bondwires at both RF Input and RF Output.

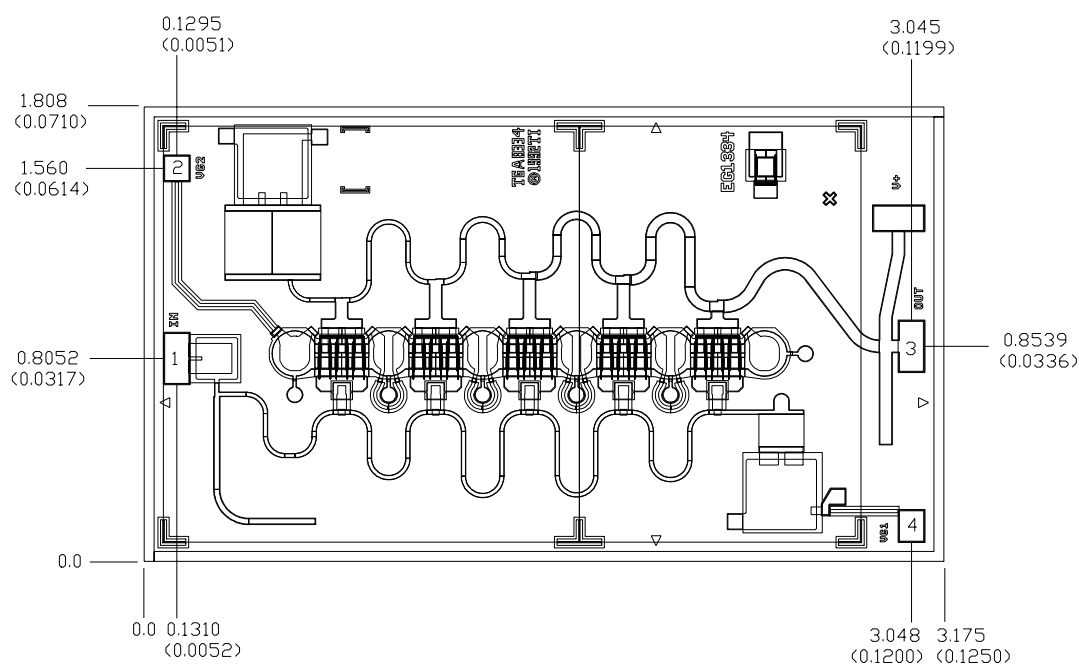
DC blocks required at RF Output port.

Close placement of external components is essential to stability.

Refer to TriQuint Semiconductor Gallium Arsenide Products Designers' Information on website or order literature number GMNA002.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

**MECHANICAL
DRAWING**



Units: millimeters (inches)

Thickness: 0.1524 (0.006) (reference only)

Chip edge to bond pad dimensions are shown to center of bond pad

Chip size tolerance: +/- 0.051 (0.002)

Bond Pad #1 (RF Input)	0.0965 x 0.1981 (0.0038 x 0.0078)
Bond Pad #2 (Vctrl)	0.0965 x 0.0965 (0.0038 x 0.0038)
Bond Pad #3 (RF Output/V+)	0.0965 x 0.1981 (0.0038 x 0.0078)
Bond Pad #4 (V-)	0.0965 x 0.1206 (0.0038 x 0.0048)

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