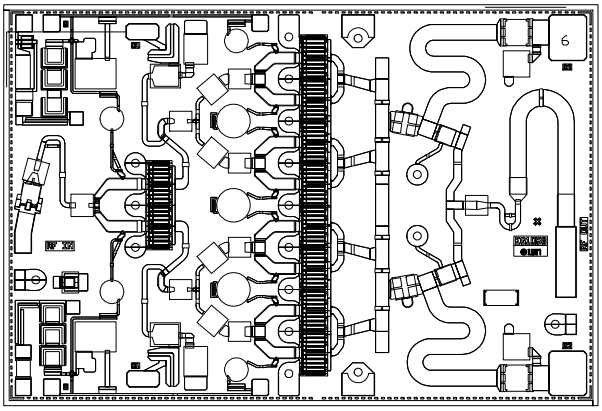
TriQuint SEMICONDUCTOR

Product Data Sheet
March 30, 2001

6.5 - 11.5 GHz High Power Amplifier TGA9083-SCC



Key Features and Performance

- 0.25um pHEMT Technology
- 6.5 GHz - 11.5 GHz Frequency Range
- Nominal 5 Watt Output Power at 7V, 6W at 8V, 8W at 9V.
- Nominal Gain of 19 dB
- 40% Power Added Efficiency at 7V, 35% PAE at 9V
- 12 dB Typical Input Return Loss, 9 dB Typical Output Return Loss
- On-Chip Active Gate Bias Circuit Option Simplifies Biasing
- Chip Dimensions 4.521 x 3.048 x 0.1 mm (0.178 x 0.120 x 0.004 in)

Description

The TriQuint TGA9083-SCC is a monolithic power amplifier which operates from 6.5 to 11.5 GHz. This device is currently a fully released product. This two stage power amplifier consist of a 2.5 mm pHEMT driving a 11.36 mm pHEMT at the output. The TGA9083-SCC is capable of providing 8 Watts of output power with 35% PAE when biased at 9 Volts. Typical 7 Volts operation provides 5 Watts of output power with a power-added efficiency of 40 percent. Typical small signal gain is 19 dB. In a balanced configuration, 12 Watts of output power is achievable with 40% PAE.

The TGA9083-SCC is fabricated using TriQuint's 0.25 um T-gate power pHEMT process. This device offers either standard gate biasing or an on-chip active gate bias circuit which simplifies gate biasing. The active gate bias (AGB) circuit requires a negative 5 V supply. This amplifier's output power and high efficiency over 6.5 to 11.5 GHz makes it a viable power amplifier solution in applications such as point-to-point radio, phased-array radar, and telecommunications.

Bond pad and backside metallization is gold plated for compatibility with eutectic alloy attachment methods as well as with thermocompression and thermosonic wire-bonding processes. The TGA9083-SCC is supplied in chip form and is readily assembled using automated equipment. Ground is provided to the circuitry through vias to the backside metallization.

TABLE I
MAXIMUM RATINGS

Symbol	Parameter	Value	Notes
V^+	Positive Supply Voltage	15V	
V^-	Negative Supply Voltage	-5 V to 0 V	
I^+	Positive Supply Current	3.5 A	
I^-	Negative Gate Current	70.4 mA	
P_D	Power Dissipation	39 W	
P_{IN}	Input Continuous Wave Power	25.5 dBm	
T_{CH}	Operating Channel Temperature	150 °C	1/, 2/
T_M	Mounting Temperature (30 seconds)	320 °C	
T_{STG}	Storage Temperature	-65°C to 150°C	

1/ These ratings apply to each individual FET

2/ Junction operating temperature will directly affect the device mean time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

TABLE II
DC PROBE TESTS (100%)
(T_A = 25°C ± 5°C)

NOTES	SYMBOL 2/	MEASUREMENT CONDITIONS 3/	LIMITS		UNITS
			MIN	MAX	
4/	I_{MAX1}	STD	938	1610	mA
1/,4/	V_{P1}	STD	0.5	1.5	V
1/,4/	V_{P2}	STD	0.5	1.5	V
1/,4/	$\|V_{BVGD1}\|$	STD	16	30	V
1/,4/	$\|V_{BVGS1}\|$	STD	16	30	V
1/,4/	$\|V_{BVGD2}\|$	STD	16	30	V

1/ V_{P1}, V_{P2}, V_{BVGD1}, V_{BVGD2} and V_{BVGS1} are negative

2/ Subscripts are refer to Q1, Q2 accordingly

3/ The measurement conditions are subject to change at the manufacture's discretion (without appropriate notification to the buyer)

4/ STD refers to Standard Test Conditions (see Table III for definitions)

TABLE III
AUTOPROBE FET PARAMETER MEASUREMENT CONDITIONS

FET Parameters	Test Conditions
V_P : Pinch-Off Voltage; V_{GS} for $I_{DS\ S}$ = 0.5 mA/mm of gate width.	V_{DS} fixed at 2.0 V, V_{GS} is swept to bring I_{DS} to 0.5 mA/mm.
V_{BVGD} : Breakdown Voltage, Gate-to-Drain; gate-to-drain breakdown current (I_{BD}) = 1.0 mA/mm of gate width.	Drain fixed at ground, source not connected (floating), 1.0 mA/mm forced into gate, gate-to-drain voltage (V_{GD}) measured is V_{BVGD} and recorded as BVGD; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.
V_{BVGS} : Breakdown Voltage, Gate-to-Source; gate-to-source breakdown current (I_{BS}) = 1.0 mA/mm of gate width.	Source fixed at ground, drain not connected (floating), 1.0 mA/mm forced into gate, gate-to-source voltage (V_{GS}) measured is V_{BVGS} and recorded as BVGS; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.
I_{MAX} : Maximum I_{DS}.	Positive voltage is applied to the gate to saturate the device. V_{DS} is stepped between 0.5 V up to a maximum of 3.5 V, searching for the maximum value of I_{DS}.

TABLE IV
RF WAFER CHARACTERIZATION TEST
(T_A = 25°C ± 5°C)

TEST	MEASUREMENT CONDITIONS	VALUE			UNITS
		MIN	TYP	MAX	
SMALL-SIGNAL GAIN MAGNITUDE	F = 6.5 – 11.5 GHz F = 10.5 – 11.5 GHz	15 13	19 17		dB dB
POWER OUTPUT AT 2 dB GAIN COMPRESSION 1/	F = 6.5 – 8.0 GHz F = 8.5 – 11.0 GHz F = 11.5 GHz	34 35 34.5			dBm
INPUT RETURN LOSS MAGNITUDE	F = 6.5 – 11.5 GHz	-7	-10		dB
OUTPUT RETURN LOSS MAGNITUDE	F = 6.5 – 11.5 GHz	-6	-10		dB
POWER ADDED EFFICIENCY	F = 6.5 – 11.5 GHz		40		%

1/ Output power is tested with Pin = 22 dBm ± 3 dBm, V_d = 7 V

Thermal Information:

PARAMETER	TEST CONDITIONS	NOM	UNIT
$R_{\theta}JC$, Thermal Resistance, channel to back side of carrier	25°C Base, V_D=9V, I_D=1.2A, P_D=6W	10	°C/W

Typical S-Parameters:

Frequency	S11		S21		S12		S22	
(GHz)	dB	ANG(°)	dB	ANG(°)	dB	ANG(°)	dB	ANG(°)
6.5	-14.31	-78.1	21.77	168.2	-64.33	88.1	-14.44	114.4
6.6	-13.64	-94.1	21.69	146	-60.56	81.2	-14.21	89.3
6.7	-13.08	-107.7	21.42	125.7	-58.66	70.2	-14.24	69.1
6.8	-12.72	-118.8	21.09	107	-57.67	59.6	-14.5	50.1
6.9	-12.36	-128.4	20.74	89.7	-57.01	48.2	-14.91	34.3
7	-12.15	-136.9	20.4	73.4	-56.72	37.4	-15.53	17.3
7.1	-11.94	-144.3	20.12	57.9	-56.97	28.1	-16.28	1.9
7.2	-11.81	-151	19.88	43.1	-57.08	20.2	-16.99	-14.2
7.3	-11.71	-157.2	19.69	28.9 -	57.77	11.7	-17. 83	-30.1
7.4	-11.62	-163	19.55	14.9	-57.76	4.5	-18.52	-46.3
7.5	-11.54	-168.6	19.48	1.3	-57.76	-5	-19.16	-61.9
7.6	-11.48	-174.6	19.44	-12.1	-57.71	-14.8	-19.83	-75.8
7.7	-11.46	179.6	19.45	-25.4	-58.13	-28.3	-20.05	-88.6
7.8	-11.49	173.5	19.51	-38.6	-58.49	-39.3	-20.59	-98
7.9	-11.56	167.5	19.61	-51.8	-58.82	-50.7	-20.68	-105.8
8	-11.64	161.1	19.75	-65	-58.75	-62.5	-20.89	-108.7
8.1	-11.84	154.7	19.93	-78.4	-59.1	-79.3	-20.52	-109.5
8.2	-12	148	20.16	-92.1	-59.09	-95.6	-19.67	-108.5
8.3	-12.27	140.8	20.41	–106.1	-59.22	–113.4	-18.6	–107.9
8.4	-12.59	133.2	20.67	–120.4	-58.89	–133.1	-17.09	–109.5
8.5	-13.03	124.8	20.93	-135	-58.8	-149.5	-15.59	-112.4
8.6	-13.55	115.8	21.18	-150	-58.78	-170.2	-14.14	-117.2
8.7	-14.2	106.2	21.39	-165.3	-58.42	173.1	-12.89	-124.4
8.8	-15	95.7	21.56	179.2	-58.06	152	-11.82	-132
8.9	-15.96	84.3	21.67	163.6	-57.95	133.7	-10.98	-141
9	-16.95	72.4	21.72	147.9	-57.57	114	-10.41	-150.3
9.1	-18.19	59.3	21.71	132.2	-57.49	93.9	-9.98	-160.1
9.2	-19.31	45.4	21.63	116.7	-57.13	77.9	-9.83	-170.4
9.3	-20.44	29.9	21.49	101.3	-57.62	59.4	-9.84	179.4
9.4	-21.28	14.1	21.3	86.3	-57.57	40.5	-10.03	168.5
9.5	-21.77	-3.6	21.07	71.4	-57.59	20.7	-10.44	158.1
9.6	-21.75	-19.6	20.81	56.8	-57.61	3.4	-10.91	147.1
9.7	-21.45	-35.6	20.52	42.5	-57.36	-15.4	-11.62	136
9.8	-20.72	-48.2	20.24	28.3	-57.08	-32.3	-12.32	124.6
9.9	-19.95	-58.9	19.95	14.3	-56.69	-51.1	-13.23	112.1
10	-19.15	-68.3	19.67	0.4	-56.18	-64.5	-14.16	100.1
10.1	-18.33	-76.7	19.38	-13.4	-55.71	-80	-15.11	86.9
10.2	-17.51	-84.1	19.11	-27.2	-54.67	-92.3	-16.2	73.2
10.3	-16.67	-91.4	18.86	–41.1	-54.34	–106.2	-17.11	59.2
10.4	-15.95	–98.1	18.61	-55	-53.49	-119.4	–18.22	43.6
10.5	-15.23	–104.5	18.37	–69	-53	-133.6	–19.22	28.4
10.6	-14.62	-110.8	18.13	-83	-52.35	-144.6	-20.24	11.4
10.7	-13.99	-117.4	17.89	-97.2	-51.8	-155.4	-21.37	-7.1
10.8	-13.41	-123.9	17.65	-111.8	-51.56	-166.5	-22.33	-26.6
10.9	-12.87	-130.8	17.42	-126.3	-51.12	-178.6	-23.12	-50.8
11	-12.39	-137.8	17.17	-141	-50.77	170.8	-23.74	-75.6
11.1	-11.97	-145.6	16.93	-156.2	-50.69	159.1	-23.25	-104.2
11.2	-11.57	-153.5	16.64	-171.4	-50.33	147.9	-22.17	-131.1
11.3	-11.21	-162.1	16.34	173.1	-50.57	136.5	-20.63	-153.4
11.4	-10.91	-171.2	16	157.3	-50.76	124.9	-18.89	-174
11.5	-10.63	179.2	15.63	141.4	-50.93	112.2	-17.29	168.8

T_A = 25°C, V_D = +8 V, I_D = 1.1 A

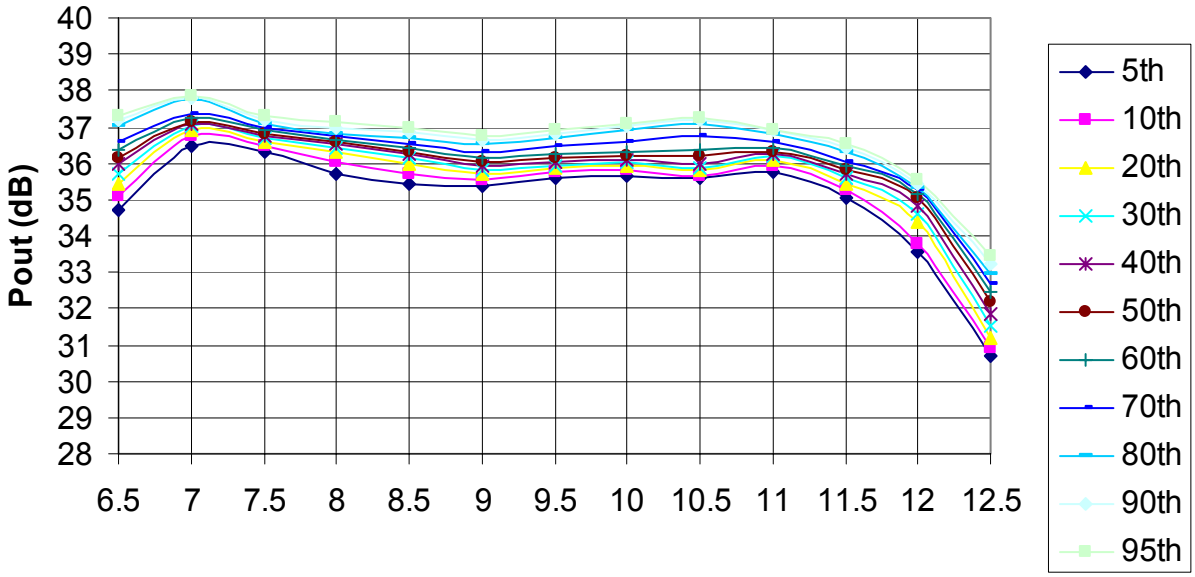
Reference planes for S-parameter data include bond wires as specified in the "Recommended Assembly Diagram"

On Wafer RF Probe Data Statistical Reference Summary

TGA9083 - 6181 Samples

Output Power:

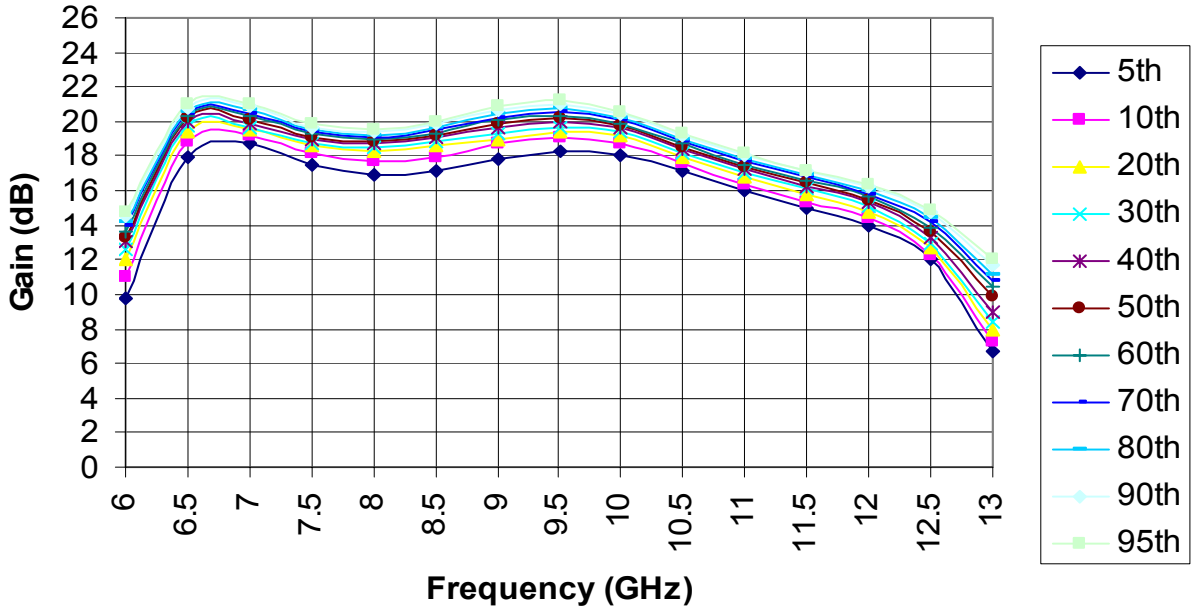
Bias Test Conditions: V_{d1}& V_{d2} = 7 V, V_{gg} = -5 V



TGA9083 - 6181 Samples

Small Signal Gain:

Bias Test Conditions: V_{d1}& V_{d2} = 7 V, V_{gg} = -5 V

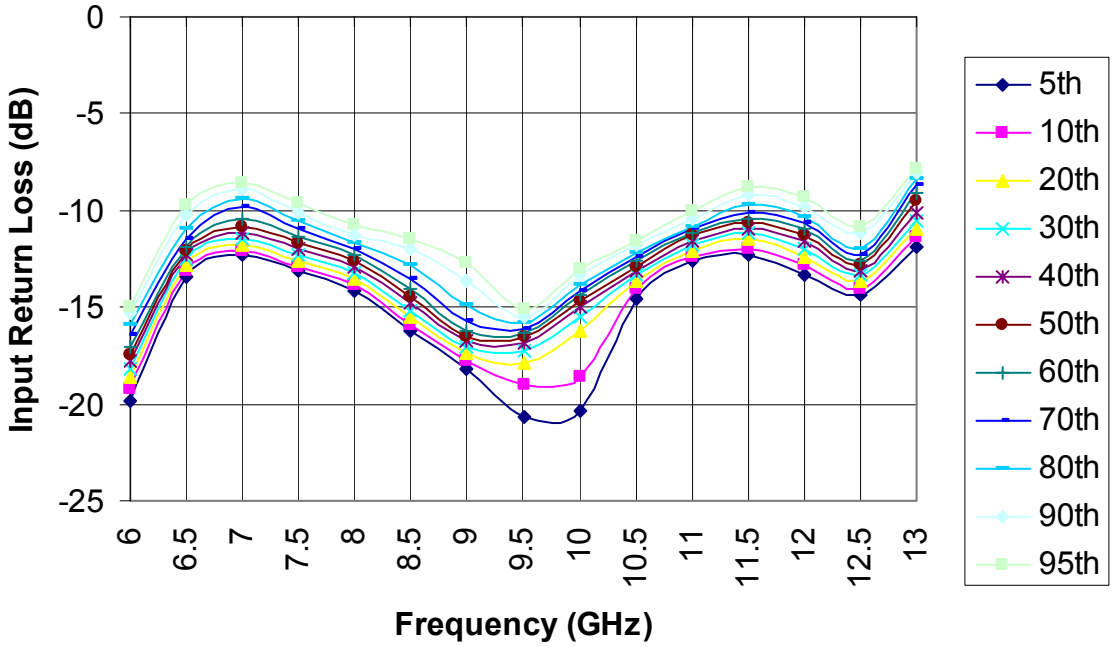


On Wafer RF Probe Data Statistical Reference Summary

TGA9083 - 6181 Samples

Input Return Loss:

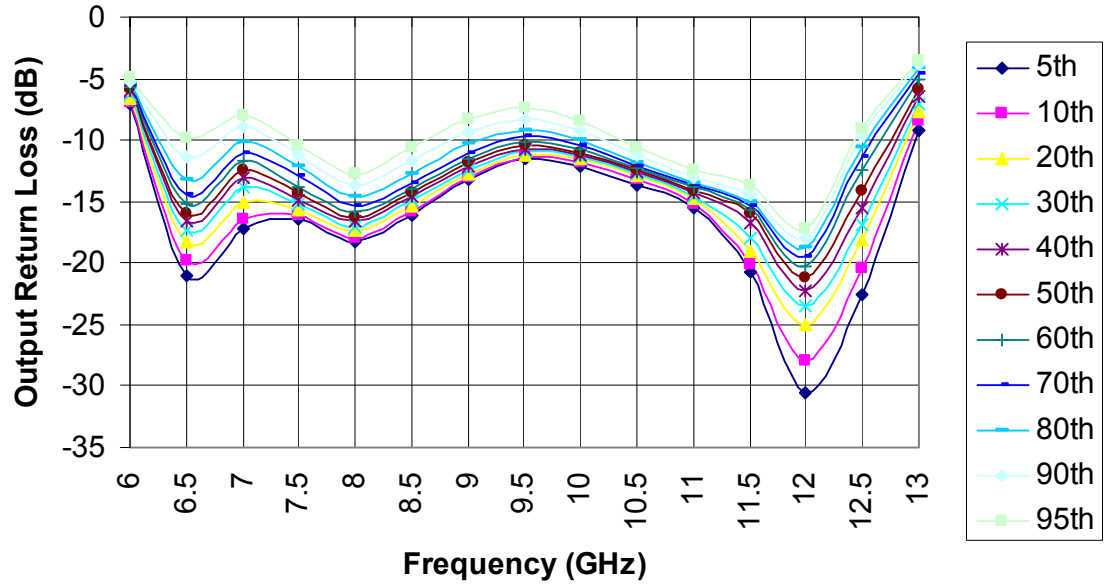
Bias Test Conditions: V_{d1}& V_{d2} = 7 V, V_{gg} = -5 V



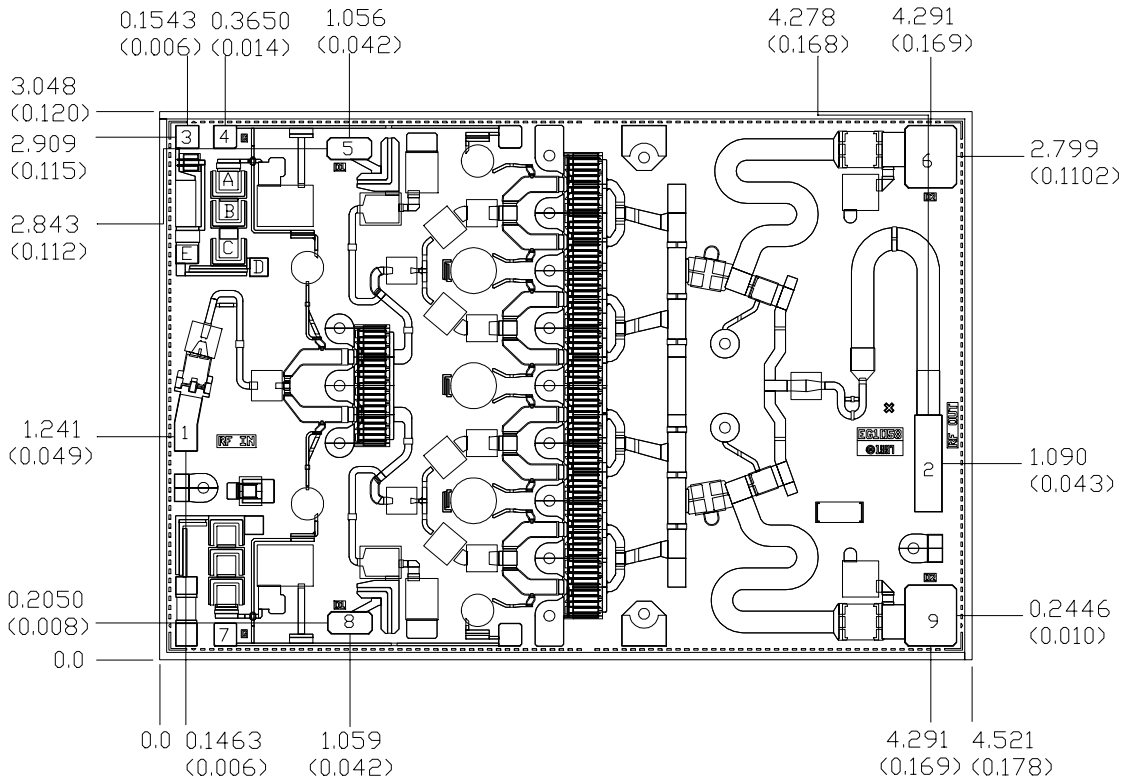
Output Return Loss:

TGA9083 - 6181 Samples

Bias Test Conditions: V_{d1}& V_{d2} = 7 V, V_{gg} = -5 V



Mechanical Drawing



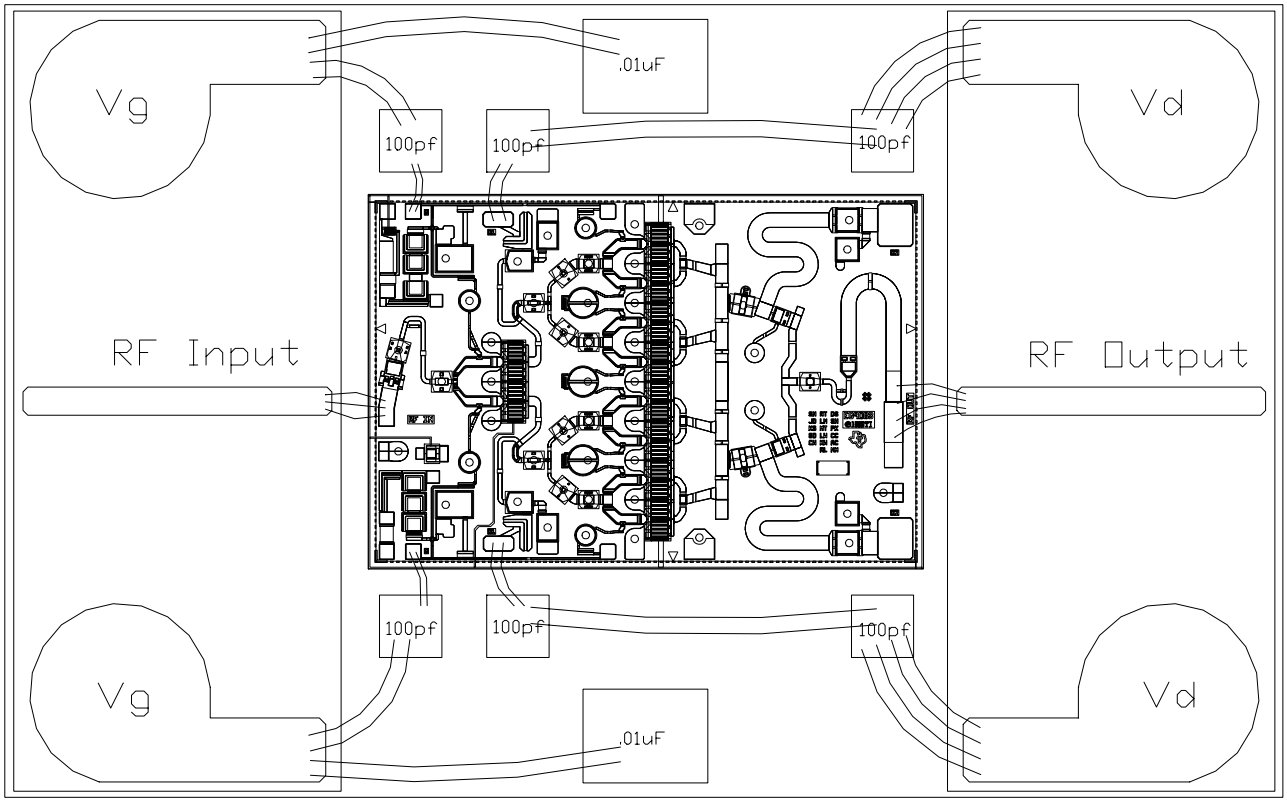
Units: millimeters (inches)
Thickness: 0.1016 (0.004)
Chip to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.051 (0.002)

Bond Pad #1 (RF Input)	Center two bond wires equal distance from centerline
Bond Pad #2 (RF Output)	Center two bond wires equal distance from centerline
Bond Pad #3 (Vgg)	0.120 x 0.120 (0.0047 x 0.0047)
Bond Pad #4,#7 (Vg)	0.120 x 0.120 (0.0047 x 0.0047)
Bond Pad #5,#8 (Vd1)	0.240 x 0.120 (0.0094 x 0.0047)
Bond Pad #6,#9 (Vd2)	0.275 x 0.340 (0.0108 x 0.0134)
Bond Pad A,B,C,D,E	0.120 x 0.120 (0.0047 x 0.0047)

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Chip Assembly and Bonding Diagrams

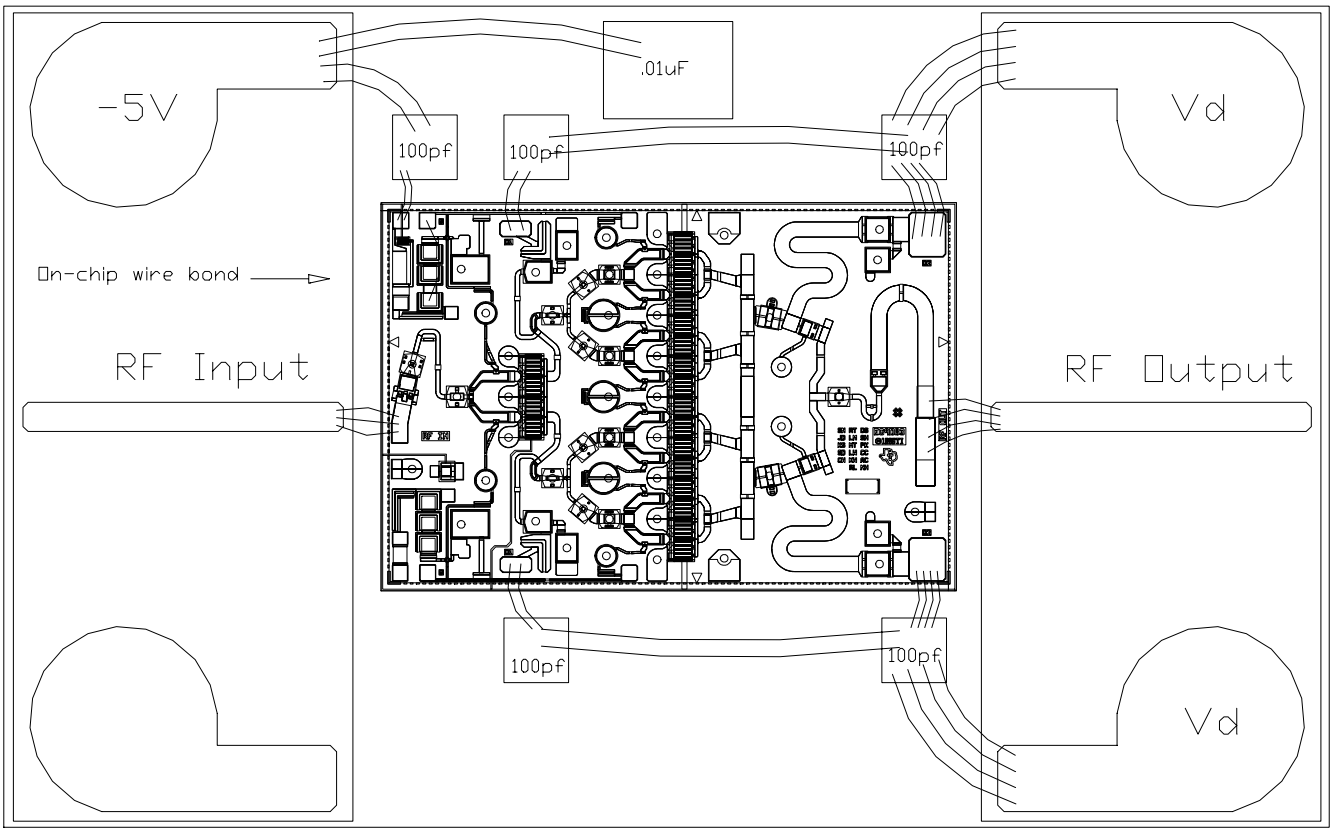
Recommended assembly diagram:



Bond using three (four at RFout) 1.0 mil diameter, 25 to 30 mil length gold bond wires at RF input and RF output for optimum performance. Bond wires connected to the RF output pad should be equal distance from center line as indicated in the drawing.

Close placement of external components is essential to stability. Drain bias should be connected to both sides of the MMIC.

Recommended Assembly Diagram Using Active Gate Bias:



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Close placement of external components is essential to stability. Drain bias should be connected to both sides of the MMIC.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Reflow process assembly notes:

- AuSn (80/20) solder with limited exposure to temperatures at or above 300°C
- alloy station or conveyor furnace with reducing atmosphere
- no fluxes should be utilized
- coefficient of thermal expansion matching is critical for long-term reliability
- storage in dry nitrogen atmosphere

Component placement and adhesive attachment assembly notes:

- vacuum pencils and/or vacuum collets preferred method of pick up
- avoidance of air bridges during placement
- force impact critical during auto placement
- organic attachment can be used in low-power applications
- curing should be done in a convection oven; proper exhaust is a safety concern
- microwave or radiant curing should not be used because of differential heating
- coefficient of thermal expansion matching is critical

Interconnect process assembly notes:

- thermosonic ball bonding is the preferred interconnect technique
- force, time, and ultrasonics are critical parameters
- aluminum wire should not be used
- discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire
- maximum stage temperature: 200°C