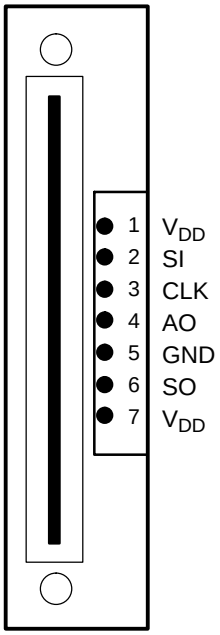
- **512 × 1 Sensor-Element Organization**
- **200 Dots-Per-Inch (DPI) Sensor Pitch**
- **Performance Upgrade for the Texas Instruments TSL218**
- **High Linearity and Low Noise for 256 Gray Scale Applications**
- **Output Referenced to Ground**
- **Low Image Lag . . . 0.5% Typ**
- **Operation to 2 MHz**
- **Single 5-V Supply**

(TOP VIEW)

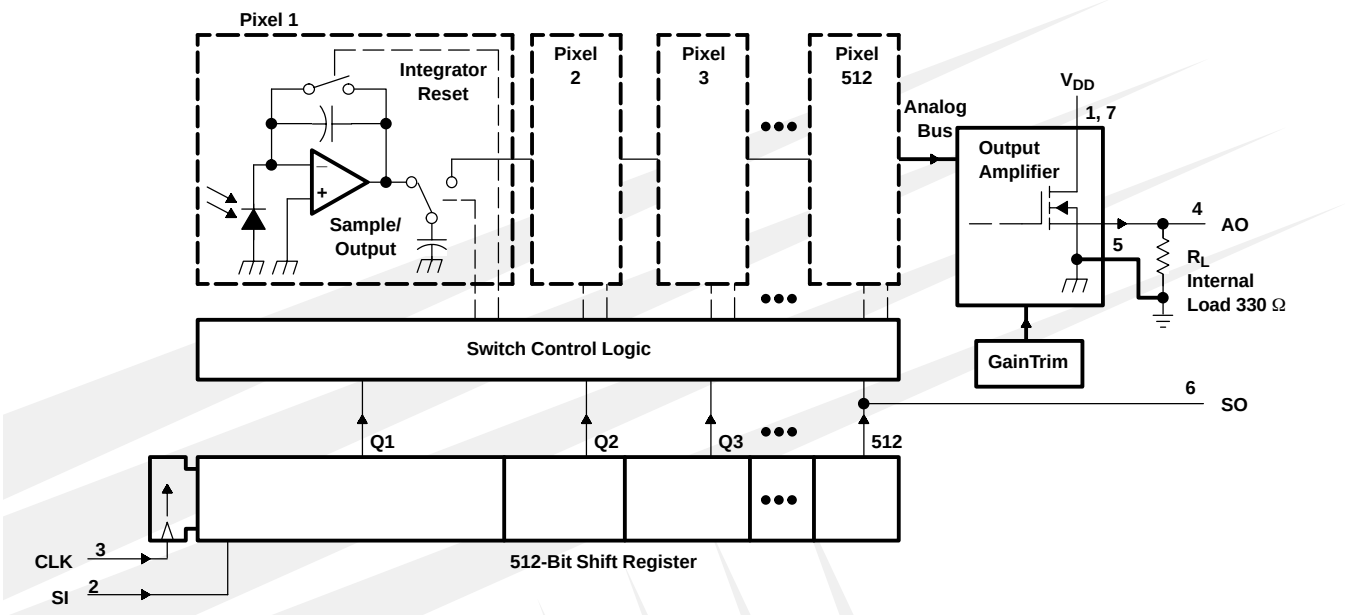


Description

The TSL208 linear sensor array consists of 512 photodiodes, each with associated charge amplifier circuitry, aligned to form a contiguous 512 by 1 pixel array. Device pixels measure 120 mm (H) by 70 mm (W) with 125-mm center-to-center spacing and 55-mm spacing between pixels. Operation is simplified by internal logic that requires only a serial input (SI) pulse and a clock.

The device is intended for use in a wide variety of applications including contact imaging, mark and code reading, bar-code reading, edge detection and positioning, OCR, level detection, and linear and rotational encoding.

Functional Block Diagram



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AO	4	O	Analog output.
CLK	3	I	Clock. The clock controls the charge transfer, pixel output and reset.
GND	5	I	Ground (substrate). All voltages are referenced to the substrate.
SI	2	I	Serial input. SI defines the start of the data out sequence.
SO	6	O	Serial output. SO signals the end of the data out sequence.
VDD	1, 7	I	Supply voltage for both analog and digital circuits.

Detailed Description

The sensor consists of 512 photodiodes, called pixels, arranged in a linear array. Light energy impinging on a pixel generates photocurrent that is then integrated by the active integration circuitry associated with that pixel.

During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity on that pixel and the integration time. The voltage output developed for each pixel is according to the following relationship:

$$Vout = KEt$$

where:

Vout is the voltage output for each pixel

K is the responsivity of the pixel at a given wavelength

E is the light intensity at the pixel given in $\mu Watts/cm^2$

t is the integration time given in seconds

The output and reset of the integrators are controlled by a 512-bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI. As the SI pulse is clocked through the shift register, the charge stored on the sampling capacitors of each pixel is sequentially connected to a charge-coupled output amplifier that generates a voltage on analog output AO (given above). After being read the pixel integrator is then reset, and the next integration period begins for that pixel. On the 513th clock rising edge, the SO pulse is clocked out on signifying the end of the read cycle. The device is then ready for another read cycle.

AO is driven by a source follower that requires an external pulldown resistor. When the output is not in the output phase, it is in a high-impedance state. The output is nominally 0 V for no light input and 2 V for a nominal full-scale output.

Absolute Maximum Ratings†

Supply voltage, V_{DD} . . . . . 7 V
Digital output current range, V_O . . . . . –0.5 V to V_{DD+}0.5 V
Digital output current . . . . . –10 mA to 10 mA
Digital input current range, I_I . . . . . –20 mA to 20 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions (see Figure 1 and Figure 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	$V_{DD} \times 0.7$		V_{DD}	V
Low-level input voltage, V_{IL}	0		$V_{DD} \times 0.3$	V
Wavelength of light source, λ	400		1000	nm
Clock frequency, f_{clock}	5		2000	kHz
Sensor integration time, t_{int}	0.2565		100	ms
Setup time, serial input, $t_{su(SI)}$	20			ns
Hold time, serial input, $t_{h(SI)}$ (see Note 1)	0			ns
Operating free-air temperature, T_A	0		70	°C

NOTE 1: SI must go low before the rising edge of the next clock pulse.

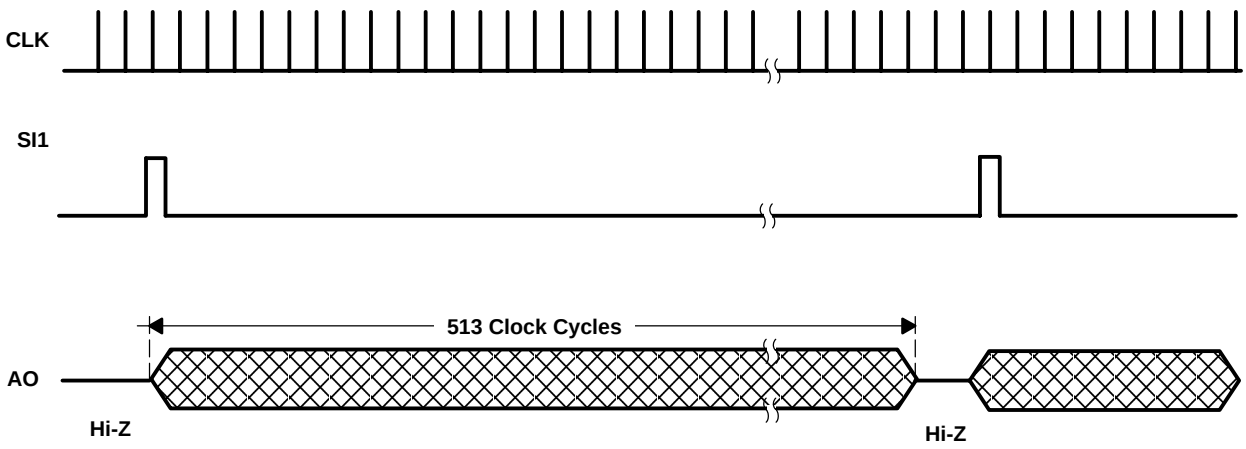


Figure 1. Timing Waveforms

Electrical Characteristics at f_{clock} = 200 kHz, V_{DD} = 5 V, T_A = 25°C, λ_p = 660 nm, t_{int} = 5 ms, R_L = 330 Ω, E_e = 20μW/cm² (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Analog output voltage (white, average over 512 pixels)		1.6	2	2.4	V
	Analog output voltage (dark, average over 512 pixels)	E_e = 0	0	0.07	0.15	V
PRNU	Pixel response nonuniformity	See Note 3			±20	%
	Nonlinearity of analog output voltage	See Note 4		±0.4%		FS
	Output noise voltage	E_e = 0, See Note 5		1		mVrms
	Saturation exposure	See Note 6	95	105		nJ/cm²
	Analog output saturation voltage		2.7	2.75		V
DSNU	Dark signal nonuniformity	All pixels, E_e = 0 See Note 7		0.04	0.12	V
IL	Image lag	See Note 8		0.5		%
I_{DD}	Supply current			32	45	mA
I_{IH}	High-level input current	$V_I = V_{DD}$			10	μA
I_{IL}	Low-level input current	V_I = 0			10	μA
C_i	Input capacitance			10		pF

NOTES: 2. Clock duty cycle is assumed to be 50%.
3. PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated.
4. Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
5. RMS noise is the standard deviation of a single-pixel output under constant illumination as observed over a 5-second period.
6. Minimum saturation exposure is calculated using the maximum responsivity and minimum output saturation voltage figures.
7. DNSU is the difference between the maximum and minimum of dark-current voltage.
8. Image lag is a residual signal left in a pixel from a previous exposure. It is defined as a percent of white-level signal remaining after a pixel is exposed to a white condition followed by a dark condition:

$$IL = \frac{V_{AO} - V_{AO(dark)}}{V_{AO(white)} - V_{AO(dark)}} \times 100$$

Operating Characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{w(H)}$	Clock pulse duration (high)		50			ns
$t_{w(L)}$	Clock pulse duration (low)		50			ns
t_s	Analog output settling time to ±1%	R_L = 330 Ω, C_L = 50 pF		350		ns

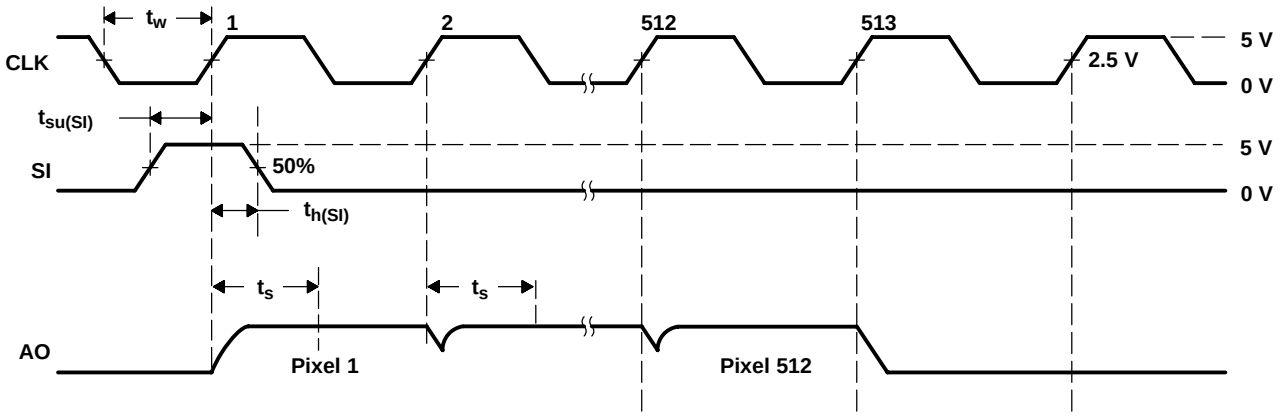


Figure 2. Operational Waveforms

TYPICAL CHARACTERISTICS

PHOTODIODE SPECTRAL RESPONSIVITY

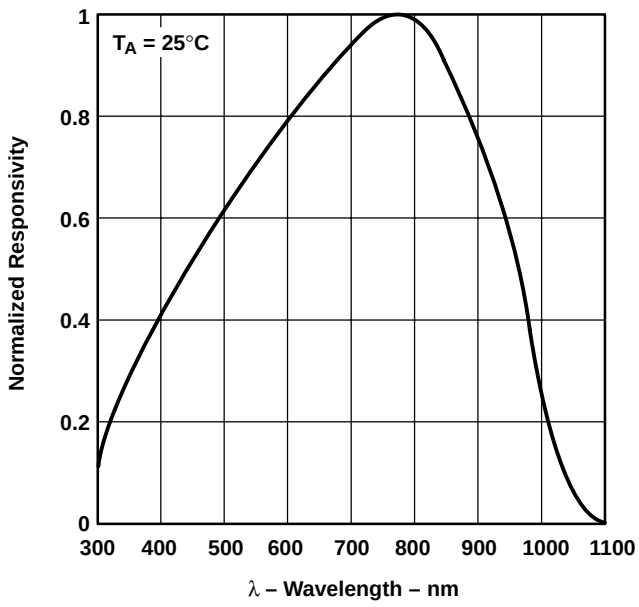
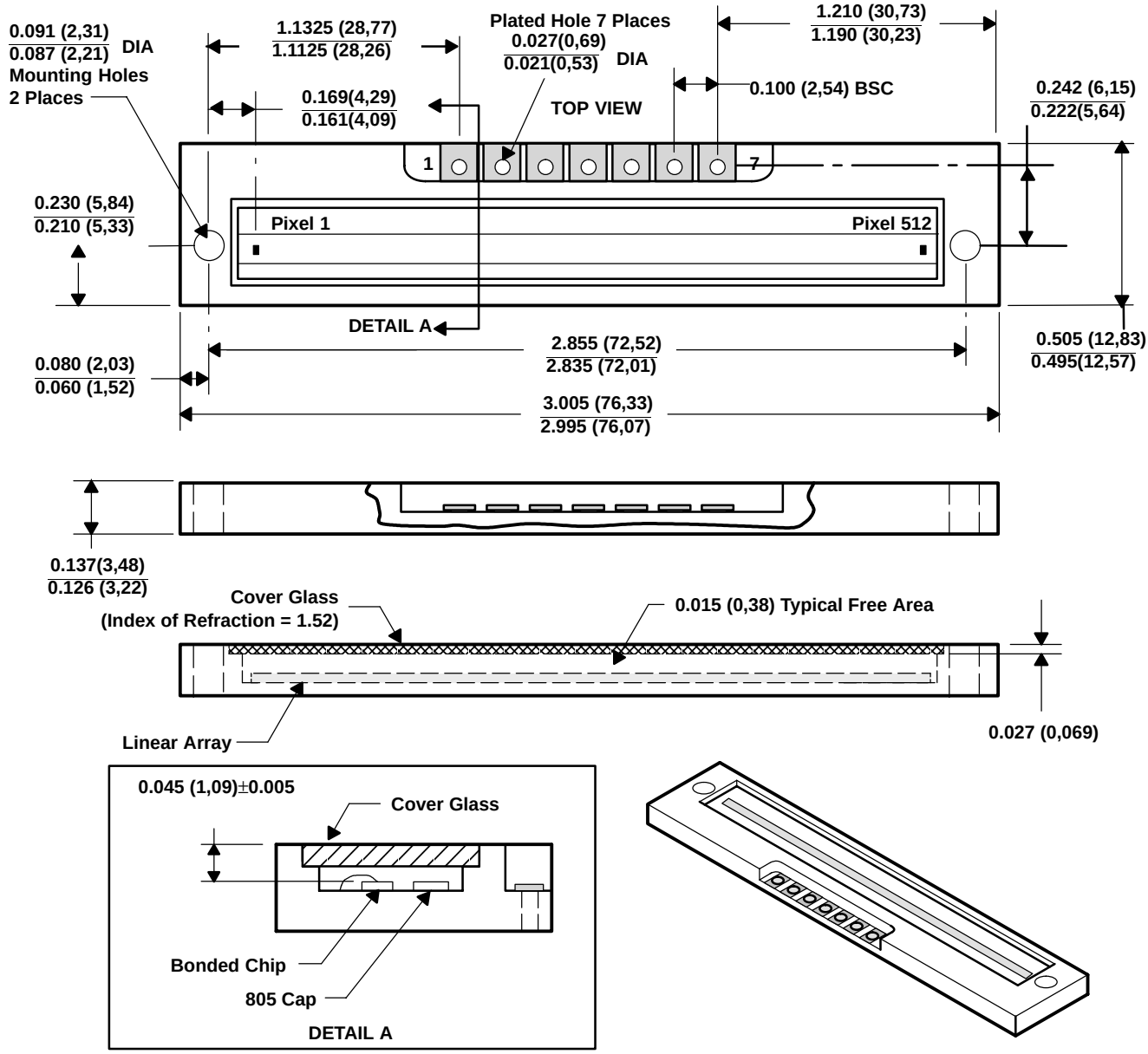


Figure 3

MECHANICAL INFORMATION



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Pixel centers are located along the center line of the mounting holes.

Figure 4. TSL208 Mechanical Specifications

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