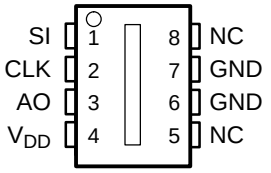
- **64 × 1 Sensor-Element Organization**
- **200 Dots-Per-Inch (DPI) Sensor Pitch**
- **Performance Upgrade for the Texas Instruments TSL213**
- **High Linearity and Uniformity for 256 Gray-Scale (8-Bit) Applications**
- **Output Referenced to Ground**
- **Low Image Lag . . . 0.5% Typ**
- **Operation to 2 MHz**
- **Single 5-V Supply**

(TOP VIEW)



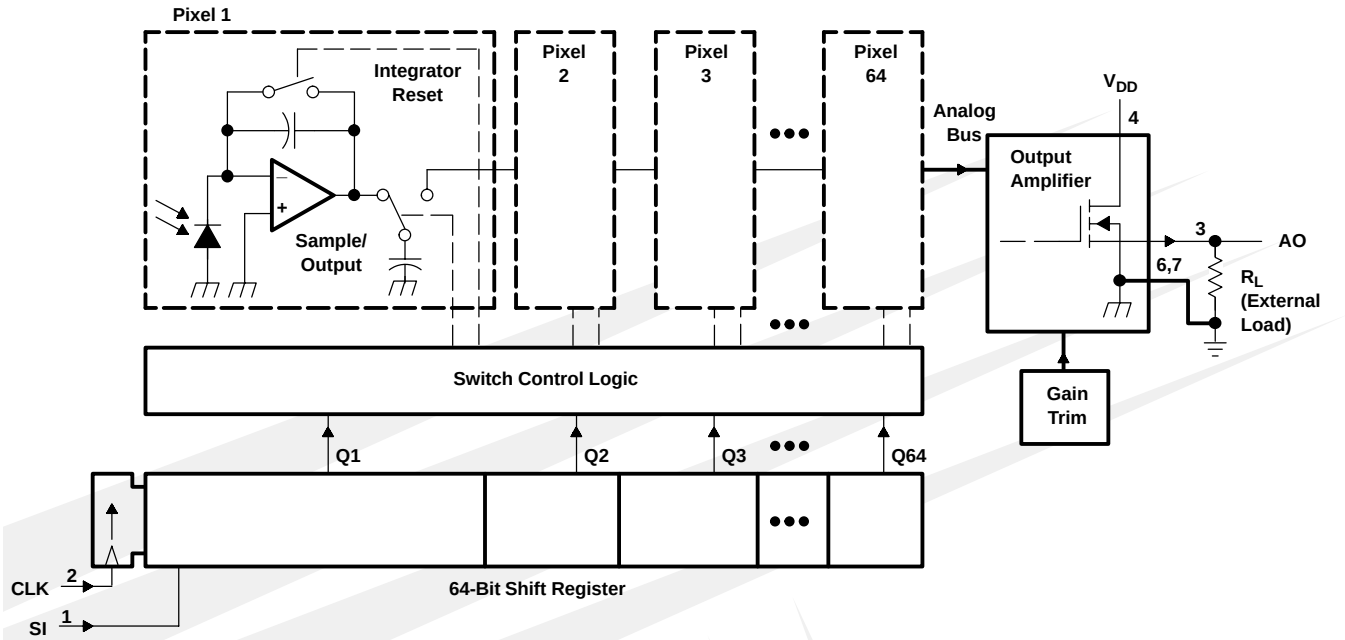
NC – No internal connection

Description

The TSL201 linear sensor array consists of a 64 × 1 array of photodiodes, associated charge amplifier circuitry, and a pixel data-hold function that provides simultaneous-integration start and stop times for all pixels. The pixels measure 120 μm (H) by 70 μm (W) with 125-μm center-to-center spacing and 55-μm spacing between pixels. Operation is simplified by internal control logic that requires only a serial-input (SI) signal and a clock.

The TSL201 is intended for use in a wide variety of applications including mark detection and code reading, optical character recognition (OCR) and contact imaging, edge detection and positioning as well as optical linear and rotary encoding.

Functional Block Diagram



Texas Advanced Optoelectronic Solutions Inc.
800 Jupiter Road, Suite 205 • Plano, TX 75074 • (972) 673-0759

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AO	3	Analog output
CLK	2	Clock. The clock controls charge transfer, pixel output, and reset.
GND	6, 7	Ground (substrate). All voltages are referenced to the substrate.
NC	5, 8	No internal connection
SI	1	Serial input. SI defines the start of the data-out sequence.
V_{DD}	4	Supply voltage. Supply voltage for both analog and digital circuits.

Detailed Description

The sensor consists of 64 photodiodes arranged in a linear array. Light energy impinging on a photodiode generates photocurrent, which is integrated by the active integration circuitry associated with that pixel. During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity and the integration time. The integration time is the interval between two consecutive output periods.

The output and reset of the integrators is controlled by a 64–bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI for one positive going clock edge (see Figures1 and 2). As the SI pulse is clocked through the 64 bit shift register, the charge on the sampling capacitor of each pixel is sequentially connected to a charge–coupled output amplifier that generates a voltage output AO. When the bit position goes low the pixel integrator is reset. On the 65th clock rising edge, the SI pulse is clocked out of the shift register and the output assumes a high impedance state. Note that this 65th clock pulse is required to terminate the output of the 64th pixel and return the internal logic to a known state. A subsequent SI pulse can be presented on the 66th clock pulse, thereby initiating another pixel output cycle.

The voltage developed at analog output (AO) is given by:

$$\mathbf{Vout = KEt}$$

where:

Vout	is the output voltage
K	is the device responsivity for a given wavelength of light given in $V/(\mu J/cm^2)$
E	is the intensity of light at each pixel given in $\mu W/cm^2$
t	is integration time in seconds

AO is driven by a source follower that requires an external pulldown resistor (330 ohms typ.). The source follower configuration permits an analog wired OR hookup of multiple devices. When the device is not in the output phase AO is in a high impedance state. The output is nominally 0 volts for no light and 2 volts for a nominal white level output, with a nominal full–scale (saturation) voltage of 2.5V.

Absolute Maximum Ratings†

Supply voltage, V_{DD} . . . . . 7 V
Digital input current range, I_I . . . . . –20 mA to 20 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions (see Figure 1 and Figure 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	$V_{DD} \times 0.7$		V_{DD}	V
Low-level input voltage, V_{IL}	0		$V_{DD} \times 0.3$	V
Wavelength of light source, λ	400		1000	nm
Clock frequency, f_{clock}	5		2000	kHz
Sensor integration time, t_{int}	0.0325		100	ms
Setup time, serial input, $t_{su(SI)}$	20			ns
Hold time, serial input, $t_{h(SI)}$ (see Note 1)	0			ns
Operating free-air temperature, T_A	0		70	°C

NOTE 1: SI must go low before the rising edge of the next clock pulse.

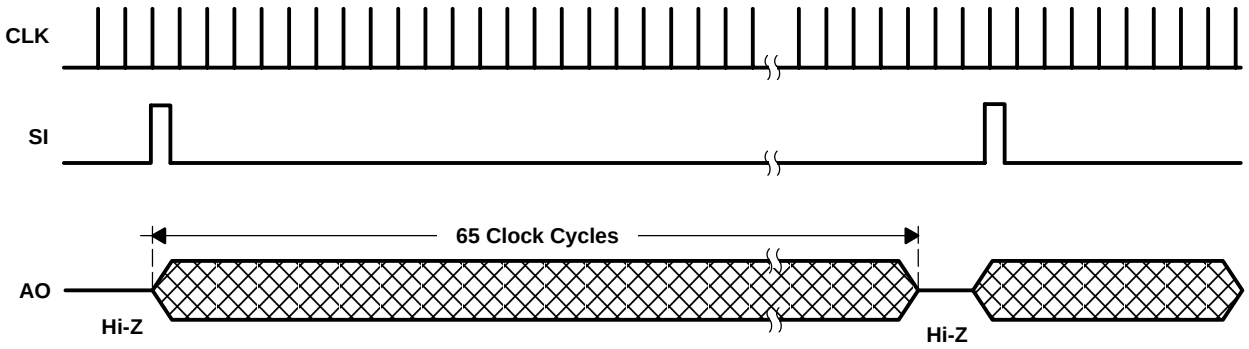


Figure 1. Timing Waveforms

Electrical Characteristics at f_{clock} = 200 kHz, V_{DD} = 5 V, T_A = 25°C, λ_p = 565 nm, t_{int} = 5 ms, R_L = 330 Ω, E_e = 20 μW/cm² (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Analog output voltage (white, average over 64pixels)			1.6	2	2.4	V
	Analog output voltage (dark, average over 64 pixels)	E_e = 0		0	0.07	0.15	V
PRNU	Pixel response nonuniformity	See Note 3			±4	±7.5	%
	Nonlinearity of analog output voltage	See Note 4			±0.4%		FS
	Output noise voltage	See Note 5			1		mVrms
	Saturation exposure	See Note 6		120	137		nJ/cm²
	Analog output saturation voltage			2.5	2.75		V
DSNU	Dark signal nonuniformity	See Note 7	E_e = 0		0.04	0.120	V
IL	Image lag	See Note 8			0.5%		
I_{DD}	Supply current				2.5	4	mA
I_{IH}	High-level input current	$V_I = V_{DD}$				1	μA
I_{IL}	Low-level input current	V_I = 0				1	μA
C_i	Input capacitance				5		pF

NOTES: 2. Clock duty cycle is assumed to be 50%.
3. PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated.
4. Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
5. RMS noise is the standard deviation of a single-pixel output under constant illumination as observed over a 5-second period.
6. Saturation exposure is calculated using the maximum responsivity and minimum output saturation voltage figures.
7. DNSU is the difference between the maximum and minimum of dark-current voltage.
8. Image lag is a residual signal left in a pixel from a previous exposure. It is defined as a percent of white-level signal remaining after a pixel is exposed to a white condition followed by a dark condition:

$$IL = \frac{V_{AO} - V_{AO(dark)}}{V_{AO(white)} - V_{AO(dark)}} \times 100$$

Operating Characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{w(H)}$	Clock pulse duration (high)		50			ns
$t_{w(L)}$	Clock pulse duration (low)		50			ns
t_s	Analog output settling time to ±1%	R_L = 330 Ω, C_L = 50 pF		350		ns

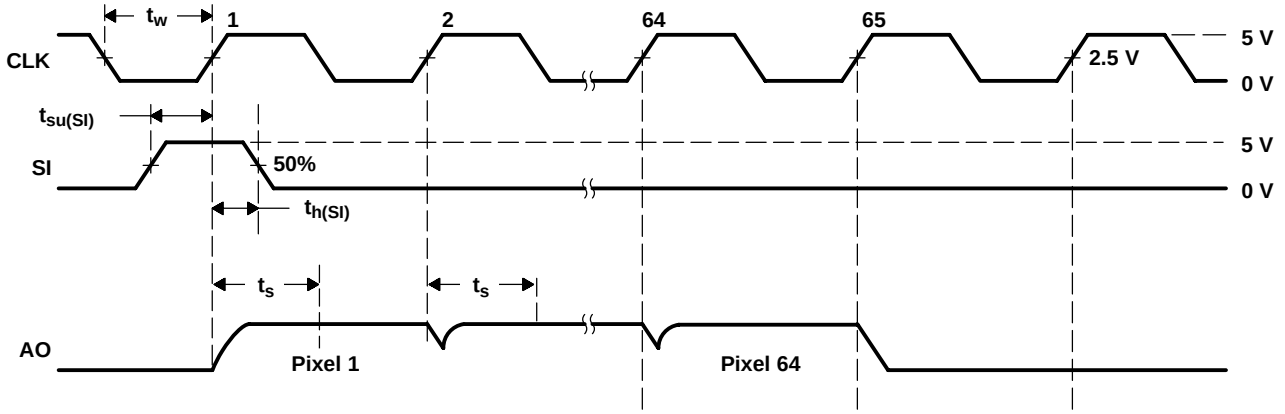


Figure 2. Operational Waveforms

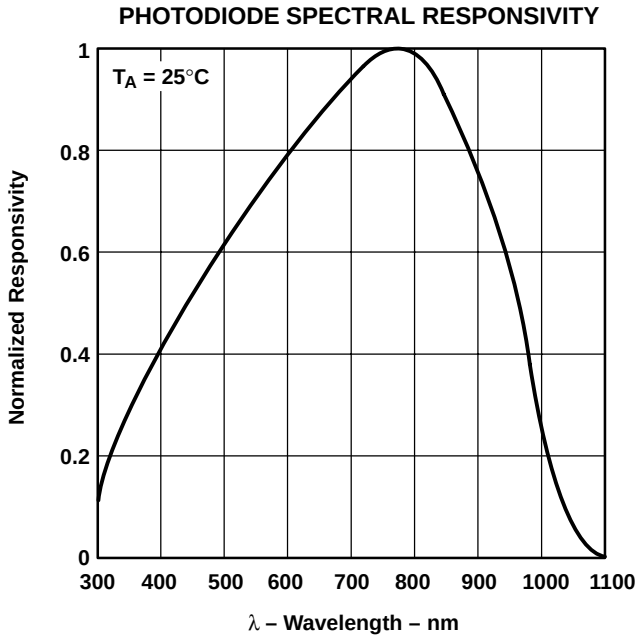
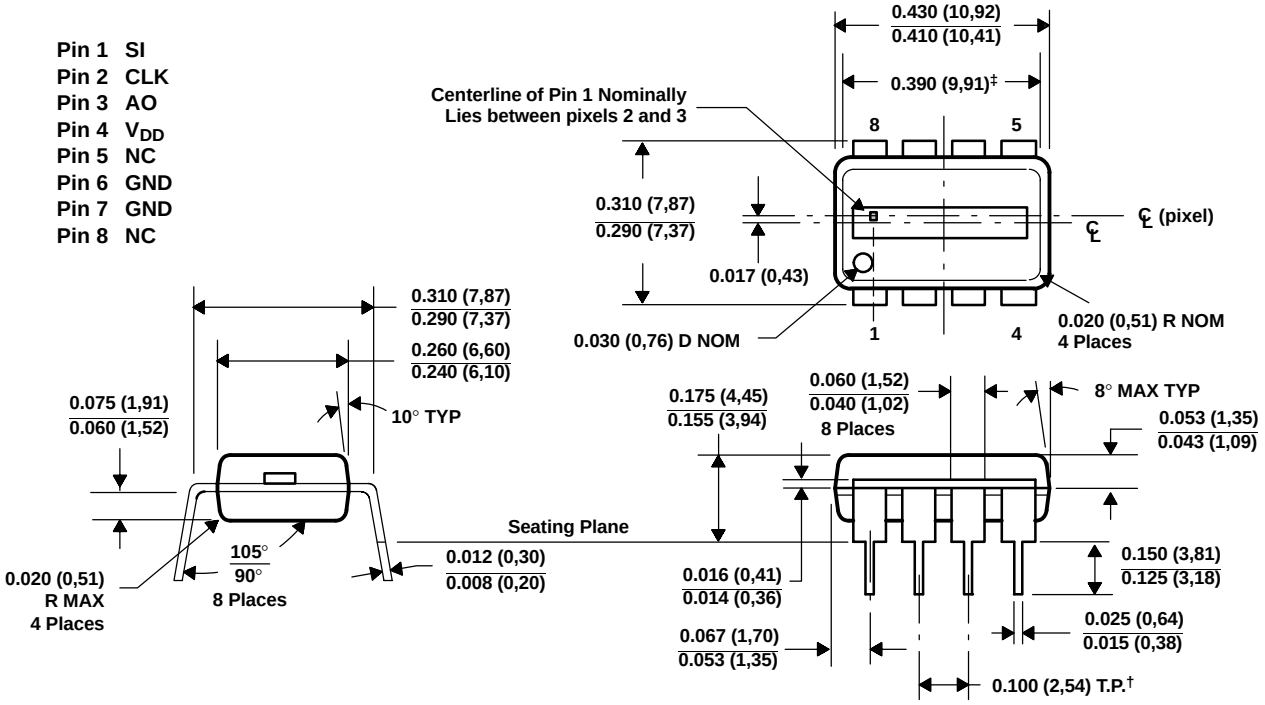


Figure 3

MECHANICAL INFORMATION

This dual-in-line package consists of an integrated circuit mounted on a lead frame and encapsulated with an electrically nonconductive clear plastic compound.



† True position when unit is installed
‡ Minimum flat-optical-surface length

NOTES: A. All linear dimensions are in inches and parenthetically in millimeters.
B. This drawing is subject to change without notice.
C. Index of refraction of clear plastic is 1.55.

Figure 4. Packaging Configuration

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