TC3399A

PCMCIA ETHERNET CONTROLLER AND UART INTERFACE

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PCMCIA Ethernet Controller And Uart Interface

1 Features

- PCMCIA 2.01 bus interface.
- Use serial EEPROM 93C56/66 to store CIS.
- 100-pin LQFP package.
- Low Power CMOS process.

Ethernet LAN features:

- NE2000 compatible.
- IEEE 802.3 compatible.
- Endec, UTP, AUI.
- Auto media select between AUI, UTP.
- TC3399A for UTP and AUI interface.
- LED support for Link.

UART interface features:

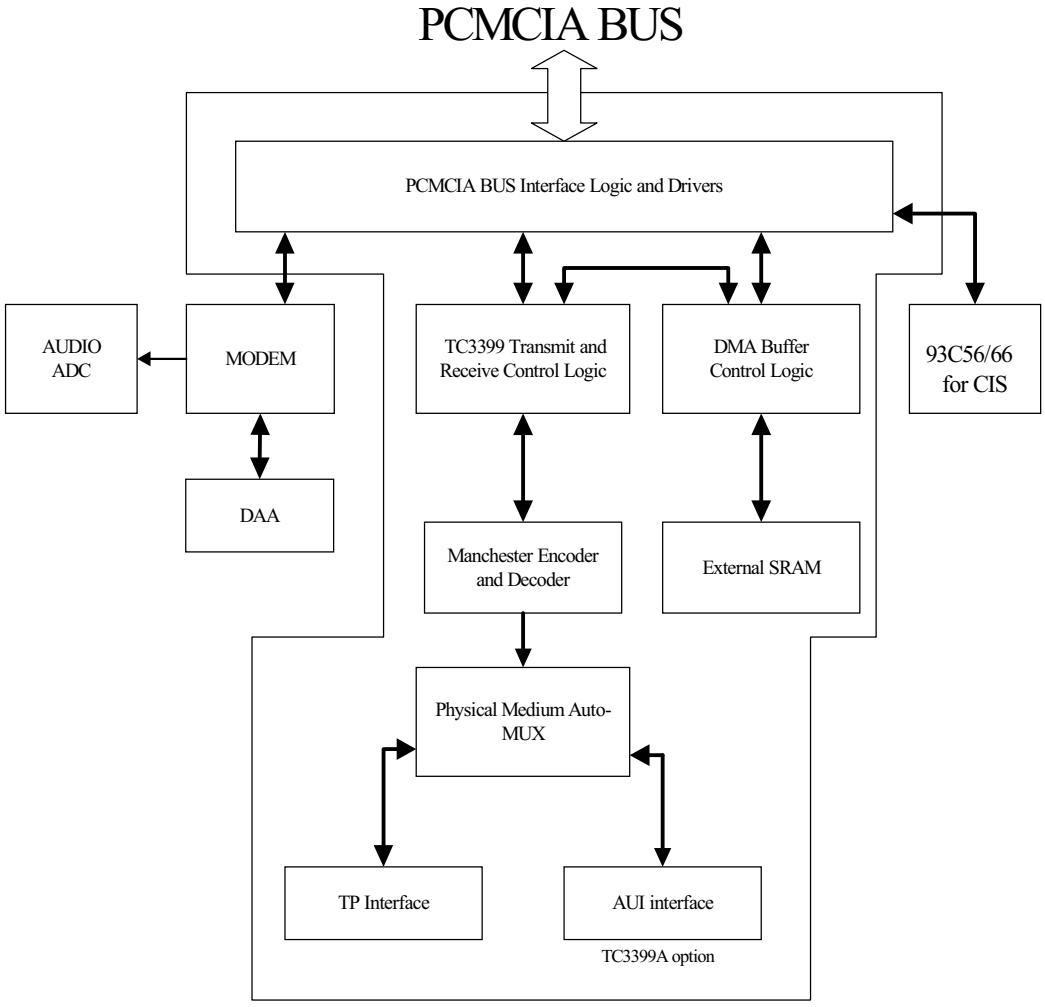
- Provide PCMCIA interface and POWER DOWN control for the following Fax/Modem groups:
  ⇒ General modem chip sets with parallel bus interface, for example,
  Rockwell C39/C29 controller base RC96V24AC/RC14V24AC modem chipset,
  Rockwell C39/C29 controller base RC96ACL/RC144ACL modem chipset,
  AT&T V.32lite modem chipset,
  CIRRUS CL-MD1414ECT,
  etc....
- Support two ring handling methods:
  ⇒ I/O Event indication Register
  ⇒ Ring indication pass-through to Status Change
- Support two Interrupt handling methods:
  ⇒ ORed with Ethernet controller and modem interrupt
  ⇒ Ethernet controller interrupt pass-through to Status Change
- Support Ethernet controller and Modem interrupt status indication register

2 General Description

The TC3399A (PECUI) is designed to reduce parts count and cost for easy implementation of PCMCIA CSMA/CD. Local Area Networks and Fax/Modem in one card. The TC3399A is the integration of the entire bus interface for PCMCIA BUS and includes Ethernet controller, Manchester Encoder/Decoder, 10BaseT function, AUI interface and UART interface. It complies with IEEE 802.3 standards. TC3399A is compatible to NS8390 controller's register and Novell NE2000 industry Ethernet standard. To store CIS, TC3399A only need EEPROM 93C56/66 in PCMCIA LAN CARD to reduce part cost. Physical media 10BaseT, AUI interface are fully automatic detection. LED driver for Link are also provided. For UART interface, It buffers ring indicator, the audio input and the interrupt to the PCMCIA.
10BaseT functional block includes receiver and transmitter, collision, loopback, jabber and link integrity and Polarity Detection/Correction blocks as defined in standard.

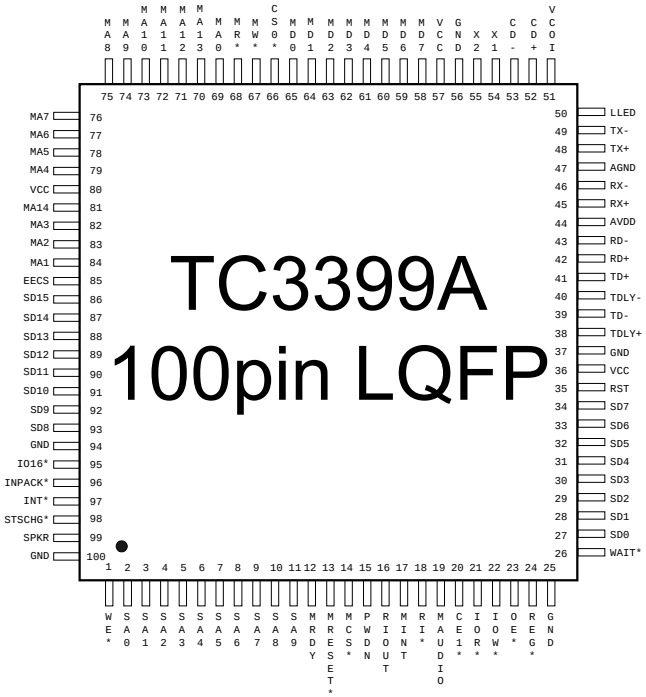
TC3399A uses analog Phase Lock Loop method for the manchester encoding and decoding required by the IEEE 802.3 specification at 10 Mbit/sec. A collision detect translator and diagnostic Loopback Capability are included.
TC3399A is designed for conventional PCMCIA LAN/MODEM CARD with AUI cable connecting to external MAU. TC3399A provides both UTP and AUI interface for maximum flexibility.

Block Diagram



Block Diagram of TC3399A

Pin Configuration



3 Pin Description

PCMCIA Bus Interface Pins

Symbol	Pin No.	I/O	Description
SA0-SA9	2-11	I	The address signal lines of PCMCIA Bus are used to select a register to be read or written and attribute memory enable.
SD0-SD7 SD8-SD15	27-34 93-86	I/O	Register Access, with DMA inactive, SD0-SD7 are used to read/write register data. SD8-SD15 invalid during this state. Remote DMA Bus Cycle, SD0-SD15 contain packet data. direction of transfer is depend on Remote read/write.
RST	35	I/O	RST is active high and places the TC3399A in a reset mode immediately. During falling edge the TC3399A controller loads the configuration from MD0-7, MA0-13.
WAIT*	26	O	This pin is set low to insert wait states during Remote DMA transfer.
REG*	24	I	REG* is an active low input used to determine whether a host access is to Attribute memory (The first 1K) or to common memory (above 1K). If REG* is low the access is to attribute memory, if REG* is high the access is to common memory. REG* is also asserted low for all accesses to the TC3399A IO Registers.
IOR*	21	I	Read Strobe: Strobe from host to read registers or Remote DMA read.
IOW*	22	I	Write Strobe: Strobe from host to read registers or Remote DMA write.
OE*	23	I	Host memory read strobe, when OE* and REG* both low

PCMCIA Bus Interface Pins

Symbol	Pin No.	I/O	Description
			attribute memory can be read. When OE* is low and REG* is high common memory can be read.
WE*	1	I	Host memory write strobe, After Power reset if TC3399A is configured to memory write enable, then WE* and REG* is both low , Attribute memory can be written. When WE* is low and REG* is high common memory can be written.
INPACK*	96	O	Active low signal, asserted if the host access register or Remote DMA read cycle.
IO16*	95	O	IO16* is driven by TC3399A to support host 16 bits access cycle.
INT* (RDY/BSY*)	97	O	While the TC3399A is configured as a memory device, This pin servers as RDY/BSY* pin, If the TC3399A is ready to perform a transfer, this pin is set high. When TC3399A is operation at I/O device, this pin used as interrupt pin. To indicate that the TC3399A require host service. RDY/BSY* state can be read in the pin replacement register. While LAN and MODEM function are enabled and IntSel bit in control Register is a zero. this pin output is logical OR of LAN and MODEM interrupt.
STSCHG*	98	O	STATUS CHANGED. The STSCHG* out is to alter the host to changes in the RDY/BSY* bit in the pin replacement register and to the setting of the RIEvt bit in the I/O event indication register. Optionally, if the RingEn bit in the card configuration and Status Register is set, this pin is used for Ring indication to the host as follows: while the input on the RI* pin is low (no ring), the STSCHG* pin is held high. while the input on the RI* is toggling (ring incoming), STSCHG* is output is low. STSCHG* will also be asserted if the IntSel bit is a one in the TC3399A control register and Ethernet interrupt is becomes active.
SPKR	99	O	When audio bit in the Configuration and Status register is set to high, this pin reflects the signal at the MAUDIO input. When the Audio is a low, this pin is tri-state. A 100K ohm pull-up resister should be added to this pin.
CE1*	20	I	Card enable 1, are active low signals driven by the host. These signals provide a card select based on an address decode (decode by the host).

UART Interface Pins

Symbol	Pin No.	I/O	Description
MRDY	12	I	MRDY LOW indicates that modem is busy initializing the modem after a reset, is in the SLEEP mode or is in STOP mode.
MRESET*	13	0	This output drives an active low reset signal to modem controller and data pump. MRESET* is determined the FUNC bit of the TC3399A configuration option register as well as the state of the PCMCIA RST pin.
MCS*	14	0	This decoded chip select output signal ties to the modem controller chip select pin.
PWDN	15	0	Interface to Rockwell modem chipset: (MA14 is pull-low) , for -PWRDWN function. -PWRDWN: This signal reflects the state of the PwrDwn bit in the Card configuration and Status Register. A LOW state indicates that the PwrDwn bit has been set by the host and that the modem should

UART Interface Pins

Symbol	Pin No.	I/O	Description
			enter the stop mode. Interface to AT&T modem chipset: (MA14 isn't pull-low) This pin server as MPwrDwn pin (Active high). When the host set the Pwrdwn bit in the card configuration and status register. this pin is output high. While loading data from EEPROM. PWDN pin also servers as data output pin., This pin is connected to EEPROM data input pin.
RIOUT	16	I/O	Interface to Rockwell modem chipset: (MA14 is pull-low) for RINGOUTB function. RINGOUTB: This is the Ring signal out for the RC96V24AC/RC14V24AC and R96ACL/RC144ACL modem families. While loading data from EEPROM. this pin also servers as data input pin, This pin is connected to EEPROM data output pin.
MINT	17	I	This input is used for the interrupt driven by modem controller. While LAN and MODEM function are enabled and IntSel bit in control Register is a zero. This input is ORed the interrupt from Ethernet to drive the interrupt pin (INT*) on the PCMCIA bus. While IntSel bit in control Register is a one. Only this input drive interrupt pin (INT*) and Ethernet interrupt drive STSCHG* pin.
RI*	18	I	The ring indicate input is driven by DAA's ring detect circuit. When a telephone ringing signal is being received.
MAUDIO	19	I	This input signal is tied to modem's digital audio circuit. the signal is inverted and passed to the PCMCIA interface bus via SPKR, whenever the Audio bit in the Configuration and Status Register is set to high.

Memory Interface Pins

Symbol	Pin No.	I/O	Description
MD0-7	65-58	I/O	When RST is inactive these pins can be used to access external memory. When RST is active configuration is loaded with the data value on MD0-MD7 pins.
MA4-13 MA14 MA3-1, MA0	79-70 81 82-84, 69	I/O	When RST is inactive These pins drive the memory address bus during DMA access cycle. When RST is active configuration is loaded with the data value on MA0-MA13 pins.
MR*	68	O	Memory Bus Read: Strobes data from the buffer memory into the PECUI via the memory data bus.
MW*	67	O	Memory Bus Write: Strobes data from the PECUI into the external buffer memory via the memory data bus.
CS0*	66	O	Buffer RAM chip select, active low.
EECS	85	O	EEPROM chip select. It is asserted when to access EEPROM.

Clock Interface Pins

Symbol	Pin No.	I/O	Description
X1	54	I	CRYSTAL OR EXTERNAL OSCILLATOR INPUT: 20 MHZ
X2	55	O	CRYSTAL FEEDBACK OUTPUT: Used in crystal connection only.

Network Interface Pins

Symbol	Pin No.	I/O	Description
TD+/-	41,39	O	10BaseT differential transmit drivers.
TDLY+/-	38,40	O	10BaseT wave pre distortion control differential outputs.
RD+/-	42,43	I	10BaseT differential receive input port.
VCOI	51	I	Filter input for data recover analog PLL.
LLED	50	O	Link integral LED driver. During Link loss, output high. During loading EEPROM data, used as Serial clock to the EEPROM.

Network Interface Pins (TC3399A option)

Symbol	Pin No.	I/O	Description
RX+/RX-	45,46	I	10Base5, Receiver input pair to controller.
TX+/TX-	48,49	O	10Base5, Transmit output pair from controller.
CD+/CD-	52,53	I	10Base5, Collision input pair to controller.

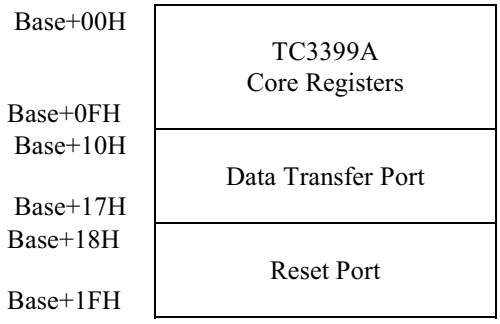
Power Supply Pins

Symbol	Pin No.	I/O	Description
VCC	36,57,80		+5V DC is required. It is suggested that a decoupling capacitor be connected between VCC and GND.
GND	25,37,56,94, 100		
AVDD, AGND	44, 47		Power for analog Phase Lock Loop circuit of PECUI.

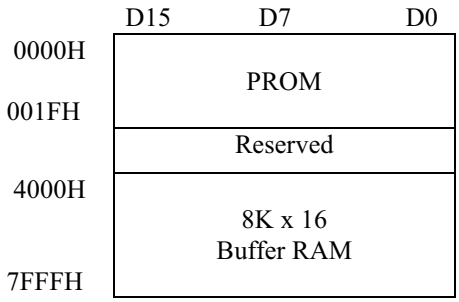
4 Functional Description

I/O PORT ADDRESS MAPPING

This is compatible with Novell's NE2000. The base I/O address of PECUI Controller is configured by Configuration Register (either upon power up or by software writing to this register). At that address the following structure appears.



The registers within this area are 8 bits wide, but the data transfer port is 16 bits wide. By accessing the data transfer port (using I/O instructions) the user can transfer data to or from the PECUI Controller's internal memory. The PECUI Controller's internal memory map is as shown below.



PECUI Core's Memory Map

PROM Location	Location Contents
00h	ETHERNET ADDRESS 0
01h	ETHERNET ADDRESS 1
02h	ETHERNET ADDRESS 2
03h	ETHERNET ADDRESS 3
04h	ETHERNET ADDRESS 4
05h	ETHERNET ADDRESS 5
06-0Dh	RESERVED
0E,0Fh	57h
10-15h	ETHERNET ADDRESS 0-5
16-1Dh	RESERVED
1E-1Fh	42h

Details of PROM Map

PECUI Controller actually has a 64k address range but only does partial decoding on these devices. The PROM data is mirrored at all decodes up to 4000H and the entire map is repeated at 8000H. To access either the PROM or the RAM the user must initiate a Remote DMA transfer between the I/O port and memory.

Remote Read/Write Cache:

The PECUI Controller includes 4 words cache internally. On a remote read the PECUI Controller moves data from external memory buffer to the internal cache buffer, the PECUI moves data continuously until the cashe buffer is full. On a remote write the system can writes data into the cache buffer until the 4 words cache buffer is full.

PCMCIA CIS Structures & Decode Function:

The TC3399A supports access to 1K of attribute Memory. Attribute memory is defined by the PCMCIA standard to be comprised of the card information structure and four 8-bits Card Configuration Registers. These four registers are contained in the TC3399A.
The attribute Memory (only even address can be accessed) map for a PCMCIA card is shown below.

Address	Description
00H-3E0H	Card's information structure
3F0H (CCR4)	I/O Event indication Register
3F2H (CCR5)	Control Register
3F4H-3F6H	Reserved

Address	Description
3F8H(CCR0)	Configuration Option Register
3FAH(CCR1)	Card Configuration and Status Register
3FCH(CCR2)	Pin Replacement Register
3FEH(CCR3)	Reserved
400H-FFFFH	Common Memory

Card Option Registers 0 (R/W) : 3F8H (CCR0)

D7	D6	D5	D4	D3	D2	D1	D0
SRESET	XX	PCMIOEN	FUNC	MIO1	MIO0	PJ1	PJ0

Name	Description
PJ0-PJ1	If MA12 pulled low during power on reset and FUNC=0, The two bits select one of 4 ethernet I/O base address.
MIO0-MIO1	If MA12 pulled low during power on reset and Modem function is enabled, The two bits select one of 3 COM I/O base address.
FUNC	The bit allows the user to enable LAN or MODEM function.
PCMIOEN	To set high make the card enter I/O mode.
XX	Reserved
SRESET	Setting this bit to high, place the card into reset mode.

MA12 isn't pull-low during power on reset:

Ethernet and Modem I/O base

FUNC	MIO1	MIO0	I/O ADDRESS BASE	DESCRIPTION
0	0	0	300H,320H,340H,360H	LAN ONLY
0	0	1	300H,320H,340H,360H 2F8H,3E8H,2E8H	LAN COM
1	0	1	2F8H,3E8H,2E8H	COM ONLY

MA12 pull low during power on reset:

Ethernet I/O address range

PJ1	PJ0	ADDRESS RANGE
0	0	300H-31FH
0	1	320H-33FH
1	0	340H-35FH
1	1	360H-37FH

Modem I/O address range

FUNC	MIO1	MIO0	ADDRESS RANGE	DESCRIPTION
0	0	0	Depend on PJ1,0	LAN ONLY
0	0	1	PJ1,0 2F8H-2FFH	LAN AND COM2
0	1	0	PJ1,0 3E8H-3EFH	LAN AND COM3
0	1	1	PJ1,0 2E8H-2EFH	LAN AND COM4

1	0	0	XX	NO DEFINE
1	0	1	2F8H-2FFH	COM2 ONLY
1	1	0	3E8H-3EFH	COM3 ONLY
1	1	1	2E8H-2EFH	COM4 ONLY

Card Configuration and Status Registers 0 (R/W) : 3FAH (CCR1)

D7	D6	D5	D4	D3	D2	D1	D0
Changed	Sigchg	XX	RingEn	Audio	PwrDwn	Ireq	XX

Name	Description
Ireq	Interrupt. This bit describes the interrupt signal of LAN and MODEM
PwrDwn	power down. This bit is set to one by the host to request the MODEM chipset enter power down mode.
Audio	To set this bit make audio signal from MAUDIO pin pass to SPKR pin on PCMCIA bus.
RingEn	This bit is set by host to enable a Ring indication signal on STSCHG* pin. When this bit is zero, the state of STSCHG* is controlled by the Sigchg and Change bits.
Sigchg	This bit is set/reset by the host to enable/disable a state-changed signal from the status register. When this bit is set to one and RingEn bit is zero, the Changed bit controls STSCHG* pin, If both the Sigchg bit and RingEn bit are set to a zero, then STSCHG* pin is always held HIGH.
Changed	This bit is logical OR of CRdy/Bsy* and RIEvt bit state. When the Sigchg bit is a one and the RingEn bit is a zero, the STSCHG* pin is low whenever the changed bit is a one.

Card Configuration and Status Registers 0 (R/W) : 3FCH (CCR2)

D7	D6	D5	D4	D3	D2	D1	D0
XX	XX	CRdy/Bsy*	XX	XX	XX	RRDY/BSY*	XX

Name	Description
RRDY/BSY*	When read, this bit represents the internal state of the RDY/BSY* signal, When written, this bit acts as a mask for writing the CRdy/Bsy* bit on that write cycle (e.g. to write a one to bit 5, the host writes 22h to this register, and to reset bit 5 to a zero, the host writes 02h to this register).
CRdy/Bsy*	This bit is set to a one when the bit RRDY/BSY* changes state, and may also be written by the host if a one is simultaneously written to bit 1 of this register.

I/O Event Indication Registers 0 (R/W) : 3F0H (CCR4)

D7	D6	D5	D4	D3	D2	D1	D0
XX	XX	XX	RIEvt	XX	XX	XX	RIEnab

Name	Description
RIEnab	Setting this bit to a one enables the setting of the Changed bit when the RIEvt bit is set.
RIEvt	This bit is latched to a one at the start of each ring frequency cycle to indicate line ringing. the host writes a one to reset it.

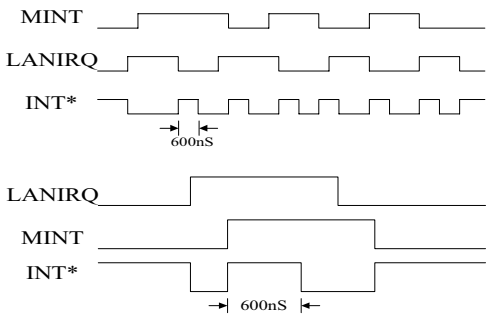
Control Registers 0 (R/W) : 3F2H (CCR5)

D7	D6	D5	D4	D3	D2	D1	D0
XX	XX	XX	XX	IntSel	XX	Mreset	Mintsel

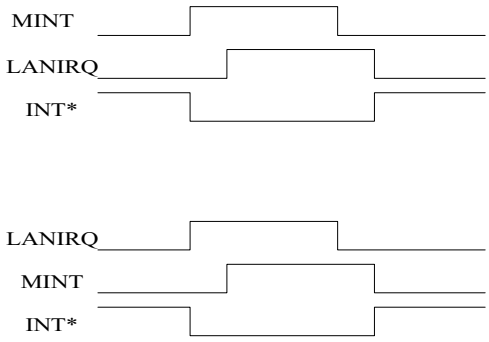
Name	Description
IntSel	Interrupt select. This bit allows the user to select two different interrupt schemes. When this bit is high, the modem interrupt drives INT* and the Ethernet interrupt appear at STSCHG* pin. A zero in this bit, the logical OR of Ethernet and Modem interrupt drive INT* pin.
Mreset	Modem reset. Setting this bit a one, MRESET* output low to reset Modem controller and data pump.
Mintsel	At shared interrupt, this bit controls the generation of interrupts, Which includes "Interrupt Regeneration Mode" and "Equal priority mode". 1. Interrupt Regeneration Mode : Mintsel=0, InSel=0. During Modem [LAN] interrupt period, If LAN [Modem] interrupt is asserted, INT* stay at low. After Modem [LAN] interrupt is cleared, INT* go high for approximately 600nS and then stay at low until LAN interrupt is cleared. 2. Equal priority mode : Mintsel=1, InSel=0. The interrupts are OR'ed together so that INT* will be low when either the modem or the LAN interrupt is asserted. If the interrupts overlap, then INT* will remain low until both are cleared.

The shared interrupt control

1.Interrupt Regeneration mode:Mintsel=0,IntSel=0.



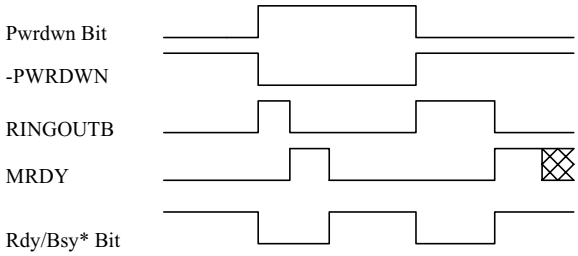
2.Equal priority mode:Mintsel=1,IntSel=0.



Power Down Mode Control

Power down mode controls is provided to support the operation of the lowest power mode (stop mode).Sleep mode is the normal power down mode entered automatically during periods of inactivity, When the PwrDwn bit is set in the CCR1, all accesses to the modem UART interface blocked. Additionally, the modem will not be awakened by telephone line ringing because pass through of Ring signals on the RI* pin is blocked.
While the modem is in a power mode, Mutually exclusive call indication pass through methods are a (using the I/O Event Indicate indication Register or b) enabling the RingEn bit in CCR1.
I/O event indication register : The RIEvt bit is latched a one upon detection of a RI* signal rising edge. The host can poll RIEvt at any time (even during power down mode) because the PECUI CCR1 interface remains active at all times. Furthermore, if the RIEnab bit is set to a one by the host, enabling indication of state changes on the STSCHG* pin.
RingEn bit in the CCR1 : STSCHG* becomes a Ring indication signal when the RingEn bit is set to a one by the host. During the ring On period, STSCHG* is held low. during the ringing off period and when there is no incoming Ring

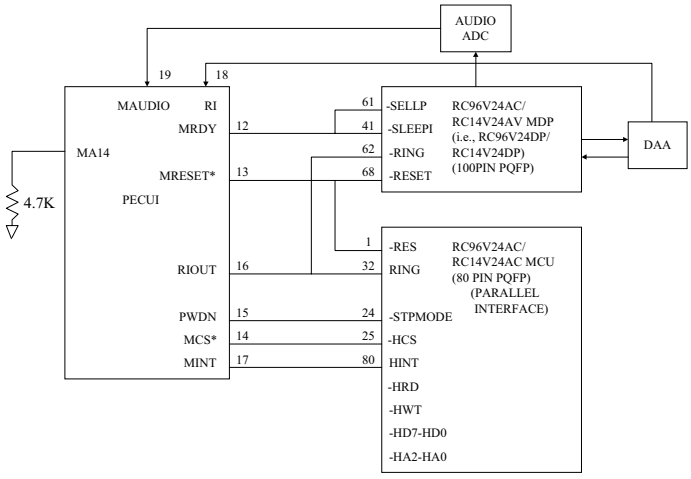
signal, STSCHG* is held high. when the RingEn function is enabled, all other state change indications on STSCHG* are disabled.



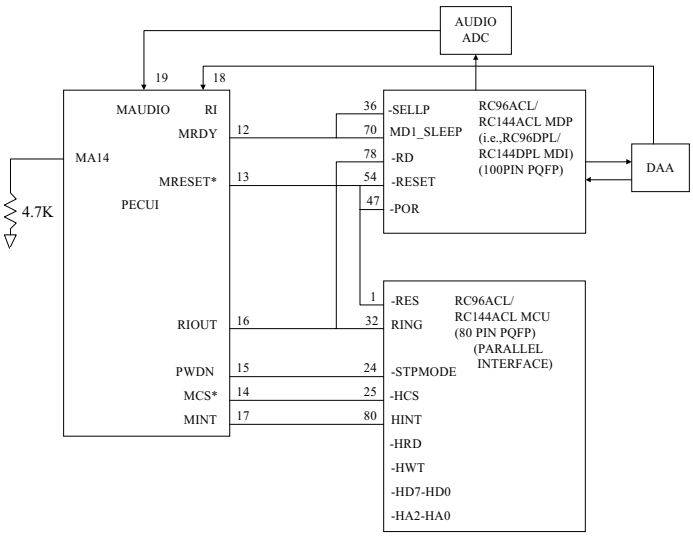
*Grey areas indicate that the modem may be in Sleep Mode

RC96V24AC/RC14VAC and RC96ACL/RC144ACL
Modem Families Power Down/Up Signal State Diagram

Interface Modem Families :



PECUI to RC96V24AC/RC14V24AC Modem Interface



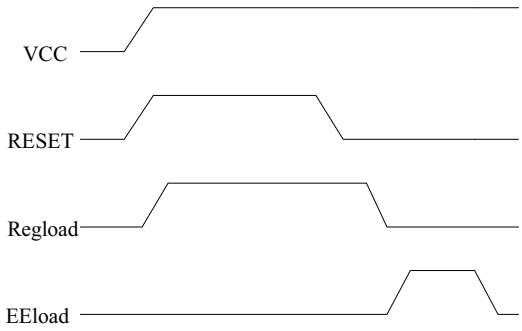
PECUI to RC96ACL/RC144ACL Modem Interface

4.1 Power On Configuration

The PECUI Controller configures itself after a RST signal is applied. When a Power-On-Reset occurs the PECUI Controller latches in the values on the configuration pins and uses these to configure the internal registers and options. Internally these pins contain pull-up resistance. If any pins are unconnected they have a default logic. The configuration registers are loaded from the memory data bus when RST goes inactive.

A Power-On-Reset also causes the PECUI Controller to load the internal PROM store from the EEPROM, which can take up to 3 ms. This Occurs after Config-Regs. has completed. If EECONFIG is high (MA9 pull down) the configuration data loaded on the falling edge of RST will be overwritten with data read from the serial EEPROM. Regardless of the level on EECONFIG the PROM store will always be loaded with data from the serial EEPROM during the time specified as EELOAD.

Figure 1 shows how the RESET circuitry operates.



The PECUI Controller users an 93C56/66, The programmed contents of the EEPROM is shown as following.

	D15	D0
.....	CIS byte n	CIS byte n-1
.....		
16H	.....	.....
14H	.....	.....
12H	CIS byte 3	CIS byte 2
10H	CIS byte 1	CIS byte 0
0FH	Not Used	Reserved
0EH	Config. B	Config. A
	Reserved	Reserved
08H	42H	42H
07H	57H	57H
04H	Reserved	Reserved
03H	Reserved	bit (0) : 8 bit enable, bit (7:0) : Reserved
02H	E'net Address 5	E'net Address 4
01H	E'net Address 3	E'net Address 2
00H	E'net Address 1	E'net Address 0

**03H bit (0) : If MA11 is pulled low during power on reset, This bit is setting high. TC3399A can work at NE2000's 8 bit mode.

EEPROM Programming Map

Storing and Loading configuration from EEPROM:

If the EECONFIG is set high (MA9 pull low) during boot up the PECUI Controller's configuration is read from the EEPROM, before the PROM data is read. The configuration data is stored within the address 0EH,0FH of the EEPROM's address space. Configuration Register A and B are located in the address 0EH.
To write this configuration into the EEPROM, The user can program register in PECUI's address 02H of page 3. This operation will work regardless of the level on EECONFIG.

5 Configuration Registers

Configuration Register A (R/W)

To prevent any accidental writes of this register it is"hidden" behind a previously unused register. Register 0AH in the PECUI Controller's Page 0 of registers was previously reserved on a read. Now Configuration Register A can be read at that address and can be written to by following a read to 0AH with a write to 0AH. If any other PECUI Controller register accesses take place between the read and the write then the write to 0AH will access the Remote Byte Count Register 0.

7	6	5	4	3	2	1	0
XX	FREAD	XX	XX	XX	XX	XX	XX

FREAD : The PECUI Controller supports 4 words Remote DMA read/write cache. When this bit is set high, Remote DMA cache control will be enabled.
XX : Reserved

Configuration Register B (R/W)

To prevent any accidental writes of his register it is "hidden" behind a previously unused register. Register 0BH in the PECUI Controller's Page 0 of registers was previously reserved on a read. Now Configuration Register B can be read at that address and can be written to by following a read to 0BH with a write to 0BH. If any other PECUI Controller register accesses take place between the read and the write then the write to 0BH will access the Remote Byte Count Register 1.

7	6	5	4	3	2	1	0
XX	LINK /IOEN	MINT	LINT	IO16CON	GDLINK	PHYS1	PHYS0

PHYS1,0 : PHYSICAL LAYER INTERFACE

0	0	AUTO DETECT
0	1	RESERVED
1	0	10Base5
1	1	10BaseT

In auto detect mode. MA10 open for 10BaseT or 10Base5 auto_detect (TC3399A option).

GDLINK : When this bit is high, to disable link test pulse generation and integrity checking.
IO16CON : When this bit is set high the Controller generates IO16* after REG* and CE1* active. If low this output is generated only on address decode.
MINT : MINT input signal status indicate.
LINT : Internal LAN interrupt status indicate. To write a one to this bit can reset it.
LINK : When this bit is high, link test integrity checking is Good.
Otherwise, indicate link signal Loss.

XX : Reserved.

Hardware Configuration:

These functions are configured during a power on RESET.

EECFG(MA9) : If MA9 is pull down. enable CFGA, CFGB load from EEPROM.
AUICB(MA10) : In media physic auto detect mode, for 10BaseT or 10Base5 auto_detect. It should be opened.
ENG8(MA11) : If MA11 is pull down and EEPROM 03H bit(0) is setting high, PECUI can work at NE2000 8 bit mode. otherwise, at 16 bit mode.
IOSP(MA12) : If MA12 is pull down, enable I/O base 300H, 320H, 340H, and 360H separately. If MA12 isn't pulled low, despite of the value of PJ1,0, TC3399A response to I/O access at the I/O baseaddress 300h, 320h, 340h, 360h.
RCON(MA0) : Reserved.
ATNT(MA14) : If MA14 is pull down, Interface to Rockwell Modem families, If MA14 isn't pulled down, Interface to AT&T Modem families.

Programming Register (R/W)

The PECUI Controller enable software (driver) programming EEPROM or testing interrupt signal through this register directly. It is located at PECUI's core register Page3 base+02H.

7	6	5	4	3	2	1	0
EESEL	FIRQ	XX	READ	CS	SK	DI	DO(r) ATTRDIS

EESEL,CS,SK,DI,DO : The software can read or programming serial EEPROM directly through access these bits. EESEL should be set high before starting the EEPROM read/write.
FIRQ : The PECUI interrupt signal IRQ will be asserted when this bit is set high.
READ : PECUI can reload CFGA,CFGB and internal PROM if this bit is set high. When reload state is completed, READ will be cleared to low.
ATTRDIS: Attribute and common memory access will be disable if it is programmed to high.
NOTE : DO : read only
ATTRDIS : write only

5.1 PECUI Core Registers

All registers are 8-bit wide and mapped into two pages which are selected in the Command Register(PS0,PS1). Pins A0-A3 are used to address registers within each page. Page 0 register are those registers which are commonly accessed during PECUI Controller operation while Page 1 registers are used primarily for initialization. The registers are partitioned to avoid having to perform two read/write cycles to access commonly used registers.

Register Assignments:

Page 0 Address Assignments(PS1=0,PS0=0)

A0-A3	RD	WR
00H	Command(CR)	Command(CR)
01H	Current Local DMA Address 0 (CLDA0)	Page Start Register (PSTART)
02H	Current Local DMA Address 1 (CLDA1)	Page Stop Register (PSTOP)
03H	Boundary Pointer (BNRY)	Boundary Pointer (BNRY)
04H	Transmit Status Register(TSR)	Transmit Page Start Address (TPSR)
05H	Number of Collisions Register(NCR)	Transmit Byte Count Register 0 (TBCR0)

Page 0 Address Assignments(PS1=0,PS0=0)

A0-A3	RD	WR
06H	FIFO(FIFO)	Transmit Byte Count Register 1 (TBCR1)
07H	Interrupt Status Register(ISR)	Interrupt Status Register(ISR)
08H	Current Remote DMA Address 0(CRDA0)	Remote Start Address Register 0(RSAR0)
09H	Current Remote DMA Address 1(CRDA1)	Remote Start Address Register 1(RSAR1)
0AH	Config. Register A (CFGA)	Remote Byte Count Register 0(RBCR0)
0BH	Config. Register B (CFGB)	Remote Byte Count Register 1(RBCR1)
0CH	Receive Status Register(RSR)	Receive Configuration Register(RCR)
0DH	Tally Counter 0(Frame alignment Errors) (CNTR0)	Transmit Configuration Register(TCR)
0EH	Tally Counter 1 (CRC errors) (CNTR1)	Data Configuration Register(DCR)
0FH	Tally Counter 2 (Missed Packet Errors) (CNTR2)	Interrupt Mask Register(IMR)

Register Assignments:

Page 1 Address Assignments(PS1=0,PS0=1)

A0-A3	RD	WR
00H	Command(CR)	Command(CR)
01H	Physical Address Register 0(PAR0)	Physical Address Register 0(PAR0)
02H	Physical Address Register 1(PAR1)	Physical Address Register 1(PAR1)
03H	Physical Address Register 2(PAR2)	Physical Address Register 2(PAR2)
04H	Physical Address Register 3(PAR3)	Physical Address Register 3(PAR3)
05H	Physical Address Register 4(PAR4)	Physical Address Register 4(PAR4)
06H	Physical Address Register 5(PAR5)	Physical Address Register 5(PAR5)
07H	Current Page Register(CURR)	Current Page Register(CURR)
08H	Multicast Address Register 0(MAR0)	Multicast Address Register 0(MAR0)
09H	Multicast Address Register 1(MAR1)	Multicast Address Register 1(MAR1)
0AH	Multicast Address Register 2(MAR2)	Multicast Address Register 2(MAR2)
0BH	Multicast Address Register 3(MAR3)	Multicast Address Register 3(MAR3)
0CH	Multicast Address Register 4(MAR4)	Multicast Address Register 4(MAR4)
0DH	Multicast Address Register 5(MAR5)	Multicast Address Register 5(MAR5)
0EH	Multicast Address Register 6(MAR6)	Multicast Address Register 6(MAR6)
0FH	Multicast Address Register 7(MAR7)	Multicast Address Register 7(MAR7)

Page 2 Address Assignments(PS1=1,PS0=0)

A0-A3	RD	WR
00H	Command(CR)	Command(CR)
01H	Page Start Register (PSTART)	Current Local DMA Address 0(CLDA0)
02H	Page Stop Register (PSTOP)	Current Local DMA Address 1(CLDA1)

Page 2 Address Assignments(PS1=1,PS0=0)

A0-A3	RD	WR
03H	Remote Next Packet Pointer	Remote Next Packet Pointer
04H	Transmit Page Start Address(TPSR)	Reserved
05H	Local Next Packet Pointer	Local Next Packet Pointer
06H	Address Counter (Upper)	Address Counter (Upper)
07H	Address Counter (Lower)	Address Counter (Lower)
08H	Reserved	Reserved
09H	Reserved	Reserved
0AH	Reserved	Reserved
0BH	Reserved	Reserved
0CH	Receive Configuration Register(RCR)	Reserved
0DH	Transmit Configuration Register(TCR)	Reserved
0EH	Data Configuration Register(DCR)	Reserved
0FH	Interrupt mask Register(IMR)	Reserved

Note: Page 2 registers should only be accessed for diagnostic purposes. They should not be modified during normal operation. Page 3 Reserved should never be modified.

Register Assignments:

Page 3 Address Assignments(PS1=1,PS0=1)

A0-A3	RD	WR
00H	Command(CR)	Command(CR)
01H	Reserved	Reserved
02H	Programming Reg.	Programming Reg.
03H	Reserved	Reserved
04H	Reserved	Reserved
05H	Reserved	Reserved
06H	Reserved	Reserved
07H	Reserved	Reserved
08H	Reserved	Reserved
09H	Reserved	Reserved
0AH	Reserved	Reserved
0BH	Reserved	Reserved
0CH	Reserved	Reserved
0DH	Reserved	Reserved
0EH	Reserved	Reserved
0FH	Reserved	Reserved

Register Descriptions:

Command Register (CR) (Read/Write)

The Command Register is used to initiate transmissions, enable or disable Remote DMA operations and to select register pages. To issue a command the microprocessor sets the corresponding bit(s) (RD2,RD1,RD0,TXP). Further commands may be overlapped, but with the following rules:(1) if a transmit command overlaps with a remote DMA operation, bits RD0,RD1, and RD2 must be maintained for the remote DMA command when setting the TXP bit. Note, if a remote DMA command is re-issued when giving the transmit command, the DMA will complete immediately if the remote byte count register have not been reinitialized. (2) if a remote DMA operation overlaps a transmission, RD0,RD1, and RD2 may be written with the desired values and a "0"to this bit has no effect. (3) A remote write DMA may not overlap remote read operation or visa versa. Either of these operations must either complete or be aborted before the other operation may start. Bits PS1,PS0,RD2, and STP may be set any time.

7	6	5	4	3	2	1	0
PS1	PS0	RD2	RD1	RD0	TXP	STA	STP

Bit	Symbol	Description
D0	STP	Stop:Software reset command, takes the controller offline, no packets will be received or transmitted. Any reception of transmission in progress will continue to completion before entering the reset state. To exit this state, the STP bit must be reset. The software reset has executed only when indicated by the RST bit in the ISR being set to a 1. STP powers up high.
D1	STA	Start:This bit is used to active the PECUI core after either power up, or when the PECUI cord has been placed in a reset mode by software command. STA power up low.
D2	TXP	Transmit Packet:This bit must be set to initiate transmission of a packet. TXP is internally reset either after the transmission is completed or aborted. this bit should be set only after the Transmit Byte Count and Transmit Page Start registers have been programmed. TXP powers up low.
D3-D5	RD0-RD2	Remote DMA Command:These three encoded bits control operation of the Remote DMA channel. RD2 can be set to about any Remote DMA command in progress. The Remote Start Addresses are not restored to the starting address if the Remote DMA is aborted. RD2 powers up high. RD2 RD1 RD0 0 0 0 Not Allowed 0 0 1 Remote Read 0 1 0 Remote Write (Note) 0 1 1 Send Packet 1 X X Abort/Complete Remote DMA (Note)
D6,D7	PS0,PS1	Page Select:Three two encoded bits select which register page is to be accessed with addresses A0-3. PS1 PS0 0 0 Register Page 0 0 1 Register Page 1 1 0 Register Page 2 1 1 Register Page 3

Data Configure register (DCR)

This Register is used to program the PECUI for 8 or 16-bit memory interface, select byte ordering in 16-bit applications and establish FIFO thresholds. The DCR must be initialized prior to loading the Remote Byte count Registers.

7	6	5	4	3	2	1	0
-	FT1	FT0	ARM	LS	-	-	WTS

Bit	Symbol	Description
D0	WTS	Word Transfer Select 0: Selects byte-wide DMA transfers. 1: Selects word-wide DMA transfers Note:when word-wide mode is selected, up to 32k words are addressable; A0 remains low.
D1	-	Reserved
D2	-	Reserved
D3	LS	Loopback Select 0: Loopback mode selected. Bits D1,D2 of the TCR must also be programmed for Loopback mode selected. 1: Normal Operation.
D4	ARM	Auto-Initialize Remote 0: Send Command not executed, all packets removed from Buffer Ring under program control. 1: Send Command executed, Remote DMA auto-initialized to remove packets from Buffer Ring.
D5,D6	FT0,FT1	FIFO Threshold Select:Encoded FIFO threshold. During reception, the FIFO threshold indicates the number of bytes (or words) the FIFO has filled serially from the network before the FIFO is emptied onto memory bus. RECEIVE THRESHOLDS FT1 FT0 Word Wide Byte Wide 0 0 1 Word 2 Bytes 0 1 2 Word 4 Bytes 1 0 4 Word 8 Bytes 1 1 6 Word 12 Bytes During transmission, the FIFO threshold indicates the number of bytes (of words) the FIFO has filled from the Local DMA before being transferred to the memory. Thus, the transmission threshold is 16 bytes less the receive threshold.

Transmit configuration Register (TCR)

The transmit configuration establishes the actions of the transmitter section of the PECUI during transmission of a packet on the network, LB1 and LB0 power up as 0.

7	6	5	4	3	2	1	0
-	-	-	OFST	ATD	LB1	LB0	CRC

Bit	Symbol	Description
D0	CRC	Inhibit CRC 0: CRC appended by transmitter 1: CRC inhibited by transmitter
D1,D2	LB0,LB1	Encoded Loopback Control:These encoded configuration bits set the type of loopback that is to be performed. Note that loopback in mode 2 sets the LPBK pin high, this places the TC3096 in loopback mode and that D3 of the DCR must be

Bit	Symbol	Description
		set to zero for loopback operation. LB1 LB0 Mode0 0 0 Normal Operation (LPBK=0) Mode1 0 1 Internal Loopback (LPBK=0) Mode2 1 0 External Loopback (LPBK=1) Mode3 1 1 External Loopback (LPBK=0)
D3	ATD	Auto Transmit Disable:This bit allows another station to disable the PECUI'S transmitter by transmission of a particular multicast packet. The transmitter can be re-enabled by resetting this bit or by reception of a second particular multicast packet. 0: Normal Operation 1: Reception of multicast address hashing to 62 bit disables transmitter, reception of multicast address hashing to bit 63 enables transmitter.
D4	OFST	Collision Offset Enable:This bit modifies the back off algorithm to allow prioritization of nodes. 0: Backoff Logic implements normal algorithm. 1: Forces Backoff algorithm modification to 0 to $2^{mim(3+n,10)}$ slot times for first three collisions, Then follows standard backoff. (For first three collisions station has higher average backoff delay making a low priority mode.)
D5	-	Reserved
D6	-	Reserved
D7	-	Reserved

Transmit Status Register (TSR)

This register records events that occur on the media during transmission of a packet. It is cleared when the next transmission is initiated by the host. All bits remain low unless the event that corresponds to a particular bit occurs during transmission. Each transmission should be followed by a read of this register. The contents of this register are not specified until after the first transmission.

7	6	5	4	3	2	1	0
OWC	CDH	FU	CRS	ABT	COL	-	PTX

Bit	Symbol	Description
D0	PTX	Packet Transmitted: Indicates transmission without error (No excessive collisions or FIFO underrun) (ABT="0",FU="0").
D1	-	Reserved
D2	COL	Transmit Collided: Indicates that the transmission collided at least once with another station on the network. The number of collisions is recorded in the Number of Collisions Registers. (NCR).
D3	ABT	Transmit Aborted: Indicates the PECUI aborted transmission because of excessive collisions. (Total number of transmissions including original transmission attempt equals 16).
D4	CRS	Carrier Sense Lost: This bit is set when carrier is lost during transmission of the packet. Carrier Sense is monitored from the end of Preamble/Synch until TXE is dropped. Transmission is not aborted on loss of carrier.

Bit	Symbol	Description
D5	FU	FIFO Underrun: If the PECUI cannot gain access of the bus before the FIFO empties, this bit is set. Transmission of the packet will be aborted.
D6	CDH	CD Heartbeat: Failure of the transceiver to transmit a collision signal after transmission of a packet will set this bit. The collision Detect (CD) heartbeat signal must commence during the first 6.4us of the interframe Gap following a transmission. In certain collisions, the CD Heartbeat bit will be set even though the transceiver is not performing the CD heartbeat test.
D7	OWC	Out of Window Collision: Indicates that a collision occurred after a slot time (51.2us). Transmissions rescheduled as in normal collisions.

Receive Configuration Register (RCR)

This register determines operation of the PECUI during reception of a packet and is used to program what types of packets to accept.

7	6	5	4	3	2	1	0
-	-	MON	PRO	AM	AB	AR	SEP

Bit	Symbol	Description
D0	SEP	Save Errored Packets 0: Packets with receive errors are rejected. 1: Packets with receive errors are accepted. Receive errors are CRC and Frame Alignment errors.
D1	AR	Accept Runt Packets 0: Packets with fewer than 64 bytes rejected. 1: Packets with fewer than 64 bytes accepted.
D2	AB	Accept Broadcast 0: Packets with all 1's broadcast destination address rejected. 1: Packets with all 1's broadcast destination address accepted.
D3	AM	Accept Multicast 0: Packets with multicast destination address not checked. 1: Packets with multicast destination address checked.
D4	PRO	Promiscuous Physical 0: Physical address of node must match the station address programmed in PAR0-PAR5. (Physical address checked) 1: All packets with any physical address accepted. (physical address not checked)
D5	MON	Monitor Mode: Enables the receiver to check addresses and CRC on incoming packets without buffering to memory. The missed packet Tally counter will be incremented for each recognized packet. 0: Packets buffered to memory. 1: Packets checked for address match, good CRC and frame Alignment but not buffered to memory.
D6	-	Reserved
D7	-	Reserved

Note: D2 and D3 are "OR'd" together, i. e., if D2 and D3 are set the PECUI will accept broadcast and multicast addresses as well as its own physical address. To establish full promiscuous mode, bits D2,D3 and D4 should be set. In addition the multicast hashing array must be set to all 1's in order to accept all multicast addresses.

Receive Status Register (RSR)

This register records status of the received packet, including information on errors and the type of address match, either physical or multicast. The contents of this register are written to buffer memory by the DMA after reception of a good packet. If packets with errors are to be saved the receive status is written to memory at the head of the erroneous packet if an erroneous packet is received. If packets with errors are to be rejected the RSR will not be written to memory. The contents will be cleared when the next packet arrives. CRC errors. frame Alignment errors and missed packets are counted internally by the PECUI which relinquishes the Host from reading the RSR in real time to record errors for Network Management functions. The contents of this register are not specified until after the first reception.

7	6	5	4	3	2	1	0
DFR	DIS	PHY	MPA	FO	FAE	CRC	PRX

Bit	Symbol	Description
D0	PRX	Packet Received Intact: Indicates packet received without error. (Bits CRC, FAE, FO and MPA are zero for the received packet.)
D1	CRC	CRC Error: Indicates packet received with CRC error. Increments Tally Counter (CNTR1). This bit will also be set for Frame Alignment errors.
D2	FAE	Frame Alignment Error: Indicates that the incoming packet did not end on a byte boundary and the CRC did not match at last byte boundary. Increments Tally counter (CNTR0).
D3	FO	FIFO Overrun: This bit is set when the FIFO is not serviced causing overflow during reception. Reception of the packet will be aborted.
D4	MPA	Missed Packet: Set when packet intended for node cannot be accepted by PECUI because of a lack of receive buffers of if the controller is in monitor mode and did not buffer the packet to memory. Increments Tally Counter (CNTR2).
D5	PHY	Physical/Multicast Address: Indicates whether received packet had a physical or multicast address type 0: Physical Address Match 1: Multicast/Broadcast Address Match
D6	DIS	Receiver Disabled: Set when receiver disabled by entering Monitor mode. Reset when receiver is re-enabled when exiting Monitor mode.
D7	DFR	Deferring : Set when CRS or COL inputs are active. If the transceiver has asserted the CD line as a result of the jabber, this bit will stay set indicating the jabber condition.

Note: Following coding applies to CRC and FAE bits

FAE	CRC	Type of Error
0	0	No error (Good CRC and <6 Dribble Bits)
0	1	CRC ERROR
1	0	Legal, will not occur
1	1	Frame Alignment Error and CRC Error

Interrupt Mask Register (IMR)

The interrupt Mask Register is used to mask interrupts. Each interrupt mask bit corresponds to a bit in the Interrupt Status Register (ISR). If an interrupt mask bit is set an interrupt will be issued whenever the corresponding bit in the ISR is set. If any bit in the IMR is set low, an interrupt will not occur when the bit in the ISR is set. The IMR powers up all zeroes.

7	6	5	4	3	2	1	0
-	RDCE	CNTE	OVWE	TXEE	RXEE	PTXE	PRXE

Bit	Symbol	Description
D0	PRXE	Packet Received Interrupt Enable: Enables Interrupt when packet received.
D1	PTXE	Packet Transmitted Interrupt Enable: Enables Interrupt when packet is transmitted.
D2	RXEE	Receive Error Interrupt Enable: Enables Interrupt when packet received with error.
D3	TXEE	Transmit Error Interrupt Enable: Enables Interrupt when packet transmission results in error.
D4	OVWE	Over Write Warning Interrupt Enable: Enables Interrupt when Buffer management Logic lacks sufficient buffers to store incoming packet.
D5	CNTE	Counter Overflow Interrupt Enable: Enables Interrupt when MSB of one or more of the Network Tally counters has been set.
D6	RDCE	DMA Complete Interrupt Enable: Enables Interrupt when Remote DMA transfer has been completed.
D7	-	Reserved

Interrupt Status Register (ISR)

This register is accessed to determine the cause of an interrupt. Any interrupt can be masked in the interrupt Mask Register (IMR). Individual interrupt bits are cleared by writing a "1"into the corresponding bit of the ISR. The IRQ signal is active as long as any unmasked signal is set, and will not go low until all unmarked bits in this register have been cleared. The ISR must be cleared after power up by writing it with all 1's.

7	6	5	4	3	2	1	0
RST	RDC	CNT	OVW	TXE	RXE	PTX	PRX

Bit	Symbol	Description
D0	PRX	Packet Received: Indicates packet received with no errors.
D1	PTX	Packet Transmitted: Indicates packet transmitted with no errors.
D2	RXE	Receive Error: Indicates that a packet was received with one or more of the following errors: - CRC Error - Frame Alignment Error - FIFO Overrun - Missed Packet
D3	TXE	Transmit Error: Set when packet transmitted with one or more of the following errors: - Excessive Collisions - FIFO Underrun
D4	OVW	Over Write Warning: Set when receive buffer ring storage resources have been exhausted. (Local DMA has reached Boundary Pointer).
D5	CNT	Counter Over flow: Set when MSB of one or more of the Network Tally Counters has been set.
D6	RDC	Remote DMA Complete: Set when Remote DMA operation has been completed.
D7	RST	Reset Status: A status indicator with no interrupt generated - Set when PECUI enters reset state and is cleared when a start command

Bit	Symbol	Description
		is issued - Set when a Receive Buffer Ring overflows and is cleared when leaves overflow status. Writing to this bit has no effect and powers up high.

Network Tally Counter Registers (CNTR)

Three 8-bit counters are provided for monitoring the number of CRC errors, Frame Alignment Errors and missed packets, The maximum count reached by any counter is 192 (C0H). These registers will be cleared when read by the CPU. The count is recorded in binary in CT0-CT7 of each Tally Register.

CNTR0: Monitor the number of Frame Alignment error

7	6	5	4	3	2	1	0
CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

CNTR1: Monitor the number of CRC error

7	6	5	4	3	2	1	0
CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

CNTR2: Monitor the number of Missed Packets

7	6	5	4	3	2	1	0
CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Number of Collisions Register (NCR)

This register contains the number of collisions a node experiences when attempting to transmit a packet. If no collisions are experienced during a transmission attempt, the COL bit of the TSR will be set and the contents of NCR will be zero. If there are excessive collisions, the ABT bit in the TSR will not be set and the contents of NCR will be zero. The NCR is cleared after the TXP bit in the CR is set.

7	6	5	4	3	2	1	0
-	-	-	-	NC3	NC2	NC1	NC0

FIFO Register (FIFO)

This is an eight bit register that allows the CPU to examine the contents of the FIFO after loopback. The FIFO will contain the last 8 data bytes transmitted in the loopback packet. Sequential reads from the FIFO will advance a pointer in the FIFO and allow reading of all 8 bytes. Note that the FIFO should only be read when the PECUI has been programmed in loopback mode.

7	6	5	4	3	2	1	0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Physical Address Register (PAR0-PAR5)

The physical address registers are used to compare the destination address of incoming packets for rejecting or accepting packets. Comparisons are performed on a byte-wide basis. The bit assignment shown below relates the sequence in PAR0-PAR5 to the bit sequence of the received packet.

..	Syn	Syn	DA0	DA1	DA2	DA3	DA4	DA5	DA6	DA7	..

|------- Destination Address --------|--- Source

	D7	D6	D5	D4	D3	D2	D1	D0
PAR0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
PAR1	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
PAR2	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
PAR3	DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24
PAR4	DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32
PAR5	DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40

Multicast Address Registers (MAR0-MAR7)

The Multicast address registers provide filtering of multicast addresses hashed by the CRC logic. All destination addresses are fed through the CRC logic and as the last bit of the destination address enters the CRC, the 6 most significant bits of the CRC generator are latched. These 6 bits are then decoded by a 1 of 64 decode to index a unique filter bit (FB0-63) in the multicast address register. If the filter bit selected is set, the multicast packet is accepted. The system designer would use a program to determine which filter bits to set in the multicast registers. For some address found to hash to the value 50 (32H), then FB50 in MAR6 should be initialized to "1" All multicast filter bits that correspond to multicast address accepted by the node are then set to one. To accept all multicast packets all of the registers are set to all ones.

	D7	D6	D5	D4	D3	D2	D1	D0
MAR0	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
MAR1	FB15	FB14	FB13	FB12	FB11	FB10	FB9	FB8
MAR2	FB23	FB22	FB21	FB20	FB19	FB18	FB17	FB16
MAR3	FB31	FB30	FB29	FB28	FB27	FB26	FB25	FB24
MAR4	FB39	FB38	FB37	FB36	FB35	FB34	FB33	FB32
MAR5	FB47	FB46	FB45	FB44	FB43	FB42	FB41	FB40
MAR6	FB55	FB54	FB53	FB52	FB51	FB50	FB49	FB48
MAR7	FB63	FB62	FB61	FB60	FB59	FB58	FB57	FB56

DMA Registers

LOCAL DMA TRANSMIT REGISTERS

	15 8	7 0
(TPSR)	TRANSMIT PAGE START	
(TBCR0,1)	TRANSMIT BYTE COUNT	

LOCAL DMA RECEIVE REGISTERS

	15 8	7 0
(PSTART)	PAGE START	
(PSTOP)	PAGE STOP	
(CURR)	CURRENT	

(BRNY)	BOUNDARY	

	15 8	7 0
(CLDA0,1)	CURRENT LOCAL DMA ADDRESS	

REMOTE DMA REGISTERS

	15 8	7 0
(RSAR0,1)	START ADDRESS	
(RBCR0,1)	BYTE COUNT	

(CRDA0,1)	CURRENT REMOTE DMA ADDRESS	

(i) Local DMA Transmit Registers
Transmit page start register (TPSR):

This register points to the assembled packet to be transmitted. Only the eight higher order addresses are specified since all transmit packets are assembled on 256-byte page boundaries.

7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8

Transmit byte count register0,1 (TBCR0,TBCR1):

These two registers indicate the length of the packet to be transmitted in bytes. The maximum number of transmit bytes allowed is 64k bytes. The ENIPC will not truncate transmissions longer than 1500 bytes.

	7	6	5	4	3	2	1	0
TBCR1	L15	L14	L13	L12	L11	L10	L9	L8

	7	6	5	4	3	2	1	0
TBCR0	L7	L6	L5	L4	L3	L2	L1	L0

(ii) Local DMA Receive Registers
Page start, stop registers (PSTART, STOP):

The Page Start and Page stop Registers program the starting and stopping page of the Receive Buffer Ring. Since the ENIPC uses fixed 256-byte buffers aligned on page boundaries only the upper eight bits of the start and stop address are specified.

	7	6	5	4	3	2	1	0
PSTART PSTOP	A15	A14	A13	A12	A11	A10	A9	A8

Boundary register (BNRY):

This register is used to prevent overflow of the Receive Buffer Ring. Buffer management compares the contents of this register to the next buffer address when linking buffers together. If the contents of this register match the next buffer address the local DMA operation is aborted.

	7	6	5	4	3	2	1	0
BNRY	A15	A14	A13	A12	A11	A10	A9	A8

(iii) Remote DMA registers

Remote Start Address Registers (RSAR0,1):
Remote Byte Count Registers (RBCR0,1):
Remote DMA operations are programmed via the Remote Start Address (RSAR0,1) and Remote Byte Count (RBCR0,1) registers. The Remote Start Address is used to point to the start of the block of data to be transferred and the Remote Byte Count is used to indicate the length of the block (in bytes).

	7	6	5	4	3	2	1	0
RSAR1	A15	A14	A13	A12	A11	A10	A9	A8

	7	6	5	4	3	2	1	0
RSAR0	A7	A6	A5	A4	A3	A2	A1	A0

	7	6	5	4	3	2	1	0
RBCR1	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8

	7	6	5	4	3	2	1	0
RBCR0	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0

Current Page Register:

This register is used internally by the Buffer Management Logic as a backup register for reception. CURR contains the address of the first buffer to be used for a packet reception and is used to restore DMA pointers in the event of receive errors. This register is initialized to the same value as PSTART and should not be written to again unless the controller is Reset.

	7	6	5	4	3	2	1	0
CURR	A15	A14	A13	A12	A11	A10	A9	A8

Current local DMA register 0,1 (CLDA0,1):

These two registers can be accessed to determine the current Local DMA Address.

	7	6	5	4	3	2	1	0
CLDA1	A15	A14	A13	A12	A11	A10	A9	A8

	7	6	5	4	3	2	1	0
CLDA0	A7	A6	A5	A4	A3	A2	A1	A0

Current Remote DMA Address Registers:

The Current Remote DMA Registers contain the current address of the Remote DMA. The bit assignment is shown below:

	7	6	5	4	3	2	1	0
CRDA1	A15	A14	A13	A12	A11	A10	A9	A8

	7	6	5	4	3	2	1	0
CRDA0	A7	A6	A5	A4	A3	A2	A1	A0

6 Absolute Maximum Ratings

AMBIENT TEMPERATURE UNDER BIAS	0°C	TO	70°C
STORAGE TEMPERATURE	-40°C	TO	125°C
VOLTAGE ON ALL INPUT AND OUTPUTS WITH RESPECT TO VSS	-0.5V	TO	7V

7 Standard Test Conditions

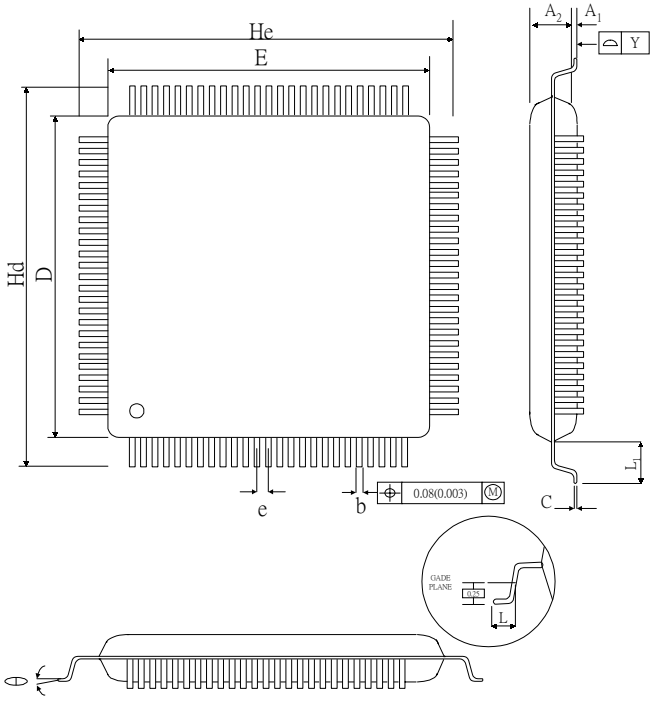
The characteristics below apply for the following standard test conditions.
Unless otherwise noted. All voltages are referred to VSS (0V GROUND), positive current flows into the referred pin.

OPERATING TEMPERATURE RANGE	0°C	TO	70°C
POWER SUPPLY VOLTAGE	4.75V	TO	5.25V

8 D.C. Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
VIL	INPUT LOW VOLTAGE	VSS	-	0.8	V	VCC=5V
VIH	INPUT HIGH VOLTAGE	2.0	-	VCC	V	VCC=5V
IIL	INPUT LOW CURRENT	-	-	-0.5	uA	VIN=1.0V
IIH	INPUT HIGH CURRENT	-	-	20	uA	VIN=VCC
VOL	OUTPUT LOW VOLTAGE	-	-	0.4	V	IOL=8.0mA
VOH	OUTPUT HIGH VOLTAGE	2.4	-	-	V	IOH=4.0mA
ICC	SUPPLY CURRENT	-	35	-	mA	VCC=5V

9 Physical Dimensions



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A_1	0.05	0.10	0.15	0.002	0.004	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.090		0.200	0.004		0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	13.90	14.00	14.10	0.547	0.551	0.555
e		0.50			0.020	
Hd	15.90	16.00	16.10	0.626	0.630	0.634
He	15.90	16.00	16.10	0.626	0.630	0.634
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1		1.00			0.039	
Y			0.08			0.003
θ	0		7	0		7

Notice

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