

TC6216M

16 Port 10/100 Unmanaged QoS Ethernet Switch



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16 Port 10/100 Unmanaged QoS Ethernet Switch

1 Features

- Stand Alone Switch On A Chip
- 16 Ethernet 10/100 ports with RMII Interface
- Port 16 is an RMII / MII port
- **Embedded 512Kbytes SSRAM packet buffer**
- **16K MAC address table**
- Multiple TC6216M can produce larger switches by trunking
- 10/100 selectable for each port
- Full / Half Duplex for each port
- Highly integrated switching logic, including the MAC functions on a single ASIC
- Flow-control for Full and Half Duplex
- **Three QoS levels checked via IP Header and 802.1Q VLAN Tag and/or selected per port basis**
- Maximum throughput
- Broadcast throttling
- Serial EEPROM Interface
- MDIO master for PHY configuration / polling
- 3.3V/1.8V dual voltage power
- **0.6 Watt power consumption**
- **0.18 micron technology**
- Packaged in PQFP 208

2 Description

TC6216M is a stand-alone 16 ports 10/100 unmanaged switch controller designed for low cost high performance solutions. In addition to the basic functions of unmanaged switches it provides features usually associated with managed switches, at very high performance levels. TC6216M offers full wire-speed switching on all 16 ports, self-learning of up to 16K MAC addresses, highly optimized flow control for full and half duplex, evolved traffic priority services, flexible trunking capabilities.

A store-and-forward switching method using a non-blocking architecture is implemented within TC6216M to improve the availability and bandwidth. The chip embeds a 512 Kbytes SSRAM packet buffer so the only external components required are the physical layer transceivers. Normal, high and very high priority queues are implemented for each transmission port.

The chip contains IEEE 802.3 MAC functions for 16 ports supporting both 10 Mbit/s and 100 Mbit/s data rates. All ports are full and half duplex capable. Each port has its dedicated receive and transmit FIFO's with necessary logic to implement flow-control for both duplex modes. TC6216M utilizes PAUSE frames as defined in IEEE 802.3x for full duplex flow control, and executes backpressure for half duplex mode. No packet will be lost when flow control is operational.

TC6216M provides leading edge QoS with three levels of priority. The priority can be checked via layer 2 (802.1Q VLAN Tagging) and/or layer 3 (IP Header TOS bits). Port based priority is also provided to enable user selectable traffic prioritization. Port based priority ensures transmission with precedence for all packets incoming from selected port(s). This feature allows effective video switching in multimedia applications and improved support for voice over packet applications.

The chip handles a 16K MAC address-lookup table with searching, self-learning, automatic aging, at a very high speed. Forwarding rules are implemented according with IEEE 802.1d specifications. TC6216M also provides filtering capability for bad packets, only good CRC and valid sized packets will be forwarded.

Larger switches can be produced using TC6216M's trunking capabilities. Two trunk groups of up to four ports each can be setup with TC6216M. Several load balancing schemes are provided through pins and EEPROM configuration.

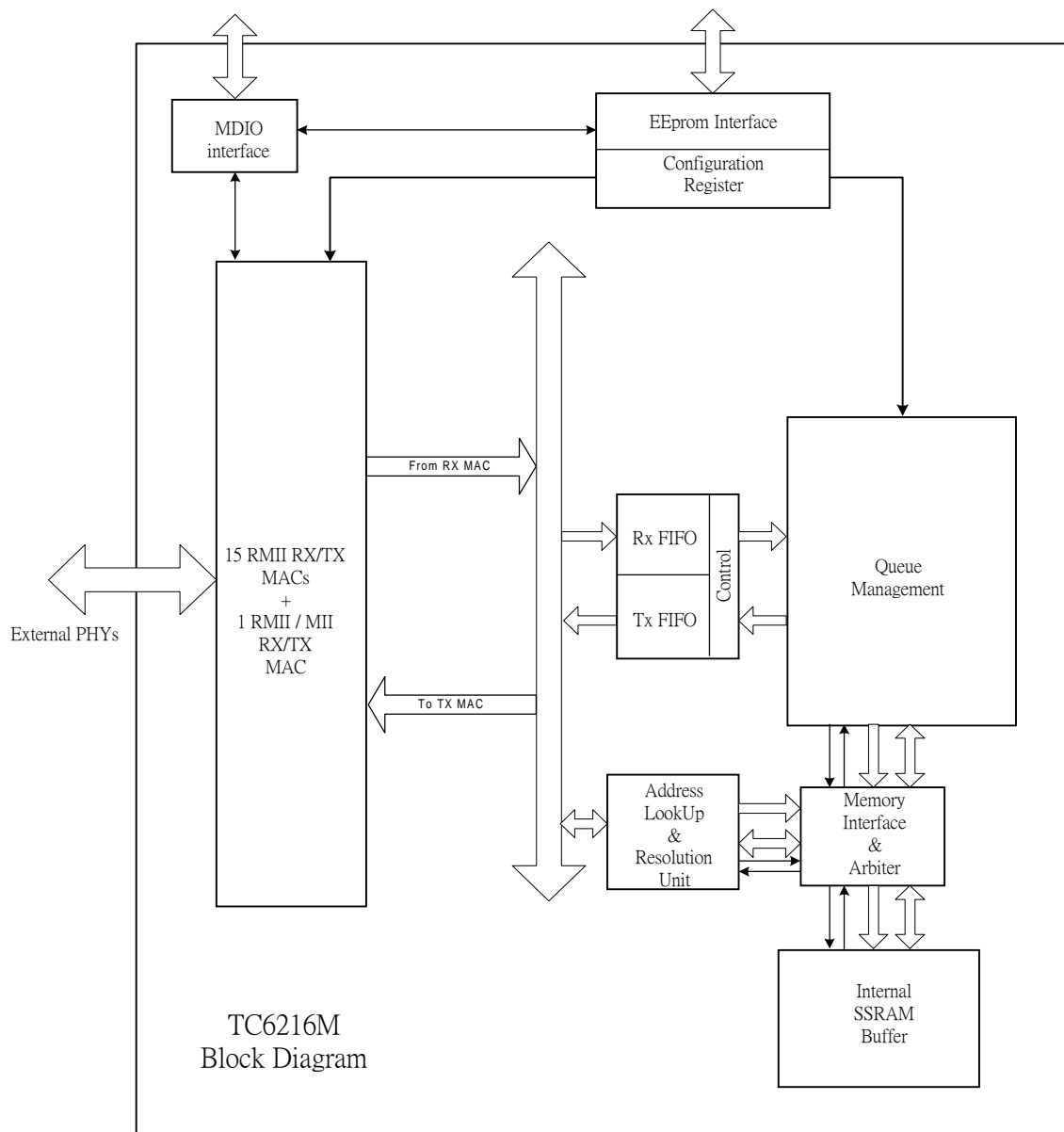
An external EEPROM device can be used to configure the TC6216M at power-up. Compared with pin configuration interface, the EEPROM extends the chip's configuration capability with new features and provides a jumperless configuration mode using a parallel print port interface for reprogramming. TC6216M can make effective use of most of its features without using the external EEPROM.

TC6216M uses an MDIO master entity for PHY autonegotiate mode polling and link status monitoring. Before extracting the autonegotiation result the chip advertises full duplex flow control ability on each port and restarts the autonegotiation.

Effective broadcast throttling based on both broadcast buffer memory utilization and broadcast bandwidth can be performed by TC6216M.

TC6216M achieves full performance at 50 MHz clock frequency. It is packaged in 208 PQFP.

3 Block Diagram



TC6216M
PQHP 208
Top View

[illegible]

5 Pin Listing (POFP 208)

Pin	Description	Pin label	Type
1	Power	Vss_3.3V	~
2	Reset	reset	I _{pu}
3	Configuration	TestMode	I _{pd}
4	Power	Vdd_3.3V	~
5	Configuration	TnkA0	I _{pd}
6	Configuration	TnkA1	I _{pd}
7	Power	Vdd_3.3V	~
8	Configuration	TnkB0	I _{pd}
9	Configuration	TnkB1	I _{pd}
10	Power	Vss_1.8V	~
11	Configuration	TnkMod0	I _{pd}
12	Power	Vss_3.3V	~
13	Configuration	TnkMod1	I _{pd}
14	Power	Vdd_1.8V	~
15	NC	NC	~
16	Configuration	PrtPri0	I _{pd}
17	Power	Vdd_3.3V	~
18	Configuration	PrtPri1	I _{pd}
19	Configuration	PrtPri2	I _{pd}
20	Power	Vss_1.8V	~
21	Configuration	PrtPri3	I _{pd}
22	Configuration	PrtPri4	I _{pd}
23	Power	Vss_3.3V	~
24	Configuration	PrtPri5	I _{pd}
25	Configuration	PrtPri6	I _{pd}
26	Power	Vdd_1.8V	~
27	Configuration	PrtPri7	I _{pd}
28	Configuration	PriLev0	I _{pd}
29	Power	Vdd_3.3V	~
30	Configuration	PriLev1	I _{pd}
31	Configuration	PriLev2	I _{pd}
32	Power	Vss_1.8V	~
33	Configuration	PriLev3	I _{pd}
34	Configuration	PriLev4	I _{pd}
35	Power	Vdd_1.8V	~
36	Configuration	PriLev5	I _{pd}
37	Configuration	PriLev6	I _{pd}
38	Configuration	PriLev7	I _{pd}
39	Power	Vss_3.3V	~
40	Power	Vdd_3.3V	~
41	Configuration	EnIPPr	I _{pd}

Pin	Description	Pin label	Type
105	RMII	Crs_Dv5	I
106	RMII	RxDat50	I
107	RMII	RxDat51	I
108	Power	Vss_3.3V	~
109	RMII	TxE6	O
110	RMII	TxDat60	O
111	RMII	TxDat61	O
112	Power	Vdd_1.8V	~
113	RMII	Crs_Dv6	I
114	RMII	RxDat60	I
115	RMII	RxDat61	I
116	Power	Vss_1.8V	~
117	RMII	TxE7	O
118	RMII	TxDat70	O
119	RMII	TxDat71	O
120	Power	Vdd_1.8V	~
121	RMII	Crs_Dv7	I
122	RMII	RxDat70	I
123	RMII	RxDat71	I
124	Power	Vss_3.3V	~
125	RMII	TxE8	O
126	RMII	TxDat80	O
127	RMII	TxDat81	O
128	Power	Vdd_3.3V	~
129	RMII	Crs_Dv8	I
130	RMII	RxDat80	I
131	RMII	RxDat81	I
132	Power	Vss_3.3V	~
133	RMII	TxE9	O
134	RMII	TxDat90	O
135	RMII	TxDat91	O
136	Power	Vdd_3.3V	~
137	RMII	Crs_Dv9	I
138	RMII	RxDat90	I
139	RMII	RxDat91	I
140	Power	Vss_3.3V	~
141	RMII	TxE10	O
142	RMII	TxDat100	O
143	RMII	TxDat101	O
144	Power	Vdd_1.8V	~
145	RMII	Crs_Dv10	I

Pin	Description	Pin label	Type
42	Configuration	EnVLPr	I _{pd}
43	Power	Vss_1.8V	~
44	Configuration	FCBcstEn	I _{pu}
45	Configuration	BcstAll	I _{pu}
46	Configuration	BcstTr	I _{pd}
47	Configuration	RejMCT	I _{pu}
48	Power	Vdd_1.8V	~
49	Configuration	FcOpt	I _{pu}
50	Power	Vdd_3.3V	~
51	Configuration	DisBPBk	I _{pd}
52	Power	Vss_3.3V	~
53	Power	Vss_1.8V	~
54	Configuration	DisBPr	I _{pd}
55	Configuration	FullBP	I _{pd}
56	Power	Vdd_1.8V	~
57	LED	PowLED	O _L
58	LED	OvBcLED	O _L
59	LED	OvUnLED	O _L
60	Power	Vss_3.3V	~
61	RMII	TxE0	O
62	RMII	TxDat00	O
63	RMII	TxDat01	O
64	Power	Vdd_3.3V	~
65	RMII	Crs_Dv0	I
66	RMII	RxDat00	I
67	RMII	RxDat01	I
68	Power	Vss_3.3V	~
69	RMII	TxE1	O
70	RMII	TxDat10	O
71	RMII	TxDat11	O
72	Power	Vdd_1.8V	~
73	RMII	Crs_Dv1	I
74	RMII	RxDat10	I
75	RMII	RxDat11	I
76	Power	Vss_1.8V	~
77	RMII	TxE2	O
78	RMII	TxDat20	O
79	RMII	TxDat21	O
80	Power	Vdd_1.8V	~
81	RMII	Crs_Dv2	I
82	RMII	RxDat20	I
83	RMII	RxDat21	I
84	Power	Vss_1.8V	~

Pin	Description	Pin label	Type
146	RMII	RxDat100	I
147	RMII	RxDat101	I
148	Power	Vss_1.8V	~
149	CLK	refck	I
150	Power	Vdd_3.3V	~
151	CLK	clk	I
152	CLK	CLK75M	O
153	MDIO	MDIO	I/O _{pu}
154	MDIO	MDClk	O
155	Power	Vdd_1.8V	~
156	RMII	TxE11	O
157	RMII	TxDat110	O
158	RMII	TxDat111	O
159	Power	Vss_1.8V	~
160	RMII	Crs_Dv11	I
161	RMII	RxDat110	I
162	RMII	RxDat111	I
163	Power	Vdd_1.8V	~
164	RMII	TxE12	O
165	RMII	TxDat120	O
166	RMII	TxDat121	O
167	Power	Vss_1.8V	~
168	RMII	Crs_Dv12	I
169	RMII	RxDat120	I
170	RMII	RxDat121	I
171	Power	Vdd_3.3V	~
172	RMII	TxE13	O
173	RMII	TxDat130	O
174	RMII	TxDat131	O
175	Power	Vss_3.3V	~
176	RMII	Crs_Dv13	I
177	RMII	RxDat130	I
178	RMII	RxDat131	I
179	Power	Vdd_1.8V	~
180	RMII	TxE14	O
181	RMII	TxDat140	O
182	RMII	TxDat141	O
183	Power	Vss_1.8V	~
184	RMII	Crs_Dv14	I
185	RMII	RxDat140	I
186	RMII	RxDat141	I
187	Power	Vdd_3.3V	~
188	(R)MII	TxE15	O

Pin	Description	Pin label	Type
85	RMII	TxE3	O
86	RMII	TxDat30	O
87	RMII	TxDat31	O
88	Power	Vdd_1.8V	~
89	RMII	Crs_Dv3	I
90	RMII	RxDat30	I
91	RMII	RxDat31	I
92	Power	Vss_1.8V	~
93	RMII	TxE4	O
94	RMII	TxDat40	O
95	RMII	TxDat41	O
96	Power	Vdd_3.3V	~
97	RMII	Crs_Dv4	I
98	RMII	RxDat40	I
99	RMII	RxDat41	I
100	Power	Vss_3.3V	~
101	RMII	TxE5	O
102	RMII	TxDat50	O
103	RMII	TxDat51	O
104	Power	Vdd_3.3V	~

Pin	Description	Pin label	Type
189	(R)MII	TxDat150	O
190	(R)MII	TxDat151	O
191	(R)MII	TxDat152	O
192	(R)MII	TxDat153	O
193	Power	Vss_3.3V	~
194	CLK	TxCk	I
195	Power	Vdd_1.8V	~
196	(R)MII	Col15	I
197	(R)MII	Crs15	I
198	(R)MII	Crs_Dv15	I
199	(R)MII	RxDat150	I
200	(R)MII	RxDat151	I
201	(R)MII	RxDat152	I
202	(R)MII	RxDat153	I
203	Power	Vss_1.8V	~
204	CLK	RxCk	I
205	Power	Vss_3.3V	~
206	Configuration	MIIMode	I _{pd}
207	EEPROM	SCL	O
208	EEPROM	SDA	I/O _{pu}

I ⇒ digital input
 I_{pd} ⇒ digital input internally pulled down
 I_{pu} ⇒ digital input internally pulled up
 O ⇒ digital output
 O_L ⇒ digital output active low
 I/O_{pu} ⇒ digital bidirectional internally pulled up

6 Pin Description

Interface	Signal	I/O	Signal Description
Control/Clock	reset	I	General reset.
	Clk	I	System clock. The switch performance is full wire speed at 50Mhz system clock frequency.
	Clk75M	O	Output clock from internal PLL. For 75MHz system clock frequency tie this to system clock pin.
Test	TestMode	I	If set to '1' the chip will be in Memory Test Mode.
Trunking	TnkA(0:1) TnkB(0:1)	I	Trunking configuration. • First trunk channel TnkA1 TnkA0 0 0 No port is configured as trunk port 0 1 Ports 0 and 1 are configured as trunk ports 1 0 Ports 0,1,2 are configured as trunk ports 1 1 Ports 0,1,2 and 3 are configured as trunk ports • Second trunk channel TnkB1 TnkB0 0 0 No port is configured as trunk port 0 1 Ports 15 and 14 are configured as trunk ports 1 0 Ports 15, 14, 13 are configured as trunk ports

Interface	Signal	I/O	Signal Description
			1 1 Ports 15, 14, 13 and 12 are configured as trunk ports
	TnkMod(0:1)	I	Trunk Balance Mode Select TnkMod1 TnkMod0 0 0 Only source port is used to select the transmission port inside the trunk. 0 1 Transmission port is selected using SA. 1 0 Transmission port is selected using SA and DA. 1 1 Not used
QoS configuration	PrtPri (0:7)	I	Indicates which ports, if any, are in Priority Mode; when selected the corresponding port will have high or very high priority depending of the state of PriLev pin. PrtPri(0:7) are used to set the priorities for ports 4 to 11. TC6216M Port (4 to 11) ⇔ PrtPri (0:7)
	PriLev (0:7)	I	Selects the high or very high priority for priority ports. '1' – Very high priority '0' – High priority PriLev (0:7) refers to TC6216M ports 4 to 11.
	EnIPPr	I	Enables QoS resolution to consider TOS Precedence bits from IP Header. '1' – IP priority will be considered '0' – IP priority will be neglected
	EnVLPr	I	Enables QoS resolution to consider user_priority bits (TCI field) from 802.1Q VLAN Tag Header. '1' – VLAN priority will be considered '0' – VLAN priority will be neglected
Broadcast configuration	FcBcstEn	I	Enables Flow Control for Broadcast operation. '1' – Enable '0' – Disable
	BcstAll	I	Broadcast All Mode Select '1' – forward broadcast packets to all the ports '0' – forward broadcast packets to active ports only
	BcstTr	I	Enables broadcast throttling. '1' – Enable '0' – Disable
MII Mode Selection	MIIMode	I	Select MII or RMII interface for port 15 '0' – RMII '1' – MII
MAC Configuration	RejMCT	I	All Mac Control Type Packets will be rejected if this pin is asserted, otherwise they will be forwarded.
Flow Control	FCOpt	I	Flow Control resolution option: '1' – the A-NEG result is considered '0' – doesn't matter the A-NEG result
	DisBPr	I	Enable / Disable Flow Control for Half Duplex Mode '1' – Disable '0' – Enable
	FullBP	I	When this is set to '0' then the backpressure process will be stopped after reaching 30 consecutive collisions. The default value (30) can be changed by EEPROM settings. Otherwise the backpressure can be executed for up to 2048 (default pause value) slot times if the flow control condition persists.

Interface	Signal	I/O	Signal Description
	DisBPBk	I	Disables completely any backoff when executing backpressure: '1' – no backoff when backpressure '0' – aggressive backoff for backpressure
Power and BIST	PowLED	O	Signals good operation state. In case of BIST error the code of the error is signaled on this pin.
Overflow signaling	OvBcLED	O	Signals overflow condition for broadcast operation.
	OvUnLED	O	Signals overflow condition for unicast operation.
EEPROM Interface	SDA	I/O	Serial Data.
	SCL	O	Serial Clock.
MDIO Interface	MDIO	I/O	MDIO BUS.
	MDClk	O	MDIO clock.
RMII Interface Port0	TxDat0(0:1)	O	RMII Tx Data.
	TxEn0	O	RMII Tx Enable.
	Crs_Dv0	I	RMII Carrier Sense / Receive Data Valid.
	RxDat0(0:1)	I	RMII Rx Data.
RMII Interface Port1	TxDat1(0:1)	O	RMII Tx Data
	TxEn1	O	RMII Tx Enable.
	Crs_Dv1	I	RMII Carrier Sense / Receive Data Valid
	RxDat1(0:1)	I	RMII Rx Data.
RMII Interface Port2	TxDat2(0:1)	O	RMII Tx Data
	TxEn2	O	RMII Tx Enable
	Crs_Dv2	I	RMII Carrier Sense / Receive Data Valid
	RxDat2(0:1)	I	RMII Rx Data
RMII Interface Port3	TxDat3(0:1)	O	RMII Tx Data
	TxEn3	O	RMII Tx Enable
	Crs_Dv3	I	RMII Carrier Sense / Receive Data Valid
	RxDat3(0:1)	I	RMII Rx Data
RMII Interface Port4	TxDat4(0:1)	O	RMII Tx Data
	TxEn4	O	RMII Tx Enable
	Crs_Dv4	I	RMII Carrier Sense / Receive Data Valid
	RxDat4(0:1)	I	RMII Rx Data
RMII Interface Port5	TxDat5(0:1)	O	RMII Tx Data
	TxEn5	O	RMII Tx Enable
	Crs_Dv5	I	RMII Carrier Sense / Receive Data Valid
	RxDat5(0:1)	I	RMII Rx Data
RMII Interface Port6	TxDat6(0:1)	O	RMII Tx Data
	TxEn6	O	RMII Tx Enable
	Crs_Dv6	I	RMII Carrier Sense / Receive Data Valid
	RxDat6(0:1)	I	RMII Rx Data
RMII Interface Port7	TxDat7(0:1)	O	RMII Tx Data
	TxEn7	O	RMII Tx Enable
	Crs_Dv7	I	RMII Carrier Sense / Receive Data Valid
	RxDat7(0:1)	I	RMII Rx Data

Interface	Signal	I/O	Signal Description
RMII Interface Port8	TxDat8(0:1)	O	RMII Tx Data
	TxEn8	O	RMII Tx Enable
	Crs_Dv8	I	RMII Carrier Sense / Receive Data Valid
	RxDat8(0:1)	I	RMII Rx Data
RMII Interface Port9	TxDat9(0:1)	O	RMII Tx Data
	TxEn9	O	RMII Tx Enable
	Crs_Dv9	I	RMII Carrier Sense / Receive Data Valid
	RxDat9(0:1)	I	RMII Rx Data
RMII Interface Port10	TxDat10(0:1)	O	RMII Tx Data
	TxEn10	O	RMII Tx Enable
	Crs_Dv10	I	RMII Carrier Sense / Receive Data Valid
	RxDat10(0:1)	I	RMII Rx Data
RMII Interface Port11	TxDat11(0:1)	O	RMII Tx Data
	TxEn11	O	RMII Tx Enable
	Crs_Dv11	I	RMII Carrier Sense / Receive Data Valid
	RxDat11(0:1)	I	RMII Rx Data
RMII Interface Port12	TxDat12(0:1)	O	RMII Tx Data
	TxEn12	O	RMII Tx Enable
	Crs_Dv12	I	RMII Carrier Sense / Receive Data Valid
	RxDat12(0:1)	I	RMII Rx Data
RMII Interface Port13	TxDat13(0:1)	O	RMII Tx Data
	TxEn13	O	RMII Tx Enable
	Crs_Dv13	I	RMII Carrier Sense / Receive Data Valid
	RxDat13(0:1)	I	RMII Rx Data
RMII Interface Port14	TxDat14(0:1)	O	RMII Tx Data
	TxEn14	O	RMII Tx Enable
	Crs_Dv14	I	RMII Carrier Sense / Receive Data Valid
	RxDat14(0:1)	I	RMII Rx Data
(R)MII Interface Port15	TxDat15(0:3)	O	RMII Tx Data (0:1) / MII Tx Data (0:3)
	RxDat15(0:3)	I	RMII Rx Data (0:1) / MII Rx Data (0:3)
	TxEn15	O	RMII / MII Tx Enable
	Crs_Dv15	I	RMII Carrier Sense / Receive Data Valid
	Col15	I	MI1 Collision.
	TxC1k15	I	MI1 Tx Clock.
	RxC1k15	I	MI1 Rx Clock.
	CRS15	I	MI1 Carrier Sense.
RMII Reference Clock	refck	I	RMII Reference Clock for Port 0-15

7 **Ethernet Media Access Controller**

The Ethernet Media Access Controller (MAC) contains IEEE 802.3 MAC functions for 16 ports. It is able to operate in 10/100 speed modes, full and half duplex. Each port has its dedicated receive and transmit FIFO's with necessary logic to implement flow-control for both duplex modes. The MAC functions are optimized and tailored for high speed and flexible interfacing.

7.1 **Receive MAC**

When a frame is received from the Ethernet media through the RMII, the data is stored in a receive FIFO. The FIFO acts as a temporary buffer between the Receive MAC section and switch core interface.

The Receive MAC layer decomposes Ethernet packets acquired from the PHY layer via RMII, by stripping off the preamble sequence and SFD. The Receive MAC then sends packets to the receive FIFO along with packet validity information.

The MAC determines the validity of each received packet by checking the CRC and packet length. The bad packets will be dropped either by the MAC or by the queue manager. Oversized packets are truncated to 1536 bytes and marked to be erroneous. Undersized packets are removed from the receive FIFO without being reported at the switch interface. The FIFO space held by undersized packets is automatically recovered by removing the packet.

The Receive MAC is also able to reject Mac Control Type frames (type 88-08). To activate this filtering function it must be selected using **RejMCT** pin or the equivalent EEPROM bit.

When the TC6216M receives a MAC control frame and determines that the opcode is a PAUSE command (flow control frame) and the frame's CRC is OK, the chip will load its internal pause counter with the 'time value' variable extracted from the incoming flow control packet. If the pause counter is not 'zero' the Receive MAC will XOFF the Transmit MAC. The pause counter will decrement after each slot time and will XON the Transmit MAC when the 'zero' value is reached.

If a frame transmission is in progress when the PAUSE frame is received, the transmission is allowed to complete but it will be stopped for the next packets until an XON command is generated by the Receive MAC. The pause time will begin at the end of current transmission or immediately (if no transmission is in course at the moment of receiving the PAUSE frame). If a pause command is received while the transmitter is already in pause, the new pause time indicated by the new Flow Control frame will be loaded into the pause register.

When the receive FIFO is full and additional data are still incoming from the MAC, then the overrun condition occurs and the frame is dropped. If the system clock frequency is not lower than the recommended value this condition will not occur.

7.2 **Transmit MAC**

The Transmit MAC section assembles the MAC frames stored in the transmit FIFO and controls their transmission onto the media via external PHY entities. It appends the standard preamble and start of frame delimiter to the transmitted packets. The Transmit MAC also controls the InterFrameGap time during transmission, maintaining for default the standard minimum InterFrameGap of 96 bit time. This value can be changed by EEPROM setting.

For half duplex mode the Transmit MAC meets CSMA/CD IEEE 802.3 requirements. The FIFO logic manages frame retransmission for early collision conditions or discards the frame if late collision occurs. It also follows the truncated binary exponential backoff algorithm, collision and jamming procedures.

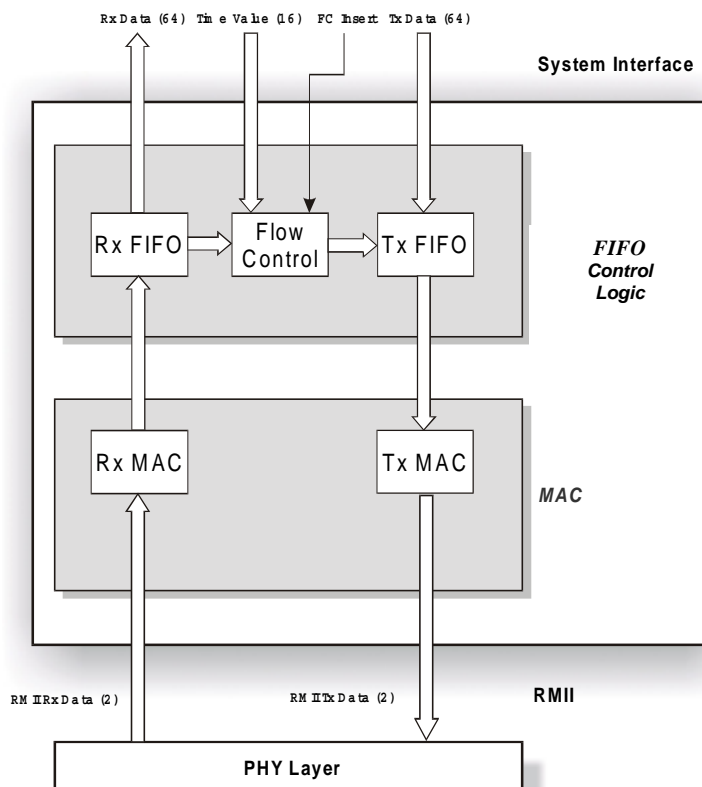
The transmit FIFO buffers the packets available for transmission in the main memory queues. If the transmit FIFO gets empty before the packet currently in transmission reaches its end, an underrun condition is generated. When the switch core transfers the rest of the packet into the FIFO the Transmit MAC safely discards it without affecting the next packet. Underrun conditions will not occur if the system is operated at the recommended clock frequency or higher.

For full duplex mode the TC6216M implements the flow-control algorithm according with the IEEE 802.3x standard. The chip uses the XON/XOFF method adjusting the Pause Value field inside the MAC Pause Frame according to traffic conditions. The full duplex flow control can be enabled/disabled depending on autonegotiation result, pin configuration and/or EEPROM settings.

The TC6216M executes backpressure algorithm as half duplex flow control mode if not disabled by **DisBPr** pin or EEPROM (**ConfigRegPx[1]**). The backpressure algorithm is based on carrier sense forced collisions and an aggressive backoff algorithm. The forced consecutive collisions generated for flow control purposes can be

limited to a maximum of 30 collisions if this option is selected. The default number of consecutive collisions can be changed by EEPROM settings. This feature can be used to avoid HUB partitioning.

MAC Block Diagram



8 Traffic Priority

TC6216M supports advanced traffic priority features (QoS). It provides three levels of priority: normal, high and very high priority. Each class of priority has its dedicated queue for each transmission port. Packets in priority mode (high or very high priority) will arrive sooner at the destination MAC address. When all (3) priority queues for the same port are not empty the transmission bandwidth is used around 8% for the low priority queue, 30% for high priority and 62% for very high priority queue. The bandwidth distribution when one of the queues is empty can be observed in the table below:

Priority Queues IF Empty	Transmission Bandwidth Utilization Factor		
	Normal (Low) Priority	High Priority	Very High Priority
Normal	X	33%	66%
High	11%	X	89%
Very High	20%	80%	X
None	8%	30%	62%

These priority rules apply for all ports and are independent of the port's speed mode or duplex mode. A special packet dropping mechanism is also implemented to offer more protection against overflow conditions for priority packets. If the packet memory load is exceeding an overflow threshold then all normal priority packets will be dropped on source port basis in order to save space for the priority packets. This will minimize the probability of packet loss in priority flows for senders that are not flow-control capable.

The QoS mechanism supports multiple prioritization sources. Packet priority can be checked via 802.1Q VLAN Tag Header TCI bits (layer 2) and/or IP Header TOS bits (layer 3). If the value of TCI/TOS bits is “0”, this packet will be treated as normal priority, if “1” then it will be high priority, if more than “1” then it will be very high priority. Port based prioritization is also available. Using port based priority the user can assign different priorities for each port. If VLAN and IP priority are disabled or not labeled, all packets received on the same port will be forwarded with the corresponding assigned port base priority. When more than one prioritization methods are active at the same time (VLAN, IP and/or port based) the priority resolution consists of maximizing the priority class.

The QoS can be configured using both pin configuration interface and/or EEPROM settings. The VLAN prioritization can be enabled by **EnVLPr** pin or by **PriorityReg[0]** EEPROM bit, while **EnIPPr** pin or **PriorityReg[1]** EEPROM bit can be used to enable the IP priority. Port based prioritization is available using **PrtPri(x)** and **PriLev(x)** pins for port 4 to 11, or equivalent EEPROM bits **ConfigRegPx[3]** and **ConfigRegPx[2]** for each ports. Setting **PrtPri(x)** pin to ‘1’ will configure the corresponding port in Priority Mode. **PriLev(x)** pin selects between high (‘0’) and very high priority (‘1’).

9 Trunk Configuration

TC6216M can setup two port aggregation links, named ‘Trunk A’ respectively ‘Trunk B’, of up to 4 ports each. Using this feature multiple TC6216M can be cascaded or interconnected with other switches supporting the trunking feature.

The trunks can be independently configured according with tables below using pin configuration **TnkA0** , **TnkA1** respectively **TnkB0** , **TnkB1** or using EEPROM configuration (**TrunkCfgReg**).

TnkA1	TnkA0	Ports grouped within Trunk A
‘0’	‘0’	Trunk A disabled
‘0’	‘1’	Trunk A groups ports 0 and 1
‘1’	‘0’	Trunk A groups ports 0,1 and 2
‘1’	‘1’	Trunk A groups ports 0,1,2 and 3

TnkB1	TnkB0	Ports grouped within Trunk B
‘0’	‘0’	Trunk B disabled
‘0’	‘1’	Trunk B groups ports 14 and 15
‘1’	‘0’	Trunk B groups ports 13,14 and 15
‘1’	‘1’	Trunk B groups ports 12,13,14 and 15

The traffic on the ports of the same trunk will be automatically balanced. TC6216M can be selected from three balancing methods based on source port, SA and DA as shown in the table below. They are selectable from TnkMod(0-1) pins or from EEPROM TrunkCfgReg register:

TnkMod1	TnkMod0	Method Description
‘0’	‘0’	Method 1. based on source port.
‘0’	‘1’	Method 2. based on SA.
‘1’	‘0’	Method 3. based on SA and DA.
‘1’	‘1’	Not used

Different stations connected on the same port may not send traffic on the same trunk line. The packet order is guaranteed for method 1 and 2 for unicast and broadcast packets. The packet order is guaranteed for method 3 only for unicast packets.

The default mode for all trunking ports is 100Mbps full duplex. Trunk port modes can be changed using EEPROM settings although this is not recommended. Also it is recommended for trunk ports to be interconnected with 100Mbps full duplex capable ports only. If the user selects a trunk configuration it must

make sure that all ports are connected within the trunk, the port order is not mandatory. If one wire from a defined trunk is not connected, the trunk may not work properly.

10 Flow Control

TC6216M executes backpressure for half duplex and is IEEE 802.3x compliant for full duplex flow control operation. The chip uses XON/XOFF flow control method in full duplex mode.

For full duplex operation, if no EEPROM is used and FCOpt pin is asserted the autonegotiation flow control capability resolution is executed. This means that if bit 10 from the Link Partner Advertisement Register is not set then the transmission of flow control packets is disabled. If FCOpt is '0' then the entire flow control operation for full duplex is always executed. The flow control on the receive side is always operational disregarding the state of FCOpt pin. FCOpt pin represents a global setting for all 16 ports.

When the EEPROM is used, the FCOpt can be override by its equivalent bit FlowControlReg[0]. Supplementary a setting is offered per port basis DsFulDpxFC (ConfigRegPx[4]). Setting this bit to '1' will disable the flow control on that port no matter of autonegotiation result.

Without EEPROM

<i>FCOpt Pin</i>	<i>A-NEG (bit 10 from the PHY's Link Partner Register)</i>	<i>FC – Ability</i>
0	Don't care	Enabled
1	Disabled	Disabled
	Enabled	Enabled

With EEPROM

<i>FCOpt Bit (FlowControlReg)</i>	<i>DsFulDpxFc Bit (ConfigRegP x)</i>	<i>A-NEG (bit 10 from the PHY's Link Partner Register)</i>	<i>FC – Ability/Port</i>
0	1	Don't care	Disabled
	0		Enabled
1	1	Don't care	Disabled
	0	Disabled	Disabled
		Enabled	Enabled

The backpressure operation can also be disabled using DisBPr pin or per port base using EEPROM (ConfigRegPx[1]). In case a HUB with many workstations is connected to a port, the HUB may be partitioned in heavy traffic when the switch executes too much continuous backpressure. TC6216M can prevent this when FullBP pin is not asserted by discontinuing the backpressure process after a determined number of consecutive collisions is reached. This number can be specified using FlowControlReg, field BackPrLv.

11 Broadcast

In case of excessive broadcast the traffic can be throttled on source port basis. TC6216M implements an evolved throttling method based on both port bandwidth and broadcast memory utilization. This feature is enabled using **BcstTr** configuration pin or the EEPROM **BroadcastReg[2]** bit.

The memory used at any time by broadcast packets that are received from the same port can not exceed a preset amount. This is represented by a number of 256 byte packet buffers that can be set using BroadcastReg EEPROM register, field MemThrotReg. When no EEPROM is present the default value of 8 buffers is used. When more than this number of buffers are in use by broadcast packets, any other broadcast incoming from the respective port will be dropped.

The broadcast receive bandwidth per port can be reduced to a value between 1.5% to 22% of the port's maximum bandwidth. When the broadcast bandwidth exceeds the preset value some broadcast packets will be dropped. The throttling bandwidth can be adjusted using register BroadcastReg, field BndwThrotReg. It is obtained by multiplying the value in this field with 1.5%. The default value is 4 (6%).

Supplementary, but not depending of the broadcast throttling configuration, all broadcast packets will be dropped when the total amount of the memory used by broadcast packets exceeds a preset threshold. This situation will occur only when flow control for broadcast is disabled, otherwise no broadcast packet will be lost. The flow control for broadcast traffic can be enabled using FcBcstEn pin or EEPROM (BroadcastReg[1]). Even when broadcast flow control is disabled TC6216M is capable of taking continuous broadcast packets from one port and deliver them to all the other ports at maximum speed without losing packets.

When TC6216M is configured in BroadcastAll mode all broadcast packets will be sent to all ports. If BroadcastAll mode is disabled the broadcast packets will be sent only to ports that have the link status on. Link status is monitored by the PHY polling entity that also reads the port mode autonegotiation result.

12 Auto Negotiation

In Auto-Negotiation Mode (assumed by default when the EEPROM is not present) TC6216M is polling the PHY's RMII Management Registers using the MDIO line in order to extract the autonegotiated port mode information, full duplex flow control ability and the link status. The switch detects and follows any changes in less than 2 seconds.

After reset TC6216M advertises the full duplex flow control capability (writing '1' to bit 10 from PHY's Advertisement Register) and restarts the autonegotiation.

If the port mode (speed and duplex) is forced by EEPROM settings then this mode is also advertised before restarting the autonegotiation. In this case TC6216M will not advertise any other speed or duplex capability other than what is set by EEPROM. Port mode can be forced using ConfigRegPx bits 5 – 7.

13 EEPROM Interface

TC6216M can be configured using a serial EEPROM device type AT24C02A (2048 bits organized as 256 pages of 1 byte each). With this device the manufacturer can deliver a pre-configured system to their customers while the customers can reconfigure the system and retain their preferences.

The TC6216M is able to operate without EEPROM and can make effective use of its features using only the pin configuration interface. The EEPROM configuration provides additional features and it can override all pin interface settings offering a jumperless configuration mode. For this reason, equivalent EEPROM settings can be found for every configuration pin.

A validation bit is provided for each one of the EEPROM Configuration Registers. A dedicated Validation Register is reserved for this purpose and corresponding bits from this register must be set in order to enable the desired EEPROM configurations.

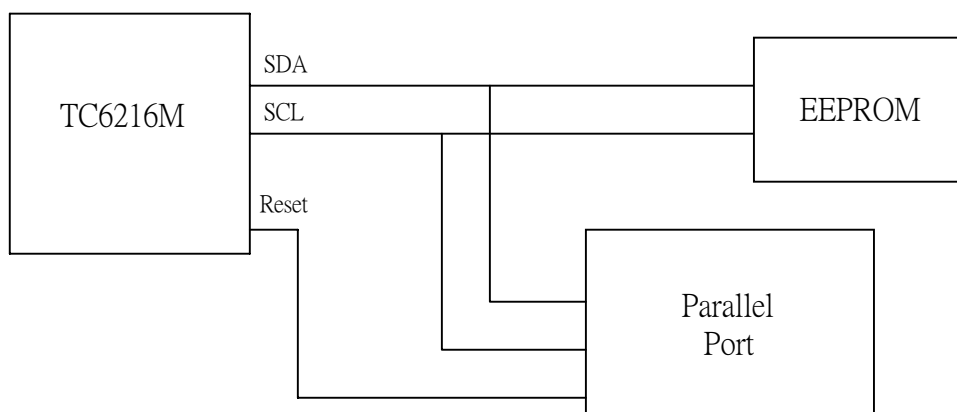
The EEPROM configuration information is accessed by the TC6216M after each reset procedure.

14 Programming the EEPROM for configuration

If the 'Reset' pin is hold low, the TC6216M's EEPROM interface will go into high impedance state. This feature enables easy programming of the EEPROM during installation or configuration.

The EEPROM can be programmed using an external parallel port. A dedicated signal from this port can be used to hold the RESET pin low. Once the TC6216M interface pins have got to the high impedance state the EEPROM can be programmed by the parallel port through the SDA and SCL pins.

To enable the AT24C02A device to be accessed by the TC6216M, its page address input pins must be hardwired to '0'.



15 [EEPROM Address Map](#)

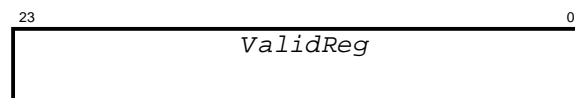
EEPROM				
Physical Address	Bits	Register Name	Validation Bit	DESCRIPTION
00	[7:0]	ValidReg [23 downto 16]	-	Validate Registers
01	[7:0]	ValidReg [15 downto 8]	-	Validate Registers
02	[7:0]	ValidReg [7 downto 0]	-	Validate Registers
03	[7:0]	ConfigRegP0 [7 downto 0]	ValidReg [0]	Port 0 Configuration Register
04	[7:0]	ConfigRegP1 [7 downto 0]	ValidReg [1]	Port 1 Configuration Register
05	[7:0]	ConfigRegP2 [7 downto 0]	ValidReg [2]	Port 2 Configuration Register
06	[7:0]	ConfigRegP3 [7 downto 0]	ValidReg [3]	Port 3 Configuration Register
07	[7:0]	ConfigRegP4 [7 downto 0]	ValidReg [4]	Port 4 Configuration Register
08	[7:0]	ConfigRegP5 [7 downto 0]	ValidReg [5]	Port 5 Configuration Register
09	[7:0]	ConfigRegP6 [7 downto 0]	ValidReg [6]	Port 6 Configuration Register
0A	[7:0]	ConfigRegP7 [7 downto 0]	ValidReg [7]	Port 7 Configuration Register
0B	[7:0]	ConfigRegP8 [7 downto 0]	ValidReg [8]	Port 8 Configuration Register
0C	[7:0]	ConfigRegP9 [7 downto 0]	ValidReg [9]	Port 9 Configuration Register
0D	[7:0]	ConfigRegP10 [7 downto 0]	ValidReg [10]	Port 10 Configuration Register
0E	[7:0]	ConfigRegP11 [7 downto 0]	ValidReg [11]	Port 11 Configuration Register
0F	[7:0]	ConfigRegP12 [7 downto 0]	ValidReg [12]	Port 12 Configuration Register
10	[7:0]	ConfigRegP13 [7 downto 0]	ValidReg [13]	Port 13 Configuration Register
11	[7:0]	ConfigRegP14 [7 downto 0]	ValidReg [14]	Port 14 Configuration Register
12	[7:0]	ConfigRegP15 [7 downto 0]	ValidReg [15]	Port 15 Configuration Register
13	[7:0]	FCPauseVal [15 downto 8]	ValidReg [16]	Flow Control Pause Value
14	[7:0]	FCPauseVal [7 downto 0]	ValidReg [16]	Flow Control Pause Value
15	[7:0]	MACCfgReg [7 downto 0]	ValidReg [17]	MAC Configuration Register
16	[7:0]	FlowControlReg [9 downto 8]	ValidReg [18]	Flow Control Register High
17	[7:0]	FlowControlReg [7 downto 0]	ValidReg [18]	Flow Control Register Low
18	[7:0]	TrunkCfgReg [7 downto 0]	ValidReg [19]	Trunk Configuration Register
19	[7:0]	BroadcastReg [11 downto 8]	ValidReg [20]	Broadcast Configuration Register High
1A	[7:0]	BroadcastReg [7 downto 0]	ValidReg [20]	Broadcast Configuration Register

EEPROM				
Physical Address	Bits	Register Name	Validation Bit	DESCRIPTION
				Low
1B	[7:0]	PriorityReg [15 downto 8]	ValidReg [21]	Reserved
1C	[7:0]	PriorityReg [7 downto 0]	ValidReg [21]	Priority Register Low

16 Register Description

Validation Register

- Address: 00h-02h



Bit(s)	Field	Description
23 – 22	Not Used	
21 – 0	ValidReg	EEPROM Configuration Validation Register

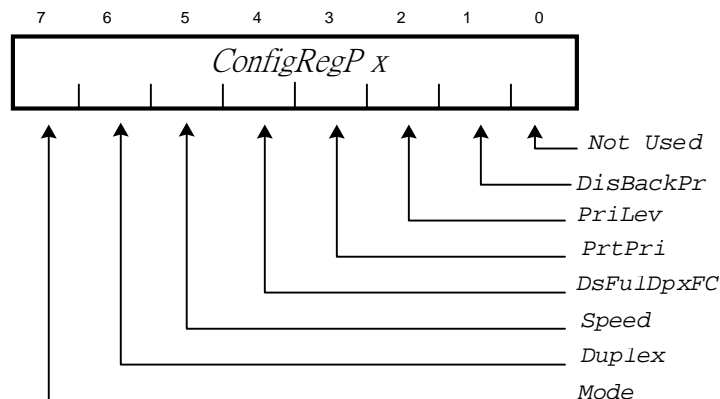
ValidReg – each bit from this field corresponds to an EEPROM Configuration Register. Configurations made using any of the EEPROM registers will be in force only if the register is validated by setting to '1' the corresponding bit in this register.

ValidReg [0]	– validation bit for ConfigRegP0 register
ValidReg [1]	– validation bit for ConfigRegP1 register
ValidReg [2]	– validation bit for ConfigRegP2 register
ValidReg [3]	– validation bit for ConfigRegP3 register
ValidReg [4]	– validation bit for ConfigRegP4 register
ValidReg [5]	– validation bit for ConfigRegP5 register
ValidReg [6]	– validation bit for ConfigRegP6 register
ValidReg [7]	– validation bit for ConfigRegP7 register
ValidReg [8]	– validation bit for ConfigRegP8 register
ValidReg [9]	– validation bit for ConfigRegP9 register
ValidReg [10]	– validation bit for ConfigRegP10 register
ValidReg [11]	– validation bit for ConfigRegP11 register
ValidReg [12]	– validation bit for ConfigRegP12 register
ValidReg [13]	– validation bit for ConfigRegP13 register
ValidReg [14]	– validation bit for ConfigRegP14 register
ValidReg [15]	– validation bit for ConfigRegP15 register
ValidReg [16]	– validation bit for FCPauseVal register
ValidReg [17]	– validation bit for MACCfgReg register
ValidReg [18]	– validation bit for FlowControlReg register
ValidReg [19]	– validation bit for TrunkCfgReg register
ValidReg [20]	– validation bit for BroadcastReg register
ValidReg [21]	– validation bit for PriorityReg register

Port x Configuration Register

- Address: 03h-12h

- Note: x = 0 to 15



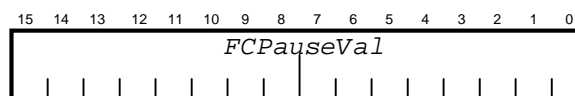
Bit(s)	Field	Description
7	Mode	Select source
6	Duplex	Full / Half Duplex Configuration
5	Speed	100 Mbps / 10Mbps Configuration
4	DsFulDpxFC	Disable Full Duplex Flow Control
3	PrtPri	Port Priority
2	PriLev	Priority Level
1	EnBackPr	Enable Backpressure
0	Not Used	

Mode – This bit selects the source of port mode configuration:

Mode	Duplex	Speed
0	Auto – Negotiation	Auto – Negotiation
1	EEPROM configuration	EEPROM configuration

- Duplex** – if 'Mode' configuration is '1' this bit will set the port's duplex mode. When high the port will be set in Full Duplex, when low it is Half Duplex.
- Speed** – if 'Mode' configuration is '1' this bit will set the port's speed mode. When high the port's data rate is 100Mbps, when low it is 10Mbps.
- DsFulDpxFC** – Setting this bit to 1 will disable transmit Full Duplex Flow Control for port X.
- Default '0'
- PortPriority** – When set forces port X in Priority Mode, otherwise the port will have normal priority.
- PriorityLevel** – If the corresponding port is in Priority Mode then the port will have a very high priority rate if this bit is asserted, otherwise only high priority rate.

Flow Control Pause Value
- Address: 14h-13h



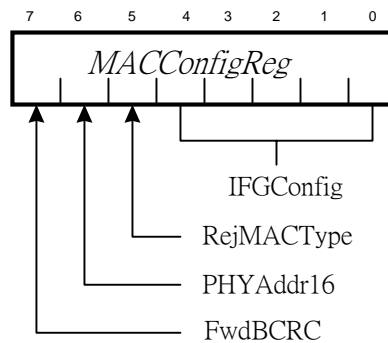
Bit(s)	Field	Description
15 – 0	FCPauseVal	Flow Control Pause Value

FCPauseVal

- 16-bits of data used by every port to determine backpressure duration after a flow control XOFF condition occurs. This value does not need to be adjusted by user.
- default '0000100000000000' = 2048

MAC Configuration Register

- Address: 15h



<u>Bit(s)</u>	<u>Field</u>	<u>Description</u>
7	<i>FwdBCRC</i>	Forward Bad CRC Packets
6	<i>RejMACType</i>	Reject MAC Control Type Frames
5	<i>PHYAddr16</i>	MDIO PHY Address 16 to 31
4 – 0	<i>IFGConfig</i>	Interframe Gap Configuration

FwdBCRC

- When set to '1' the switch will not filter bad CRC frames with valid sizes. This kind of frames will be forwarded as they were received (without correcting the CRC).

- Default '0'

PHYAddr16

- Setting this bit to '1' will program the PHY polling entity to use device address range 16 to 31 instead of range 0 to 15.

- Default '0'

RejMACType

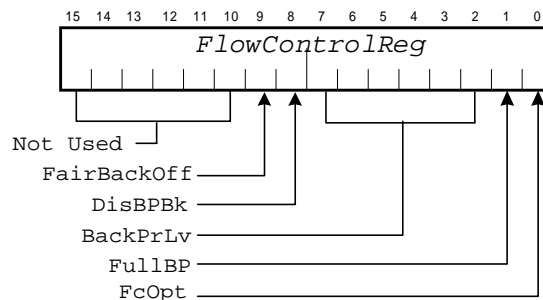
IFGConfig

- When asserted the switch filters all MAC Control Type frames (type 8808).
- These bits are used to set the minimum IFG. If default value is set then the IFG will have the standard minimum value of 960 ns, otherwise for one unit added the minimum IFG will be increased with 40 ns.

- Default '10101' = 21

Flow Control Register

- Address: 17h-16h

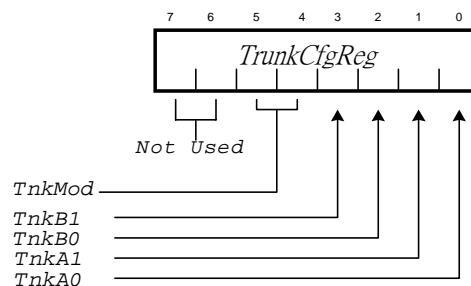


<u>Bit(s)</u>	<u>Field</u>	<u>Description</u>
---------------	--------------	--------------------

15 – 10	<i>Not Used</i>	
9	<i>FairBackOff</i>	Fair Back Off
8	<i>DisBPBk</i>	Disable BackOff in Backpressure
7 – 2	<i>BackPrLv</i>	Backpressure Level
1	<i>FullBP</i>	Full Backpressure
0	<i>FcOpt</i>	Optional Flow Control

- FairBkOff** – Selects the backoff mode. When '1' the standard backoff process is changed by resetting the collision counter after valid packet is received, instead of resetting after successful transmission. When '0' the standard backoff process is executed.
- Default '0'
- DisBPBk** – If set to '1' then no backoff will be executed when a half duplex port is in flow control mode. When '0', an aggressive backoff will be executed (recommended).
- FullBP** – When set to '1' the backpressure operation will be executed for a number of slot times determined by Flow Control Pause Value setting or until an XON command is received. When '0' the backpressure will be also stopped after reaching a number of consecutive collisions specified using **BackPrLv** field.
- BackPrLv** – Specifies the number of consecutive collisions that will determine TC6216M to cancel the backpressure (see the setting above).
- Default '011110' = 30
- FCOpt** – When is set the full duplex flow control resolution will be executed. This means that if the link partner does not advertise the flow control capability, the switch will not execute the flow control on transmission side. As result no flow control PAUSE frame will be generated, but transmission will be stopped if a valid flow control frame is received). If **FCOpt** is not set then the full duplex flow control will always be in effect unless deactivated by **ConfigRegPx[4] (DsFulDpxFC)**.

TrunkCfgReg
- Address: 18h



This register provides EEPROM equivalents for **TnkA[0-1]**, **TnkB[0-1]** and **TnkMod[0-1]** configuration pins. The trunks of TC6216M can be configured according with tables below:

TnkA1	TnkA0	Trunk 'A' Ports
0	0	Trunk A disabled
0	1	0 , 1
1	0	0, 1, 2
1	1	0, 1, 2, 3
TnkB1	TnkB0	Trunk 'B' Ports
0	0	Trunk B disabled
0	1	14, 15
1	0	13, 14, 15

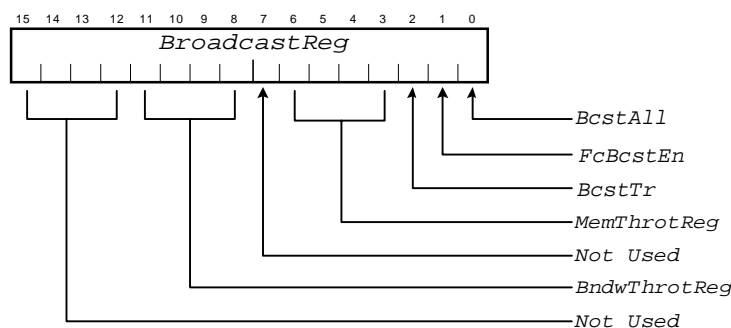
1	1	12, 13, 14, 15
---	---	----------------

TnkMod – Trunk Balance Mode Select:

TnkMod (1)	TnkMod (1)	Descriptions
0	0	Transmission port inside a trunk is selected using only the source port.
0	1	Transmission port is selected using DA.
1	0	Transmission port is selected using both SA and DA.
1	1	Not used

Broadcast Register

- Address: 1Ah-19h



Bit(s)	Field	Description
15-12	<i>Not Used</i>	
11-8	<i>BndwThrotReg</i>	Broadcast throttling bandwidth
7	<i>Not Used</i>	
6-3	<i>MemThrotReg</i>	Max broadcast memory load
2	<i>BcstTr</i>	Enable Broadcast Drop
1	<i>FCBcstEn</i>	Flow Control Broadcast Enable
0	<i>BcstAll</i>	Broadcast All

FCBcstEn – When set enables Flow Control operation for broadcast packets, otherwise broadcast will be dropped on queue overflow condition (throttling).

BcstAll – When set all the broadcast packets will be sent to all ports. When cleared all broadcast packets will be sent only to active ports. The port activity is detected by monitoring the transceiver's link status.

BcstTr – When is set the broadcast traffic will be throttled on the receive port basis.

MemThrotReg – When the **BcstTr** bit is set and all broadcast packets received on a single port and still waiting to be transmitted use a number of packet buffers that is greater than the number specified in this field, then any other broadcast incoming from this port will be dropped.

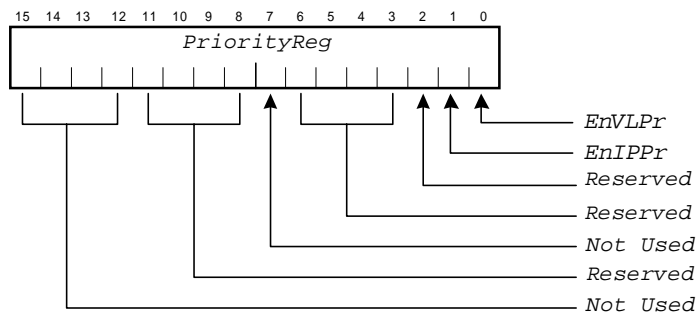
- Default "1000"

BndwThrotReg – The value contained in this field multiplied with 1.5% represents the percentage of the maximum bandwidth available for broadcast. If received broadcast on a port exceeds this bandwidth it will be throttled.

- Default "0100"

Priority Register

- Address: 1Ch-1Bh



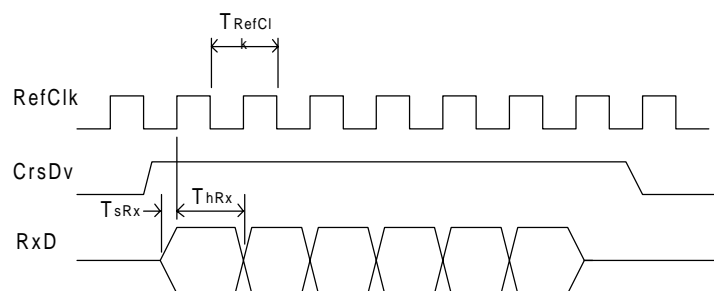
Bit(s)	Field	Description
15-12	Not Used	
11-8	Reserved	
7	Not Used	
6-3	Reserved	
2	Reserved	Should be '0'
1	EnIPPr	Enable IP Priority
0	EnVLPr	Enable VLAN Priority

- EnIPPr** – When asserted QoS resolution will consider TOS Precedence bits from IP Header.
- EnVLPr** – When asserted QoS resolution will consider user_priority bits (TCI field) from 802.1Q VLAN Tag Header.

17 [Timing Requirements](#)

• RMI Receive Timing Requirements

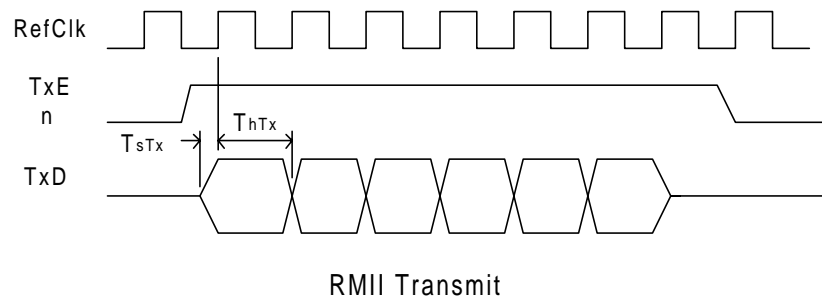
Symbol	Description	Min.	Typ.	MAX	Unit
T_{RefClk}	Reference clock period	-	20	-	ns
T_{sRx}	CrsDv, RxD to RefClk rising setup time	0	-	-	ns
T_{hRx}	CrsDv, RxD to RefClk rising hold time	4	-	-	ns



RMI Receive

• RMI Transmit Timing

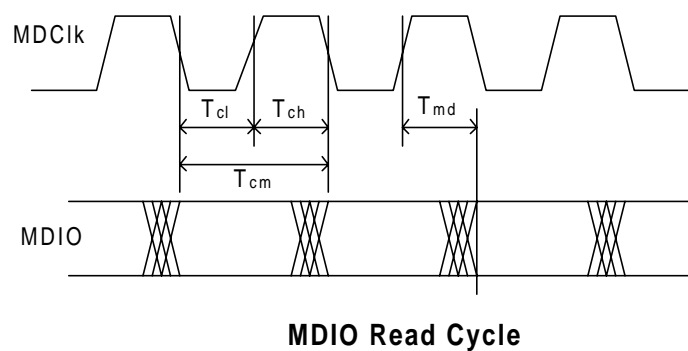
Symbol	Description	Min.	Typ.	MAX	Unit
T_{RefClk}	Reference clock period	-	20	-	ns
T_{sTx}	TxE _n , TxD to RefClk rising setup time	5	-	-	ns
T_{hTx}	TxE _n , TxD to RefClk rising hold time	4	-	-	ns

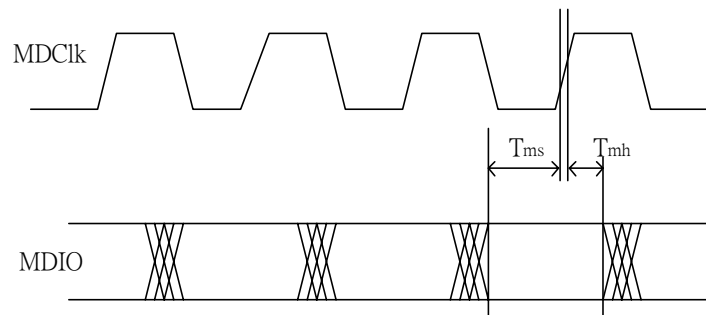


• **PHY Management (MDIO) Timing**

Symbol	Description	Min.	Typ.	MAX	Unit
T_{ch}	MDCK High Time	-	$15 * T_{\text{refck}}^{*1} = 300$	-	ns
T_{cl}	MDCK Low Time	-	$15 * T_{\text{refck}}^{*1} = 300$	-	ns
T_{cm}	MDCK period	-	$30 * T_{\text{refck}}^{*1} = 600$	-	ns
T_{md}	MDIO output delay		-	20	ns
T_{ms}	MDIO setup time	10			ns
T_{mh}	MDIO hold time	10			ns

Note: *1 T_{refck} is the period of the RMII reference clock.



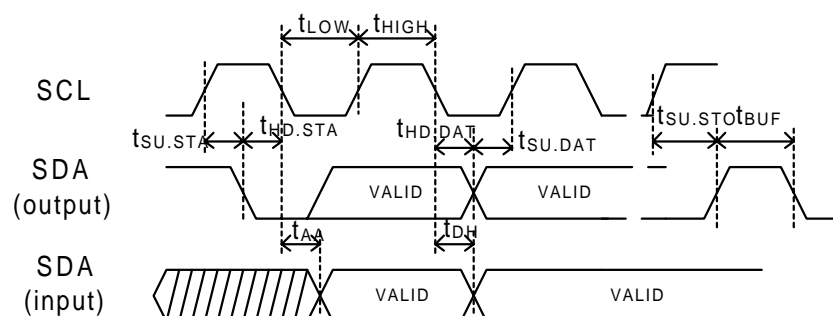


MDIO Write Cycle

• **EEPROM Timing**

Symbol	Description	Min.	Typ.	MAX	Unit
f_{SCL}	SCL frequency	-	$f_{refck}/1024=4.8.8^{*1}$	-	KHz
t_{LOW}	Clock Pulse Width Low	10	-	-	us
t_{HIGH}	Clock Pulse Width High	10	-	-	us
t_{BUF}	Time the bus must be free before starting a new transmission	5	-	-	us
$t_{HD.STA}$	Start Hold Time	5	-	-	us
$t_{SU.STA}$	Start Setup Time	5	-	-	us
$t_{HD.DAT}$	Data Hold Time	5	-	-	us
$t_{SU.DAT}$	Data Setup Time	5	-	-	us
$t_{SU.STO}$	Stop Set-up Time	5	-	-	us
t_{AA}	Clock Low to Data Out Valid	-	-	4.9	us
t_{DH}	Data Out Hold Time	0	-	-	us

Note: *1 f_{refck} is the frequency of the RMII reference clock.



EEPROM Interface Timing

18 Electrical Specifications

• ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the Recommended Operating Conditions section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	
Supply Voltage	I/O	V _{DDI/O}	V _{SSI/O} ^{*1} − 0.5	4.6	V	
	Core	V _{DDCore}	V _{SSCore} ^{*1} − 0.5	2.5	V	
Input Voltage		V _I	V _{SSI/O} ^{*1} − 0.5	6	V	
Output Voltage		V _O	V _{SSI/O} ^{*1} − 0.5	4.6	V	
Storage Temperature		T _{STG}	-65	+150	°C	
Operation Temperature		T _{OPT}	0	70	°C	
Latch-up Current		I _{LATCH}	>200			mA

Note: *1 $V_{SSI/O}, V_{SSCore} = 0V$

Note: The maximum ratings are the limit value that must never be exceeded even for short time.

• RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions represents recommended values that assure normal logic operation. As long as the device is used within the recommended operating conditions, the electrical characteristics (DC and AC characteristics) are guaranteed.

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	I/O	$V_{DDI/O}$	3.0	3.3	3.6	V
	Core	V_{DDCore}	1.62	1.8	1.98	V
Junction Temperature		T_j	0	25	125	°C
Low-level input voltage		V_{IL}	-0.5		1.0	V
High-level input voltage		V_{IH}	2.3		5.5	V

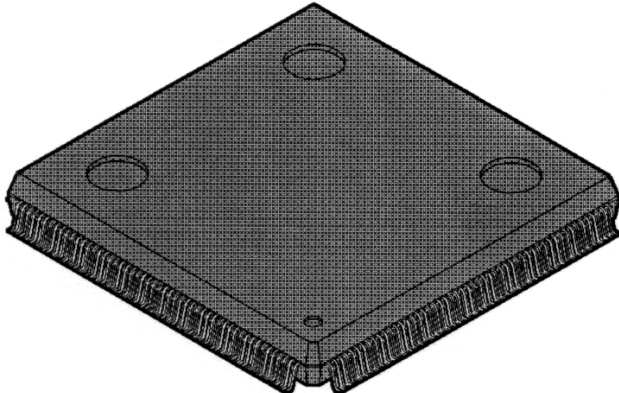
• DC CHARACTERISTICS

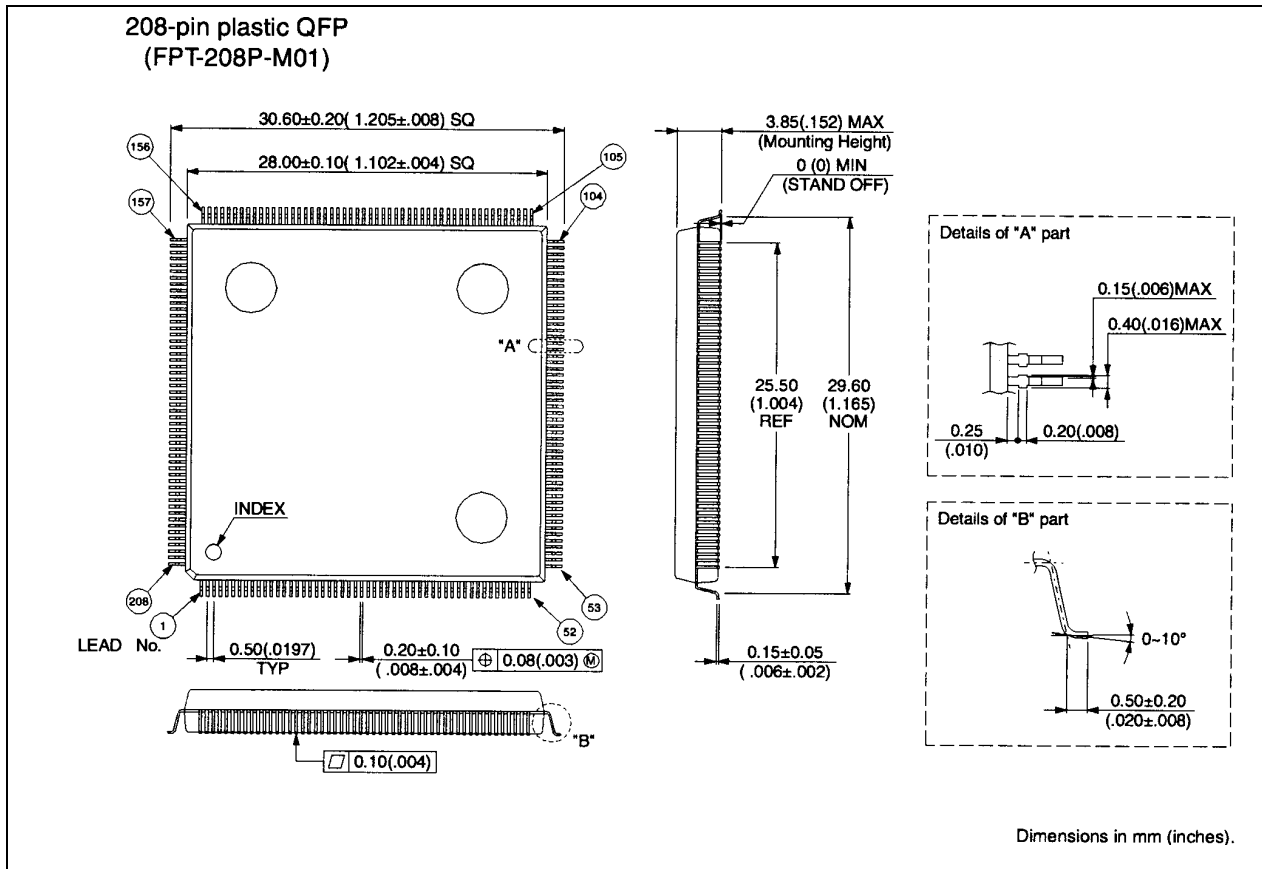
PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Output low voltage		V_{OL}			0.4	V
Output high voltage		V_{OH}	2.4			V
Low level output current	all outputs except for LEDs	I_{OL}	8.8	14.1	17.0	mA
	LED outputs		24.2	38.8	46.7	mA
High level output current	all outputs except for LEDs	I_{OH}	12.8	25.7	40.0	mA
	LED outputs		38.2	76.9	119.9	mA
Input Threshold point		V_T	1.46	1.60	1.76	V
RMII/MII Input (Schmitt trig.) Low to High threshold point ^{*1}		V_{T+}	1.66	1.75	1.79	V

RMII/MII Input (Schmitt trig.) High to Low treshold point ^{*1}	V_{T-}	0.93	1.01	1.06	V
Input leakage current (High and Low)	I_I		+/-10	+/-1000	nA
Tri-state output leakage current (High and Low)	I_{OZ}		+/-10	+/-1000	nA
Pull-up resistor	R_{PU}	56	77	122	K Ω
Pull-down resistor	R_{PD}	51	69	127	K Ω

Note: *1 This reffers to all inputs described as R(MII) in the Pin Listing section.

19 Mechanical Specifications

<p>208-pin plastic QFP</p> 	Lead pitch	0.50 mm
	Package width x Package length	28 x 28 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold



Notice

Information in this document is subject to change without notice. TMI reserves the rights to change its products at any time. Therefore, the customer is cautioned to confirm with TMI regarding the latest released version before placing orders.

TMI devices are NOT designed, intended, authorized, or warranted to be suitable for use in Life-Supporting applications.