

TC74HC40105AP, TC74HC40105AF

4 Bit×16 Word FIFO REGISTER

The TC74HC40105A is a high speed CMOS 4bit×16word first - in, first - out (FIFO) Strage Register fabricated with silicon gate C²MOS technology.

It achieves the high speed operation while maintaining the CMOS low power dissipation.

The device is capable of handling 16 four - bit words and it is possible to handle the input and output data at different shifting rates.

When the DATA - IN - READY (DIR) is high, data is written into the registers by a low to high transition of the SHIFT IN (SI) input. And when DATA - OUT - READY (DOR) is high, data is read out of the registers by a high to low transition of the SHIFT OUT (SO) input.

If the MASTER RESET (MR) is high, the DIR goes high and DOR goes low. The data in the internal registers are not changed but are declared invalid.

The TC74HC40105A can be cascaded to form longer registers or wider words.

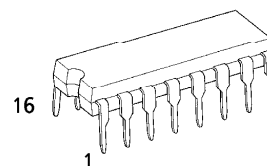
The DATA OUTPUTs (Q_n) are 3 - State Outputs. When OUTPUT ENABLE ($\overline{OE}$) is held high, the Q_n's are in high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

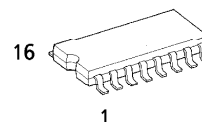
FEATURES:

- High Speed..... $f_{MAX} = 25\text{MHz}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Output Drive Capability10 LSTTL Loads For DIR,DOR
15 LSTTL Loads For Q₀~Q₃
- Symmetrical Output Impedance...

$$\begin{cases} |I_{OH}| = I_{OL} = 4\text{mA}(\text{min.}) \text{ For DIR,DOR} \\ |I_{OH}| = I_{OL} = 6\text{mA}(\text{min.}) \text{ For Q}_0 \sim \text{Q}_3 \end{cases}$$
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range.... $V_{CC} (\text{opr.}) = 2\text{V} \sim 6\text{V}$

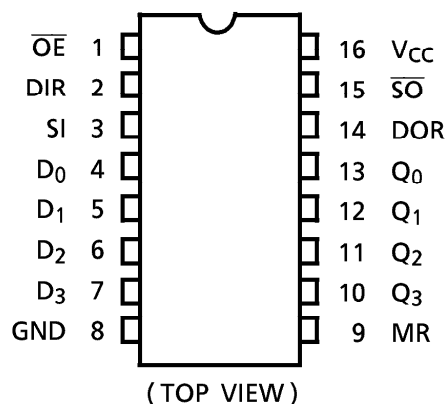


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

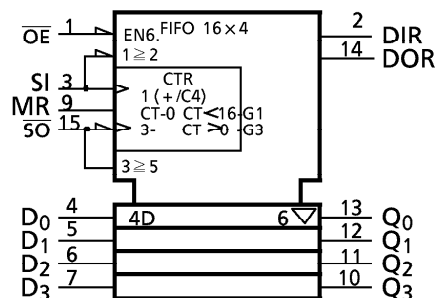


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL



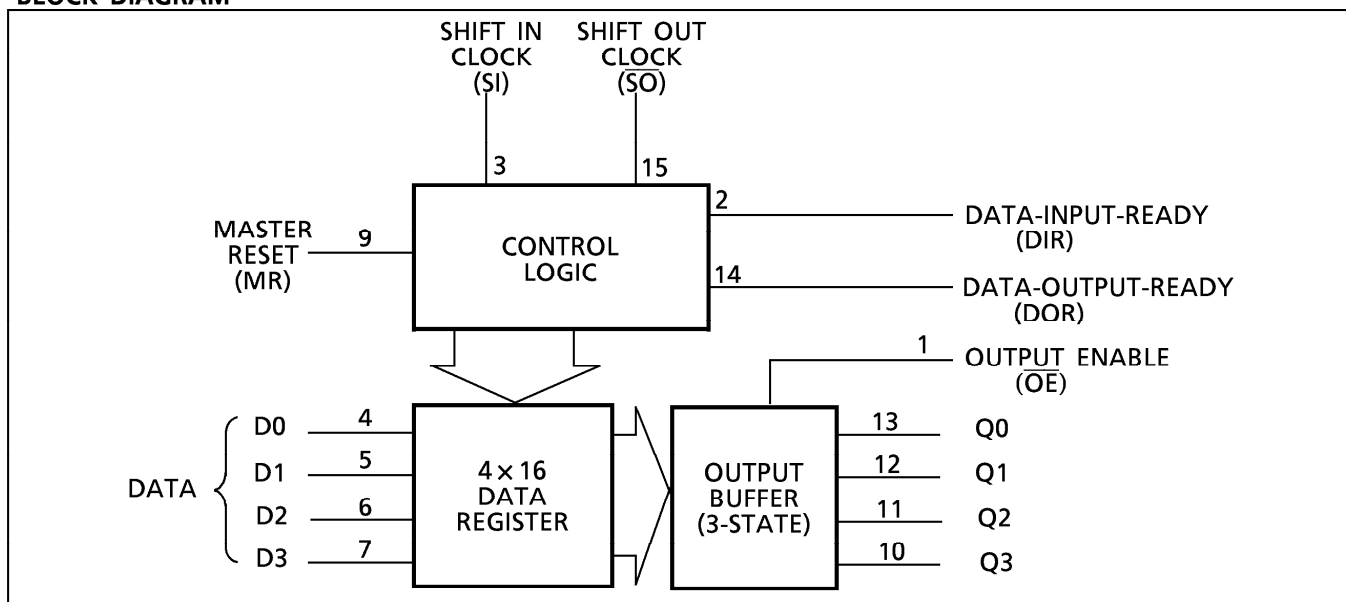
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Timing diagram for the 74VHC04B showing signals: MASTER RESET, OUTPUT ENABLE, SHIFT IN Clock, SHIFT OUT Clock, DATA INPUT READY, DATA OUTPUT READY, DATA IN (Dn), and DATA OUT (Dn). The diagram illustrates the relationship between these signals during normal operation and during invalid states. Key timing parameters are highlighted: approximately 200ns for the shift out clock setup time at $V_{CC} = 4.5V$, and approximately 230ns for the shift out clock hold time at $V_{CC} = 4.5V$. The data output is shown as 'UNKNOWN' during invalid states and 'Z' (high impedance) during normal operation.

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BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

1) WRITING DATA

Data can be written into the FIFO whenever DIR is high and a low to high transition occurs on the SI pin.

DIR will toggle momentarily until the data has been transferred to the second word register.

SI must be toggled before the next 4-bit word can be written. The first and subsequent words will automatically ripple to the output end of the device even if there is not a full 16 words of input data. When all 16 words are filled with data, DIR will go low and additional data cannot be written into the device.

2) READING DATA

When a data word appears in the sixteenth data register (just before the output buffer), DOR goes high and, if $\overline{OE}$ is low, data can be output on the high to low transition of $\overline{SO}$.

The data remaining in the registers now ripples to the next higher word position opening the first word position for new data. DIR goes high and additional data can be written in. During the output of data, DOR toggles momentarily after each read. When the data registers become empty, DOR goes low and $\overline{SO}$ is ignored.

3) MASTER REST

When a high is input to MR, the internal control logic is initialized. This causes DIR to go high and DOR to go low. The contents of the data registers are not changed, but are invalid and will be written over when the first word is loaded.

4) CASCADING

The TC74HC40105A can be cascaded to form longer registers simply by connecting DOR of the first device to SI of the second and DIR of the second device to $\overline{SO}$ of the first. Additional devices may be cascaded by repeating the above. Of course, the Q_n outputs of the first device must be connected to the D_n inputs of the second.

In this mode, an MR pulse must be applied after the supply voltage is turned on. For words wider than 4-bits, the DIR and DOR outputs from each FIFO must be ANDed respectively and the SI and $\overline{SO}$ inputs must each be paralleled.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current (DIR, DOR) (Q0~Q3)	I_{OUT}	± 25 ± 35	mA
DC V_{CC} /Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000 (V_{CC} = 2.0\text{V})$ $0 \sim 500 (V_{CC} = 4.5\text{V})$ $0 \sim 400 (V_{CC} = 6.0\text{V})$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
		(DIR) $I_{OH} = -4\text{ mA}$	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
		(DOR) $I_{OH} = -5.2\text{ mA}$	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
		Q0~Q3 $I_{OH} = -6\text{ mA}$ $I_{OH} = -7.8\text{ mA}$	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		(DIR) $I_{OL} = 4\text{ mA}$	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
		(DOR) $I_{OL} = 5.2\text{ mA}$	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
		Q0~Q3 $I_{OL} = 6\text{ mA}$ $I_{OL} = 7.8\text{ mA}$	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
3 - State Output Off - State Current	I_{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or GND}$	6.0	—	—	± 0.5	—	± 5.0	μA
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	± 0.1	—	± 1.0	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V _{CC} (V)	TYP.	LIMIT	
Minimum Pulse Width (SI)	$t_{W(L)}$ $t_{W(H)}$		2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum Pulse Width ($\overline{\text{SO}}$)	$t_{W(L)}$ $t_{W(H)}$		2.0	—	75	
			4.5	—	15	
			6.0	—	13	
Minimum Pulse Width (MR)	$t_{W(L)}$ $t_{W(H)}$		2.0	—	75	
			4.5	—	15	
			6.0	—	13	
Minimum Set-up Time (DATA—SI)	t_s		2.0	—	0	
			4.5	—	0	
			6.0	—	0	
Minimum Hold Time (DATA—SI)	t_h		2.0	—	100	
			4.5	—	20	
			6.0	—	17	
Minimum Removal Time (MR—SI)	t_{rem}		2.0	—	50	
			4.5	—	10	
			6.0	—	9	
Clock Frequency	f		2.0	—	3	MHz
			4.5	—	15	
			6.0	—	18	

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (DIR, DOR)	t_{TLH}		—	4	8	ns
	t_{THL}					
Propagation Delay Time ($\overline{\text{SO}}$, MR—DOR)	t_{pHL}		—	22	39	
Propagation Delay Time ($\overline{\text{SO}}$ —DIR)	t_{pLH}		—	242	365	
Propagation Delay Time (SI—DOR)	t_{pLH}		—	187	300	
Propagation Delay Time (SI—DIR)	t_{pHL}		—	22	35	
Propagation Delay Time (MR—DIR)	t_{pLH} t_{pHL}		—	25	39	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time (Q0~Q3)	t_{TLH} t_{THL}		50	2.0	—	21	60	—	75	ns
				4.5	—	7	12	—	15	
				6.0	—	6	10	—	13	
Output Transition Time (DIR, DOR)	t_{TLH} t_{THL}		50	2.0	—	24	75	—	95	
				4.5	—	8	15	—	19	
				6.0	—	7	13	—	16	
Propagation Delay Time ($\overline{SO}$, MR—DOR)	t_{pHL}		50	2.0	—	84	225	—	280	
				4.5	—	28	45	—	56	
				6.0	—	24	38	—	48	
Propagation Delay Time ($\overline{SO}$ —DIR)	t_{pLH}		50	2.0	—	798	2000	—	2500	
				4.5	—	266	400	—	500	
				6.0	—	226	340	—	425	
Propagation Delay Time (SI—DOR)	t_{pLH}		50	2.0	—	624	1650	—	2060	
				4.5	—	208	330	—	412	
				6.0	—	177	280	—	350	
Propagation Delay Time (SI—DIR)	t_{pHL}		50	2.0	—	78	200	—	250	
				4.5	—	26	40	—	50	
				6.0	—	22	34	—	43	
Propagation Delay Time ($\overline{SO}$ —Qn)	t_{pLH} t_{pHL}		50	2.0	—	156	400	—	500	
				4.5	—	52	80	—	100	
				6.0	—	44	68	—	85	
			150	2.0	—	171	440	—	550	
				4.5	—	57	88	—	110	
				6.0	—	48	75	—	94	
Propagation Delay Time (SI—Qn)	t_{pLH} t_{pHL}		50	2.0	—	612	1500	—	1875	
				4.5	—	204	300	—	375	
				6.0	—	173	255	—	319	
			150	2.0	—	627	1540	—	1925	
				4.5	—	209	308	—	385	
				6.0	—	178	262	—	327	
Propagation Delay Time (MR—DIR)	t_{pLH} t_{pHL}		50	2.0	—	87	225	—	280	
				4.5	—	29	45	—	56	
				6.0	—	25	38	—	48	
Output Enable time	t_{pZL} t_{pZH}	$R_L = 1\text{k}\Omega$	50	2.0	—	45	125	—	155	
				4.5	—	15	25	—	31	
				6.0	—	13	21	—	26	
			150	2.0	—	60	165	—	205	
				4.5	—	20	33	—	41	
				6.0	—	17	28	—	35	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L = 1\text{k}\Omega$	50	2.0	—	32	125	—	155	
				4.5	—	16	25	—	31	
				6.0	—	14	21	—	26	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6\text{ns}$) (Cont'd)

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f _{MAX}		50	2.0	3	7	—	2.4	—	MHz
				4.5	15	22	—	12	—	
				6.0	18	26	—	14	—	
			150	2.0	2.6	6	—	2	—	
				4.5	13	20	—	10	—	
				6.0	15	24	—	12	—	
Output Pulse Width (DIR)	t _{w(H)} t _{w(L)}		50	2.0	—	95	—	—	—	ns
				4.5	—	25	—	—	—	
				6.0	—	21	—	—	—	
Output Pulse Width (DOR)	t _{w(H)} t _{w(L)}		50	2.0	—	95	—	—	—	
				4.5	—	25	—	—	—	
				6.0	—	21	—	—	—	
Input Capacitance	C _{IN}				—	5	10	—	10	pF
Output Capacitance	C _{OUT}				—	10	—	—	—	
Power Dissipation Capacitance	C _{PD} (1)	Note (1)			—	300	—	—	—	

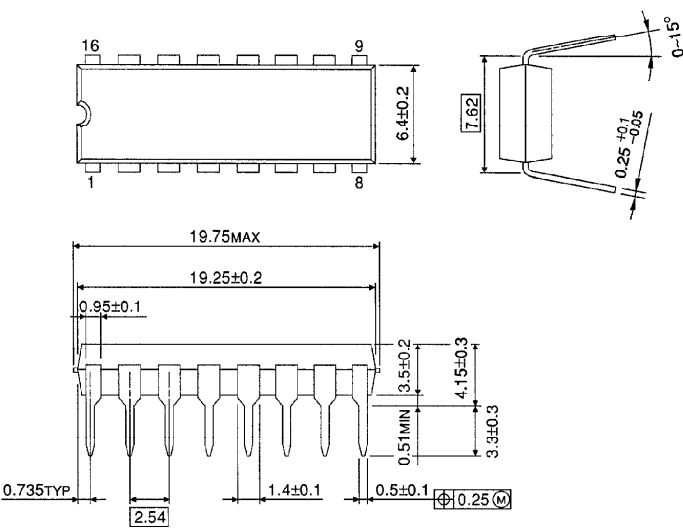
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

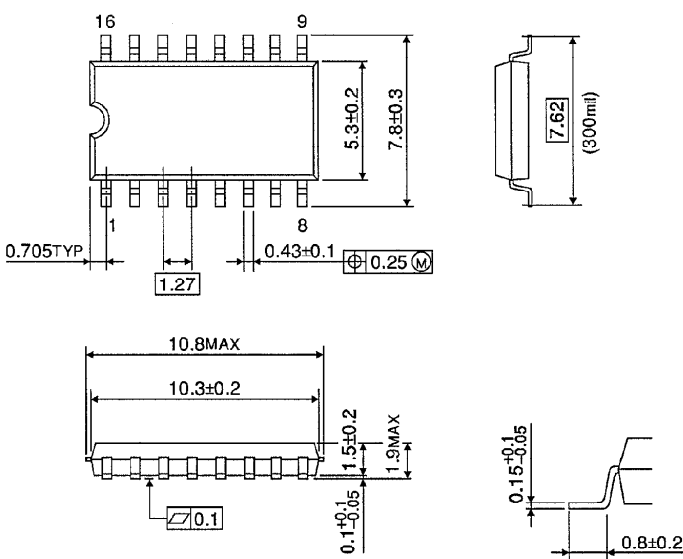
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm



Weight : 0.18g (Typ.)