

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC4044BP, TC4044BF, TC4044BFN

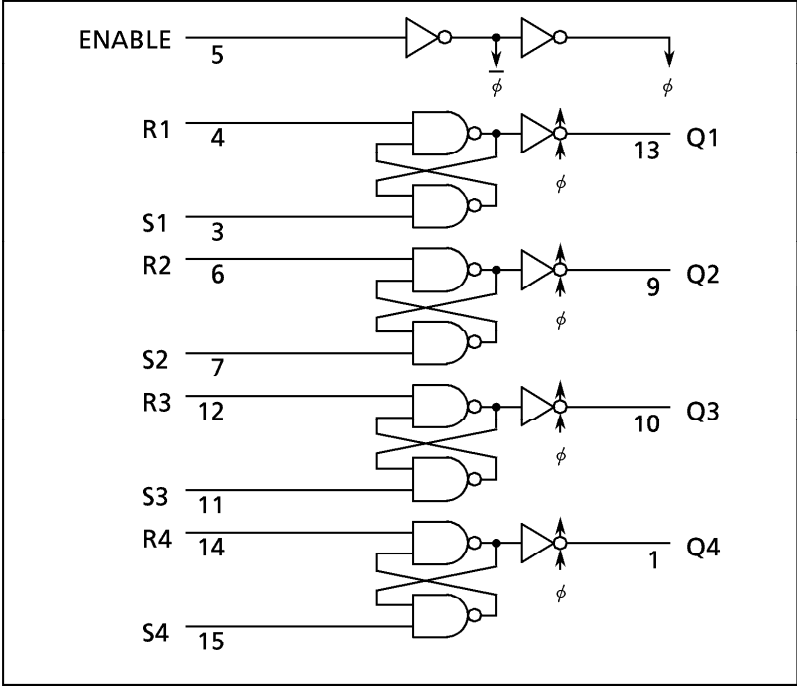
TC4044B QUAD 3-STATE R/S LATCH
(Quad NAND R/S Latch)

TC4044B the latches composed by four independent R/S flip-flop circuits. TC4044B fabricated with NAND gates is suitable for data processing of four bits configuration. four output lines can have high impedance regardless of the contents of latches by means of common ENABLE input to make connection to the bus lines easy.

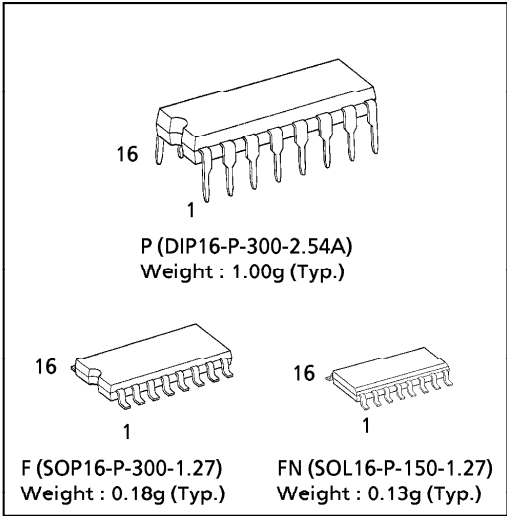
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V _{DD}	V _{SS} - 0.5~V _{SS} + 20	V
Input Voltage	V _{IN}	V _{SS} - 0.5~V _{DD} + 0.5	V
Output Voltage	V _{OUT}	V _{SS} - 0.5~V _{DD} + 0.5	V
DC Input Current	I _{IN}	± 10	mA
Power Dissipation	P _D	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	T _{opr}	- 40~85	°C
Storage Temperature Range	T _{stg}	- 65~150	°C

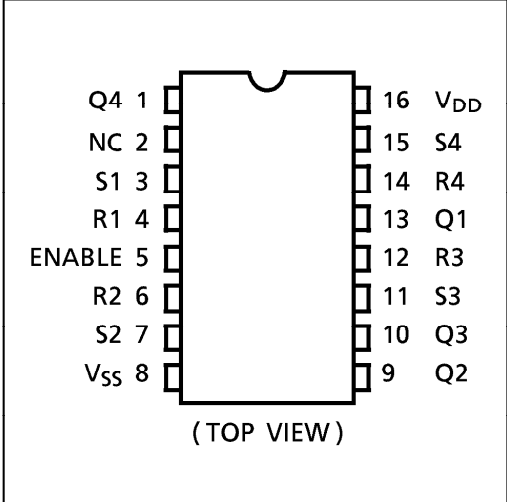
LOGIC DIAGRAM



(Note) The JEDEC SOP (FN) is not available in Japan.



PIN ASSIGNMENT



TRUTH TABLE

R	S	E	Q
*	*	L	HZ
L	L	H	L
L	H	H	L
H	L	H	H
H	H	H	No Change

* : Don't Care
HZ : High Impedance

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● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

RECOMMENDED OPERATING CONDITIONS ($V_{SS} = 0V$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	—	18	V
Input Voltage	V_{IN}		0	—	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS ($V_{SS} = 0V$)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	- 40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V
			10	9.95	—	9.95	10.00	—	9.95	—	
			15	14.95	—	14.95	15.00	—	14.95	—	
Low-Level Output Voltage	V_{OL}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	V
			10	—	0.05	—	0.00	0.05	—	0.05	
			15	—	0.05	—	0.00	0.05	—	0.05	
Output High Current	I_{OH}	$V_{OH} = 4.6V$	5	-0.61	—	-0.51	-1.0	—	-0.42	—	mA
		$V_{OH} = 2.5V$	5	-2.50	—	-2.10	-4.0	—	-1.70	—	
		$V_{OH} = 9.5V$	10	-1.50	—	-1.30	-2.2	—	-1.10	—	
		$V_{OH} = 13.5V$	15	-4.00	—	-3.40	-9.0	—	-2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Output Low Current	I_{OL}	$V_{OL} = 0.4V$	5	0.61	—	0.51	1.2	—	0.42	—	mA
		$V_{OL} = 0.5V$	10	1.50	—	1.3	3.2	—	1.10	—	
		$V_{OL} = 1.5V$	15	4.00	—	3.4	12.0	—	2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Input High Voltage	V_{IH}	$V_{OUT} = 0.5V, 4.5V$	5	3.5	—	3.5	2.75	—	3.5	—	V
		$V_{OUT} = 1.0V, 9.0V$	10	7.0	—	7.0	5.50	—	7.0	—	
		$V_{OUT} = 1.5V, 13.5V$	15	11.0	—	11.0	8.25	—	11.0	—	
		$ I_{OUT} < 1\mu A$									
Input Low Voltage	V_{IL}	$V_{OUT} = 0.5V, 4.5V$	5	—	1.5	—	2.25	1.5	—	1.5	V
		$V_{OUT} = 1.0V, 9.0V$	10	—	3.0	—	4.50	3.0	—	3.0	
		$V_{OUT} = 1.5V, 13.5V$	15	—	4.0	—	6.75	4.0	—	4.0	
		$ I_{OUT} < 1\mu A$									
Input Current	"H" Level	I_{IH}	$V_{IH} = 18V$	18	—	0.1	—	10^{-5}	0.1	—	μA
	"L" Level	I_{IL}	$V_{IL} = 0V$	18	—	-0.1	—	-10^{-5}	-0.1	—	
3-State Output Leakage Current	"H" Level	I_{DH}	$V_{OH} = 18V$	18	—	0.4	—	10^{-4}	0.4	—	
	"L" Level	I_{DL}	$V_{OL} = 0V$	18	—	-0.4	—	-10^{-4}	-0.4	—	
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{SS}, V_{DD} *$	5	—	1	—	0.002	1	—	30	
			10	—	2	—	0.004	2	—	60	
			15	—	4	—	0.008	4	—	120	

* All valid input combinations.

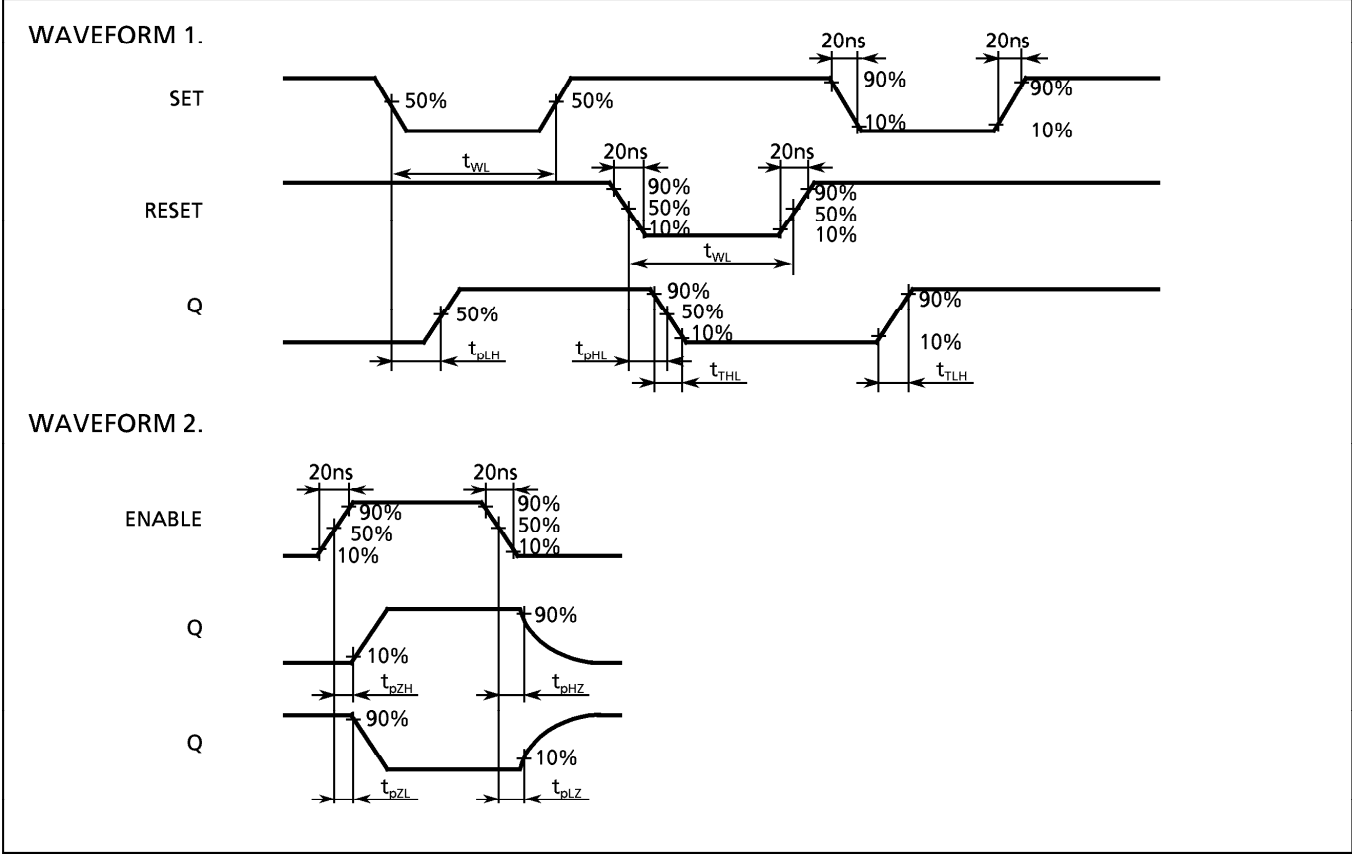
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DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vss = 0V, CL = 50pF)

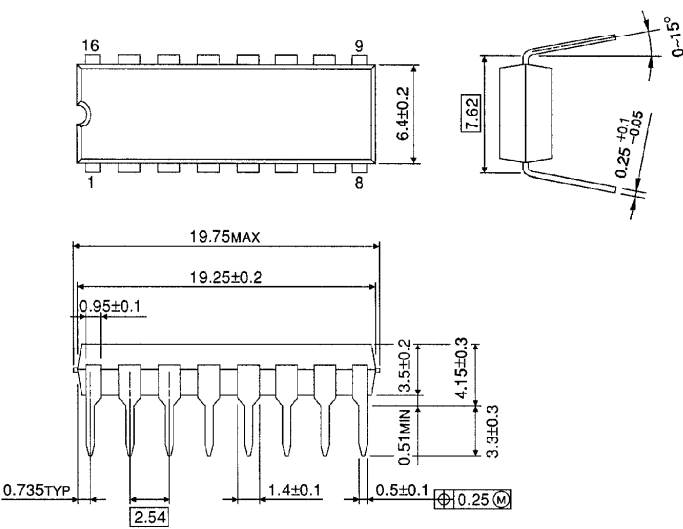
CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t _{TLH}		5 10 15	— — —	70 35 30	200 100 80	ns
Output Transition Time (High to Low)	t _{THL}		5 10 15	— — —	70 35 30	200 100 80	
Propagation Delay Time (SET, RESET - Q)	t _{pLH} t _{pHL}		5 10 15	— — —	90 45 35	300 140 100	
3-State Propagation Delay Time (ENABLE - Q)	t _{pHZ} t _{pZH}	R _L = 1kΩ	5 10 15	— — —	55 35 30	180 100 70	
3-State Propagation Delay Time (ENABLE - Q)	t _{pZH} t _{pZL}	R _L = 1kΩ	5 10 15	— — —	55 30 25	180 100 70	
Min. Pulse Width (SET, RESET)	t _{WL}		5 10 15	— — —	25 20 20	160 80 40	
Input Capacitance	C _{IN}			—	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

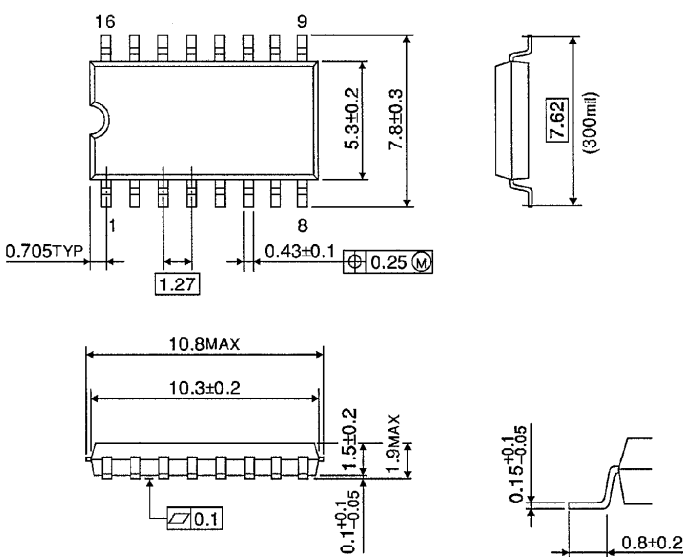
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm

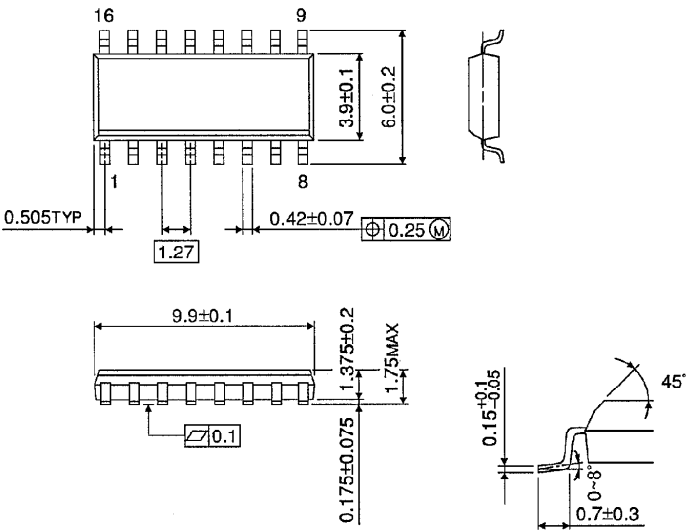


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150-1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)