TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HCT139AP, TC74HCT139AF, TC74HCT139AFN

DUAL 2 – TO – 4 LINE DECODER

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74HCT139A is a high speed CMOS 2 - to - 4 LINE DECODER / DEMULTIPLEXER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

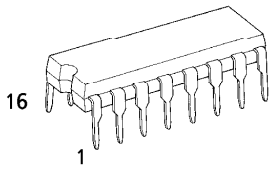
The active low enable input can be used for gating or it can be used as a data input for demultiplexing applications.

When the enable input is held "H", all four outputs are fixed at a high logic level independent of the other inputs.

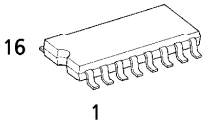
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

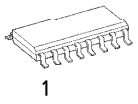
- High Speed ····· t_{pd} = 17ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- Compatible with TTL outputs ···· V_{IH} = 2V(Min.)
  V_{IL} = 0.8V(Max.)
- Wide Interfacing ability ····· LSTTL, NMOS, CMOS
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· | I_{OH} | = I_{OL} = 4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74LS139



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

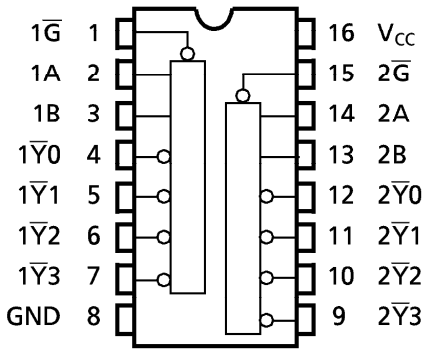


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)



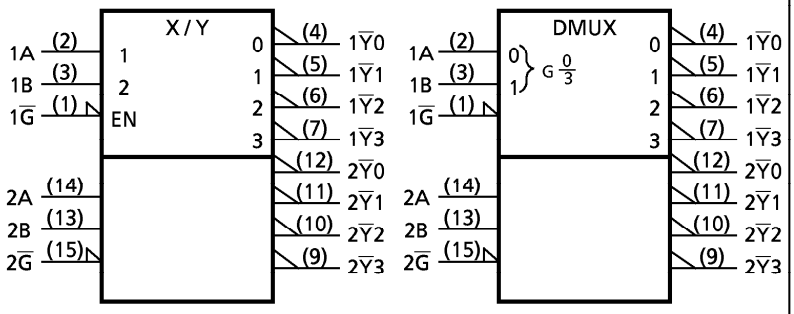
FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS			OUTPUTS				SELECTED OUTPUT
ENABLE	SELECT						
G̅	B	A	Y̅0	Y̅1	Y̅2	Y̅3	
H	X	X	H	H	H	H	NONE
L	L	L	L	H	H	H	Y̅0
L	L	H	H	L	H	H	Y̅1
L	H	L	H	H	L	H	Y̅2
L	H	H	H	H	H	L	Y̅3

X : Don't Care

961001EBA2

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} / Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta= −40°C~65°C. From Ta=65°C to 85 °C a derating factor of −10mW/ °C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			4.5 ~ 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = −4 mA	4.5	4.18	4.31	—	4.13	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	μA
	I_C	PER INPUT: V_{IN} = 0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	—	—	2.0	—	2.9	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	12	ns
Propagation Delay Time (A, B−$\overline{Y}$)	t_{pLH} t_{pHL}		—	15	25	
Propagation Delay Time ($\overline{G}$−$\overline{Y}$)	t_{pLH} t_{pHL}		—	14	23	

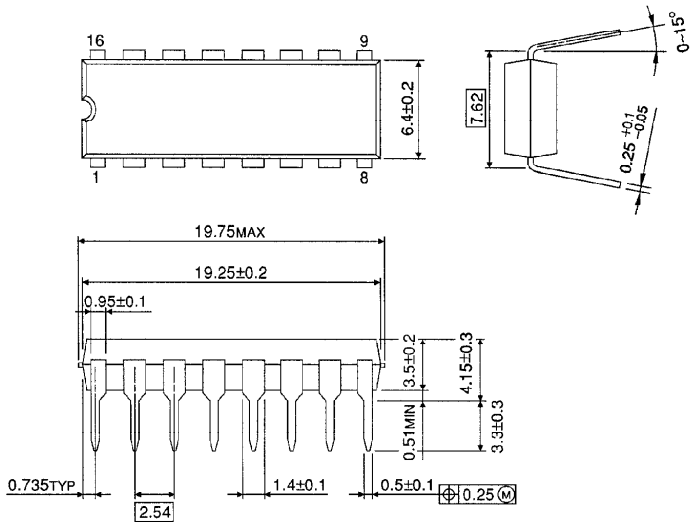
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5 5.5	— —	8 7	15 14	— —	19 17	ns
Propagation Delay Time (A, B−$\overline{Y}$)	t_{pLH} t_{pHL}		4.5 5.5	— —	19 16	30 27	— —	38 35	
Propagation Delay Time ($\overline{G}$−$\overline{Y}$)	t_{pHL}		4.5 5.5	— —	17 14	27 25	— —	34 31	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD} (1)			—	40	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

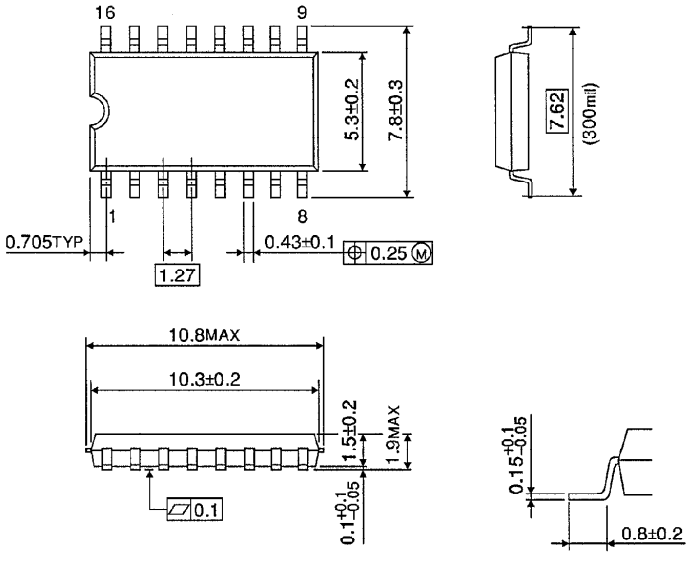
$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Decoder)}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

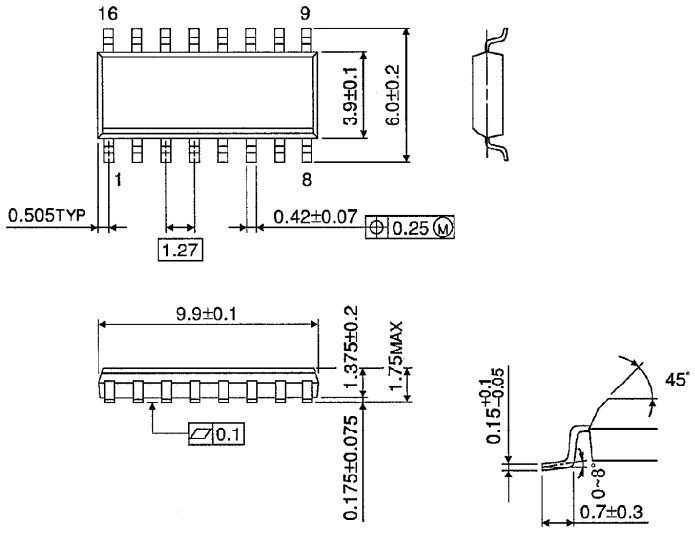
SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)