

TC7SB385FU

Single Bus Switch

The TC7SB385FU provides single bit of high-speed TTL-compatible switching. The low on resistance of the switch allows connections to be made with minimal propagation delay.

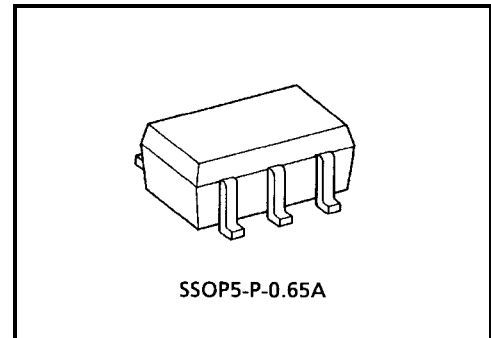
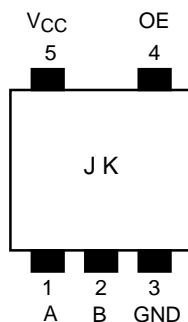
The device is organized as just 1-bit low-impedance switch with output-enable (OE) input. When OE is high, the switch is on and data can flow from port A to port B, or vice versa. When OE is low, the switch is open and a high-impedance state exists between the two ports.

All inputs are equipped with protection circuits against static discharge.

Features

- Operating voltage: $V_{CC} = 4.5 \sim 5.5 \text{ V}$
- High speed operation: $t_{pd} = 0.25 \text{ ns (max)}$
- Low on resistance: $R_{ON} = 5 \Omega \text{ (typ.)}$
- ESD performance: Machine model $> \pm 200 \text{ V}$
Human body model $> \pm 2000 \text{ V}$
- TTL level input (control input)
- Package: USV

Pin Assignment (top view)

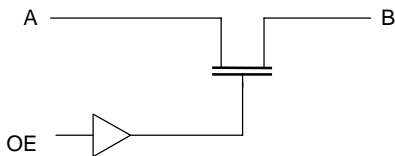


Weight: 0.006 g (typ.)

Truth Table

Input	Function
OE	
L	Disconnect
H	A port = B port

System Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply range	V_{CC}	-0.5~7.0	V
DC input voltage	V_{IN}	-0.5~7.0	V
DC switch voltage	V_S	-0.5~7.0	V
Input diode current	I_{IK}	-50	mA
Continuous channel current	I_S	128	mA
Power dissipation	P_D	200	mW
DC V_{CC}/GND current	I_{CC}/I_{GND}	± 100	mA
Storage temperature	T_{stg}	-65~150	$^{\circ}C$

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5~5.5	V
Input voltage	V_{IN}	0~5.5	V
Switch voltage	V_S	0~5.5	V
Operating temperature	T_{opr}	-40~85	$^{\circ}C$
Input rise and fall time	dt/dv	0~10	ns/V

Electrical Characteristics

DC Characteristics (Ta = -40~85°C)

Characteristics		Symbol	Test Condition		Min	Typ. (Note1)	Max	Unit
				V _{CC} (V)				
Input voltage	"H" level	V _{IH}	—	4.5~5.5	2.0	—	—	V
	"L" level	V _{IL}	—	4.5~5.5	—	—	0.8	
Input leakage current		I _{IN}	V _{IN} = 0~5.5 V	4.5~5.5	—	—	±1.0	μA
Power off leakage current		I _{OFF}	A, B, OE = 0~5.5 V	0	—	—	±1.0	μA
Off-state leakage current (switch off)		I _{SZ}	A, B = 0~5.5 V, OE = GND	4.5~5.5	—	—	±1.0	μA
ON resistance (Note2)	R _{ON}	V _{IS} = 0 V	I _{IS} = 30 mA	4.5	—	5	7	Ω
			I _{IS} = 64 mA	4.5	—	5	7	
		V _{IS} = 2.4 V, I _{IS} = 15 mA		4.5	—	10	15	
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND, I _{OUT} = 0	5.5	—	—	10	μA
		ΔI _{CC}	V _{IN} = 3.4 V (one input)	5.5	—	—	2.5	mA

Note1: Typical values are at V_{CC} = 5 V and Ta = 25°C.

Note2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Characteristics (Ta = -40~85°C)

Characteristics		Symbol	Test Condition		Min	Max	Unit
				V _{CC} (V)			
Propagation delay time (bus to bus)		t _{pLH} t _{pHL}	Figure 1, Figure 2 (Note3)	4.5	—	0.25	ns
Output enable time		t _{pZL} t _{pZH}	Figure 1, Figure 3	4.5	—	4.0	ns
Output disable time		t _{pLZ} t _{pHZ}	Figure 1, Figure 3	4.5	—	5.0	ns

Note3: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitive Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition		Typ.	Unit
				V _{CC} (V)		
Control pin input capacitance		C _{IN}	(Note4)	5.0	3	pF
Switch terminal capacitance		C _{I/O}	OE = GND (Note4)	5.0	10	pF

Note4: This item is guaranteed by design.

Switch

Open

7.0 V

GND

Output

Measure

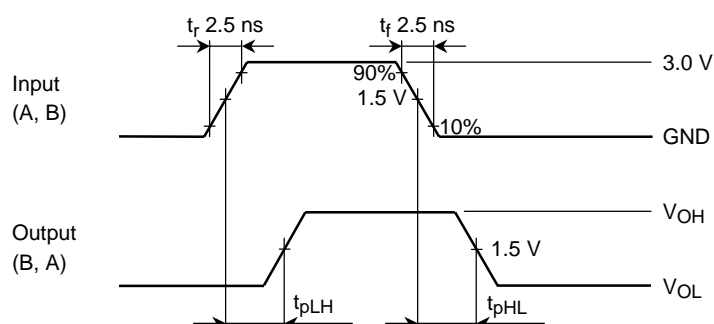
R_L

C_L

$C_L = 50 \text{ pF}$

$R_L = 500 \Omega$

Parameter	Switch
t_{pLH} , t_{pHL}	Open
t_{pLZ} , t_{pZL}	7.0 V
t_{pHZ} , t_{pZH}	Open



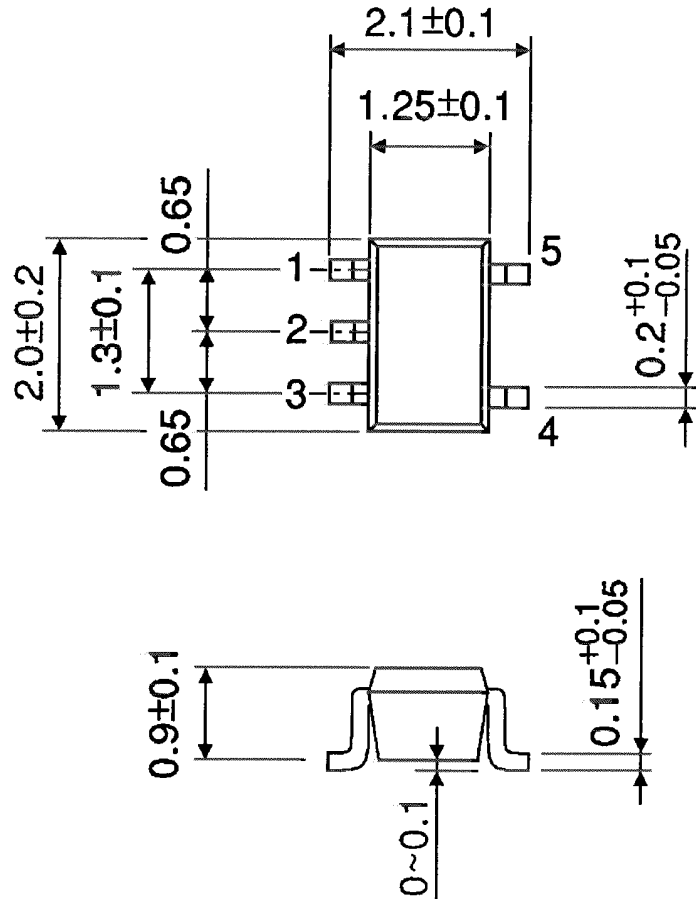
The diagram illustrates the timing characteristics of the 74VHC125. It shows three waveforms: Output Enable (OE), Output (A, B) Low to Off to Low, and Output (A, B) High to Off to High. The OE signal is a square wave with a rise time t_r of 2.5 ns. The output signals show the transition from a low state to an off state (high impedance) and back to a low state. Key timing parameters include t_{pLZ} (propagation delay from OE falling to output low), t_{pZL} (propagation delay from OE rising to output low), t_{pHZ} (propagation delay from OE falling to output high), and t_{pZH} (propagation delay from OE rising to output high). Voltage levels are marked at 3.0 V, GND, 1.5 V, $V_{OL} + 0.3$ V, and $V_{OH} - 0.3$ V. The diagram also indicates periods where the outputs are enabled, disabled, and enabled again.

Figure 3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

Package Dimensions

SSOP5-P-0.65A

Unit : mm



Weight: 0.006 g (typ.)

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