TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC652AP

OCTAL BUS TRANSCEIVER / REGISTER (3-STATE)

The TC74HC652A is high speed CMOS OCTAL BUS TRANSCEIVER / REGISTER fabricated with silicon gate CMOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

When the enable input GAB and $\overline{GBA}$ are held high, the A1 thru A8 become inputs and the B1 thru B8 become outputs. When the GAB and $\overline{GBA}$ are held low, the A1 thru A8 become output and the B1 thru B8 become inputs. When GAB is low and $\overline{GBA}$ is high, the outputs functions of the A and B Busses are disabled.

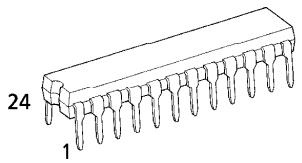
The select inputs (SAB, SBA) can multiplex stort and real-time (transparent mode) data.

Data on the A Bus or B Bus can be clocked into the registers on the positive going transition of either CAB or CBA clock inputs, respectively.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

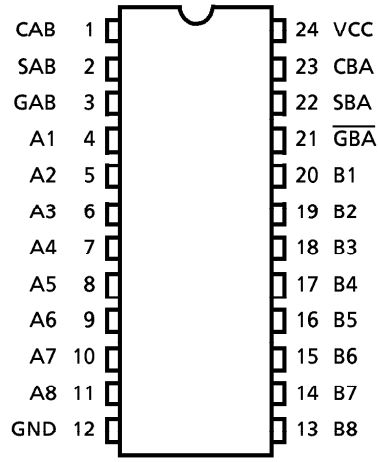
FEATURES :

- High Speed ····· f_{MAX} = 73MHz (typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 6mA (Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr.) = 2V ~ 6V
- Pin and Function Compatible with 74LS652

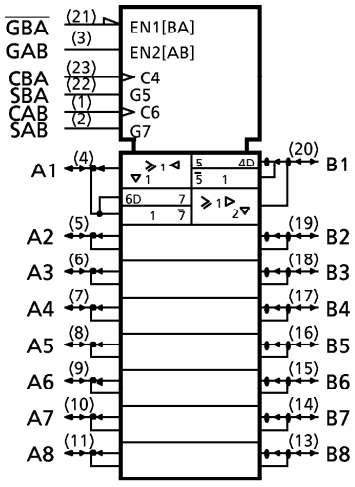


P (DIP24-P-300-2.54)
Weight : 1.50g (Typ.)

PIN ASSIGNMENT



IEC LOGIC SYSTEMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

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TRUTH TABLE

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	Function
L	H	X*	X*	X	X	INPUTS Z	INPUTS Z	The output functions of A and B Busses are disabled.
		↑	↑	X	X	X	X	Both A and B Busses are used as inputs to the internal flip-flops. Data on the Bus will be stored on the rising edge of the Clock.
L	L	X*	X*	X	L	OUTPUTS L H	INPUTS L H	The data on the B bus are displayed on the A bus.
		X*	↑	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X*	X*	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	↑	X	H	L H	L H	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.
H	H	X*	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus.
		↑	X*	L	X	L H	L H	The data on the A Bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X*	X*	H	X	X	Qn	The data in the A storage flip-flops are displayed on the B Bus.
		↑	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
H	L	X*	X*	H	H	OUTPUTS Qn	OUTPUTS Qn	The data in the A storage flip-flops are displayed on the B Bus, and the data in the B storage flip-flops are displayed onthe A

Notes : X : Don't Care
Qn : The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.
Z : High Impedance
* The clocks are not internally gated with either Output Enable or Select Inputs. Therefore, data on the A and/or B Busses may be clocked into the storage flip-flops at any time.

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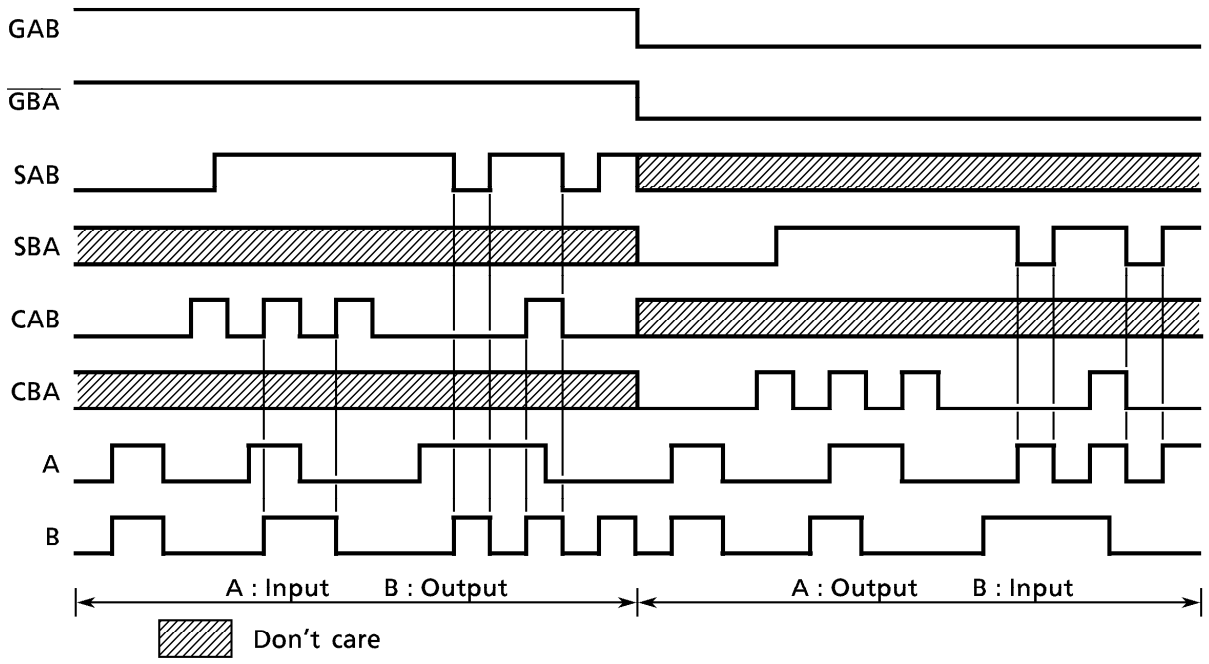
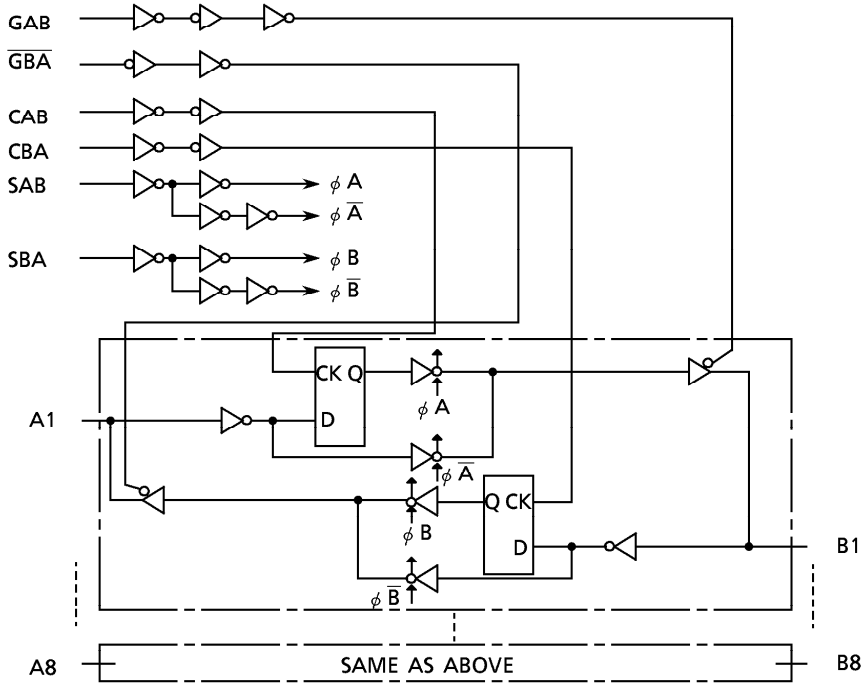
TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500 (DIP)*	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta= −40°C~65°C. From Ta=65°C to 85 °C a derating factor of −10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC} = 2.0V) 0~ 500 (V_{CC} = 4.5V) 0~ 400 (V_{CC} = 6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
			I_{OH} = −6 mA I_{OH} = −7.8mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I_{OL} = 6 mA I_{OL} = 7.8mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		Ta = −40~85°C	UNIT
			V_{CC} (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set-up Time	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			CL (pF)	V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time (BUS−BUS)	t_{pLH} t_{pHL}		50	2.0	−	74	150	−	190	
				4.5	−	21	30	−	38	
				6.0	−	18	26	−	32	
			150	2.0	−	91	190	−	240	
				4.5	−	26	38	−	48	
				6.0	−	22	32	−	41	
Propagation Delay Time (CAB, CBA−BUS)	t_{pLH} t_{pHL}		50	2.0	−	98	210	−	265	
				4.5	−	28	42	−	53	
				6.0	−	24	36	−	45	
			150	2.0	−	116	250	−	315	
				4.5	−	33	50	−	63	
				6.0	−	28	43	−	54	
Propagation Delay Time (SAB, SBA−BUS)	t_{pLH} t_{pHL}		50	2.0	−	81	170	−	215	
				4.5	−	23	34	−	43	
				6.0	−	20	29	−	37	
			150	2.0	−	98	210	−	265	
				4.5	−	28	42	−	53	
				6.0	−	24	36	−	45	
Propagation Enable Time (GAB, $\overline{GBA}$−BUS)	t_{pZL} t_{pZH}	$R_L = 1k\Omega$	50	2.0	−	74	175	−	220	
				4.5	−	21	35	−	44	
				6.0	−	18	30	−	37	
			150	2.0	−	91	215	−	270	
				4.5	−	26	43	−	54	
				6.0	−	22	37	−	46	
Output Disable time (GAB, $\overline{GBA}$−BUS)	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	50	2.0	−	50	175	−	220	
				4.5	−	21	35	−	44	
				6.0	−	18	30	−	37	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6ns$) (Cont'd)

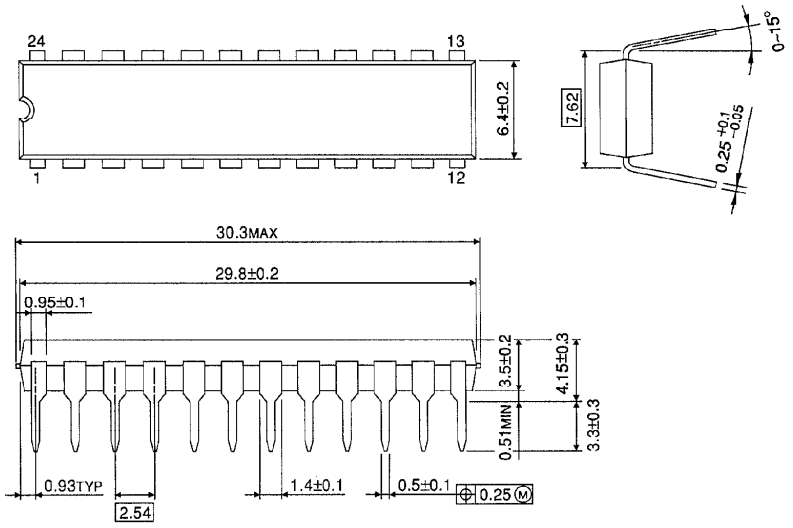
PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Maximum Clock Frequency	f_{MAX}		50	2.0	6	19	—	5	—	MHz
				4.5	31	67	—	25	—	
				6.0	36	79	—	29	—	
Input Capacitance	C_{IN}				—	5	10	—	10	pF
Output Capacitance	C_{OUT}				—	13	—	—	—	
Power Dissipation Capacitance	C_{PD} (1)				—	39	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$ (per bit)

DIP 24PIN OUTLINE DRAWING (DIP24-P-300-2.54) Unit in mm



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