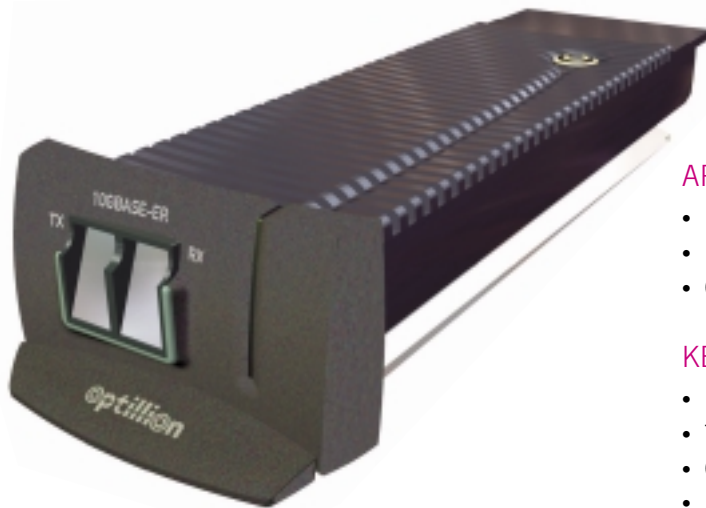


PRODUCT BRIEF



DESCRIPTION

Optillion 10 Gbit/s Ethernet Fiber Optic Transceiver module TOP 3010-LC ($\lambda=1310$ nm) is a highly integrated Ethernet PHY, that provides high-speed serial links at an optical signaling rate of 10.3 Gbit/s. Optillion Ethernet modules are compliant with IEEE 802.3ae draft standard.

These modules are Hot Swappable and permit easy configuration in manufacturing and field for different transmission distances. Extensive test-and management features ease design integration and field maintenance.

The interface to the MAC is a four lane XAUI electrical differential link operating at 4x3.125 Gbit/s. Optillion modules are Class 1 laser safe products, designed according to Telcordia GR-468-CORE for reliability.

APPLICATIONS

- Ethernet metro/aggregation switches.
- Edge/core routers.
- Communication test equipment.

KEY FEATURES

- Highly integrated Ethernet PHY.
- True system "Hot-Swappable".
- Configurable through MDIO.
- Extensive Built-In Self-Test.
- Small footprint.
- Low power consumption 5 W.
- Standard +3.3 V and +5.0 V supply.
- Allows extended traces on PCB.
- Built in back plane transceivers.
- No fiber pigtails, LC™ receptacles.
- Low connector pin count (70).

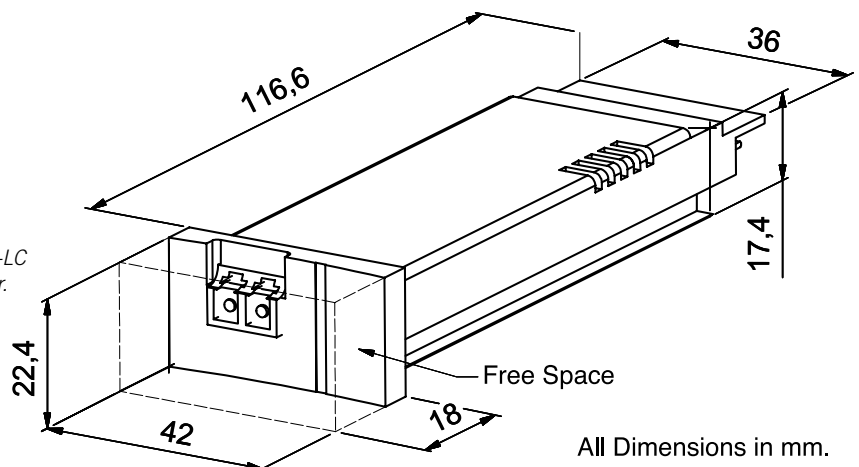
BENEFITS FOR EQUIPMENT MANUFACTURERS

- Hot Swappable concept for ease of design and manufacturing.
- Shelf distributed 10 GbE I/O ports.
- Miniaturized, low power modules.
- XENPAK multi-sourced form factor.

BENEFITS FOR SERVICE PROVIDERS

- Ethernet transmission up to 10 km over single mode fiber.
- Field configurable on-line.

Figure 1 –Mechanical outline for TOP 3010-LC 1310 nm single mode fiber optic transceiver.



All Dimensions in mm.

The diagram illustrates the 10 GbE PHY architecture, divided into four main functional blocks:

- 10 GBIT MAC:** Contains a MAC/RS block and an MI-M block. It interfaces with the SYSTEM BUS via HOSTBUS and HOST_MIIM signals.
- XGMII:** A 312.25 MHz interface between the MAC and the transceiver. It carries 36-bit TRANSMIT DATA, CLK, and RECEIVE DATA, CLK signals.
- XAUI:** A 4 X 3.125 Gbd interface between the MAC and the transceiver. It carries 36-bit signals for XAUI[0-3]IX, XAUI[0-3]IY, XAUI[0-3]OX, and XAUI[0-3]OY.
- OPTILLION XAUI 10 GBIT ETHERNET TRANSCEIVER:** Contains several internal blocks:
 - XGXS:** Receives data from the XGMII and XAUI.
 - PCS (64B66B CODE):** Processes the data into 64B66B code.
 - PMA (SERDES):** Serializes the data.
 - PMD (SERIAL OPTICAL XCVR):** Converts the electrical signal to optical.
 - MDIO, MDIOT, MDCH, MDIOH, MDIOA[0-4]:** Management interface signals.
 - MDIO and BIST:** Internal control and testing blocks.

The final output is a 10.3 G bd optical signal.

TRANSMIT PATH

The data is passed to XGXS. The encoder does an 8B/10B encoding, and data is sent out on the XAU1 output.

An MDIO interface is available for communication of transceiver status to for example a device processor. The MDIO implements the relevant addresses, status and preference registers (XGXS, 64B/66B PCS and PMA). Optionally tailored functionality may include:

Note: Latest information about the XENPAK MSA and detailed specifications: www.xenpak.org

The detector diode is detecting the incoming light. The output from the diode is amplified in the PMD. The clock is recovered and the PMA deserialize the incoming data and forward data to the RX part of the PCS. After frame synchronization (frame lock acquired) and descrambling, decoding of the 64B/66B encoded data is done to an internal parallel interface after clock rate adaptation.

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