

262,144-WORD BY 16-BIT STATIC RAM

DESCRIPTION

The TC554161FTI is a 4,194,304-bit static random access memory (SRAM) organized as 262,144 words by 16 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5 V ± 10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 10 mA/MHz (typ) and a minimum cycle time of 85 ns. It is automatically placed in low-power mode at 200 μA standby current (max) when chip enable (CE) is asserted high. There are two control inputs. CE is used to select the device and for data retention control, and output enable (OE) provides fast memory access. Data byte control pin (LB, UB) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of - 40° to 85°C, the TC554161FTI can be used in environments exhibiting extreme temperature conditions. The TC554161FTI is available in a plastic 54-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
Operating: 55 mW/MHz(typical)
- Standby current of 200 μA (maximum)
- Single power supply voltage of 5 V ± 10%
- Power down features using CE.
- Data retention supply voltage of 2 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of - 40° to 85°C

- Access Times (maximum):

	TC554161FTI	
	-85	-10
Access Time	85 ns	100 ns
CE Access Time	85 ns	100 ns
OE Access Time	45 ns	50 ns

- Package:
TSOP II 54-P-400-0.80 (FTI) (Weight: 0.55 g typ)

PIN ASSIGNMENT (TOP VIEW)

NC	1	54	A4
A3	2	53	A5
A2	3	52	A6
A1	4	51	A7
A0	5	50	NC
I/O16	6	49	I/O1
I/O15	7	48	I/O2
VDD	8	47	VDD
GND	9	46	GND
I/O14	10	45	I/O3
I/O13	11	44	I/O4
UB	12	43	LB
CE	13	42	OE
OP	14	41	OP
R/W	15	40	NC
I/O12	16	39	I/O5
I/O11	17	38	I/O6
GND	18	37	GND
VDD	19	36	VDD
I/O10	20	35	I/O7
I/O9	21	34	I/O8
NC	22	33	A8
A17	23	32	A9
A16	24	31	A10
A15	25	30	A11
A14	26	29	A12
A13	27	28	NC

(Normal pinout)

PIN NAMES

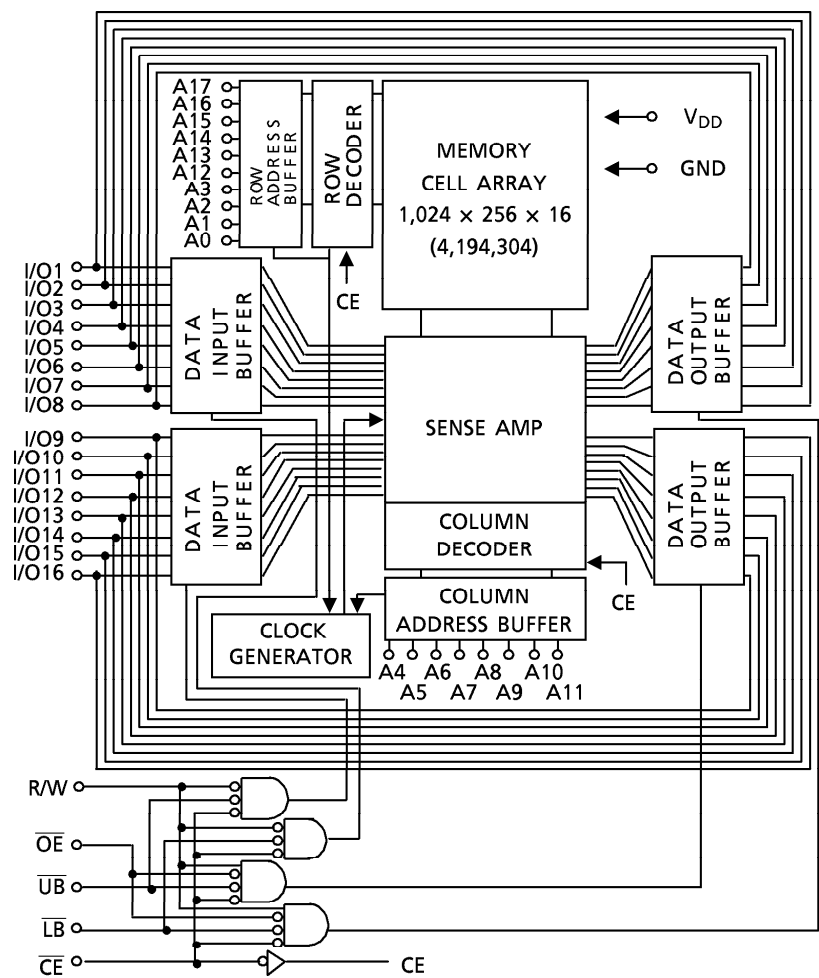
A0 to A17	Address Inputs
I/O1 to I/O16	Data Inputs/Outputs
CE	Chip Enable
R/W	Read/Write Control
OE	Output Enable
LB, UB	Data Byte Control Input
VDD	Power (+ 5 V)
GND	Ground
NC	No Connection
OP*	Option

*: OP pin must be open or connected to GND.

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BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	- 0.3 to 7.0	V
V_{IN}	Input Voltage	- 0.3 * to 7.0	V
$V_{I/O}$	Input/Output Voltage	- 0.5 to $V_{DD} + 0.5$	V
P_D	Power Dissipation	0.6	W
T_{solder}	Soldering Temperature (10 s)	260	°C
T_{strg}	Storage Temperature	- 55 to 150	°C
T_{opr}	Operating Temperature	- 40 to 85	°C

* - 3.0 V when measured at a pulse width of 30 ns

DC RECOMMENDED OPERATING CONDITIONS ($T_a = - 40^{\circ}$ to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	- 0.3 *	-	0.6	V
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

* - 3.0 V when measured at a pulse width of 30 ns

DC CHARACTERISTICS ($T_a = -40^\circ\text{ to }85^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DD}			–	–	± 1.0	μA
I _{LO}	Output Leakage Current	CE = V _{IH} or R/W = V _{IL} or OE = V _{IH} V _{OUT} = 0 V to V _{DD}			–	–	± 1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4 V			– 1.0	–	–	mA
I _{OL}	Output Low Current	V _{OL} = 0.4 V			2.1	–	–	mA
I _{DDO 1}	Operating Current	CE = V _{IL} R/W = V _{IH} , I _{OUT} = 0 mA Other Inputs = V _{IH} /V _{IL}	Tcycle	min	–	–	100	mA
I _{DDO 2}				1 μs	–	15	–	
		CE = 0.2 V R/W = V _{DD} – 0.2 V, I _{OUT} = 0 mA Other Inputs = V _{DD} – 0.2 V/0.2 V	Tcycle	min	–	–	90	mA
1 μs				–	10	–		
I _{DDS 1}	Standby Current	CE = V _{IH}			–	–	3	mA
I _{DDS 2}		CE = V _{DD} – 0.2 V, Ta = – 40° to 85°C V _{DD} = 2.0 to 5.5 V			–	–	200	μA

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High-Z	Output	I_{DDO}
				L	H	Output	High-Z	I_{DDO}
Write	L	x	L	L	L	Input	Input	I_{DDO}
				H	L	High-Z	Input	I_{DDO}
				L	H	Input	High-Z	I_{DDO}
Outputs Disable	L	H	H	x	x	High-Z	High-Z	I_{DDO}
	L	x	x	H	H			
Standby	H	x	x	x	x	High-Z	High-Z	I_{DDS}

x = don't care
H = logic high
L = logic low

AC CHARACTERISTICS AND OPERATING CONDITIONS ($T_a = -40^\circ\text{ to }85^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 10\%$)READ CYCLE

SYMBOL	PARAMETER	TC554161FTI				UNIT
		-85		-10		
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	85	–	100	–	ns
t _{ACC}	Address Access Time	–	85	–	100	
t _{CO}	Chip Enable Access Time	–	85	–	100	
t _{OE}	Output Enable Access Time	–	45	–	50	
t _{BA}	Data Byte Control Access Time	–	45	–	50	
t _{OH}	Output Data Hold Time	10	–	10	–	
t _{COE}	Chip Enable Low to Output Active	5	–	5	–	
t _{OEE}	Output Enable Low to Output Active	0	–	0	–	
t _{BE}	Data Byte Control Low to Output Active	0	–	0	–	
t _{OD}	Chip Enable High to Output High-Z	–	35	–	40	
t _{ODO}	Output Enable High to Output High-Z	–	35	–	40	
t _{BD}	Data Byte Control High to Output High-Z	–	35	–	40	

WRITE CYCLE

SYMBOL	PARAMETER	TC554161FTI				UNIT
		-85		-10		
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	85	–	100	–	ns
t _{WP}	Write Pulse Width	55	–	60	–	
t _{CW}	Chip Enable to End of Write	70	–	80	–	
t _{BW}	Data Byte Control to End of Write	55	–	60	–	
t _{AS}	Address Setup Time	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	
t _{DS}	Data Setup Time	35	–	40	–	
t _{DH}	Data Hold Time	0	–	0	–	
t _{OE_W}	R/W High to Output Active	0	–	0	–	
t _{OD_W}	R/W Low to Output High-Z	–	35	–	40	

AC TEST CONDITIONS

Output load: 100 pF + one TTL gate

Input pulse level: 0.4 V, 2.6 V

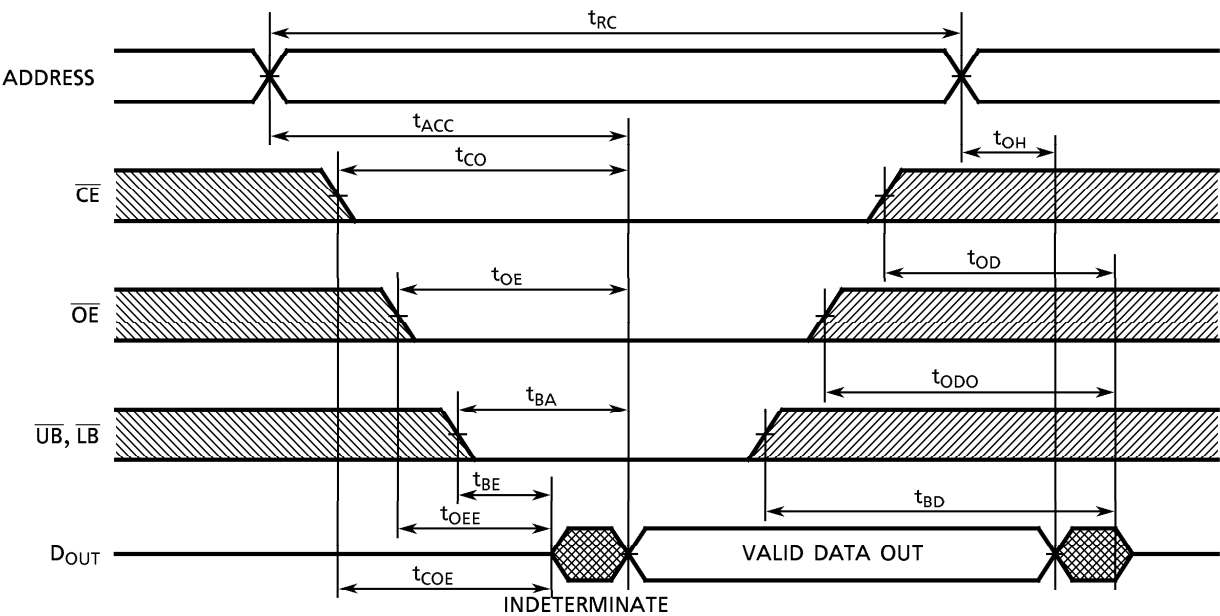
Timing measurements: 1.5 V

Reference level: 1.5 V

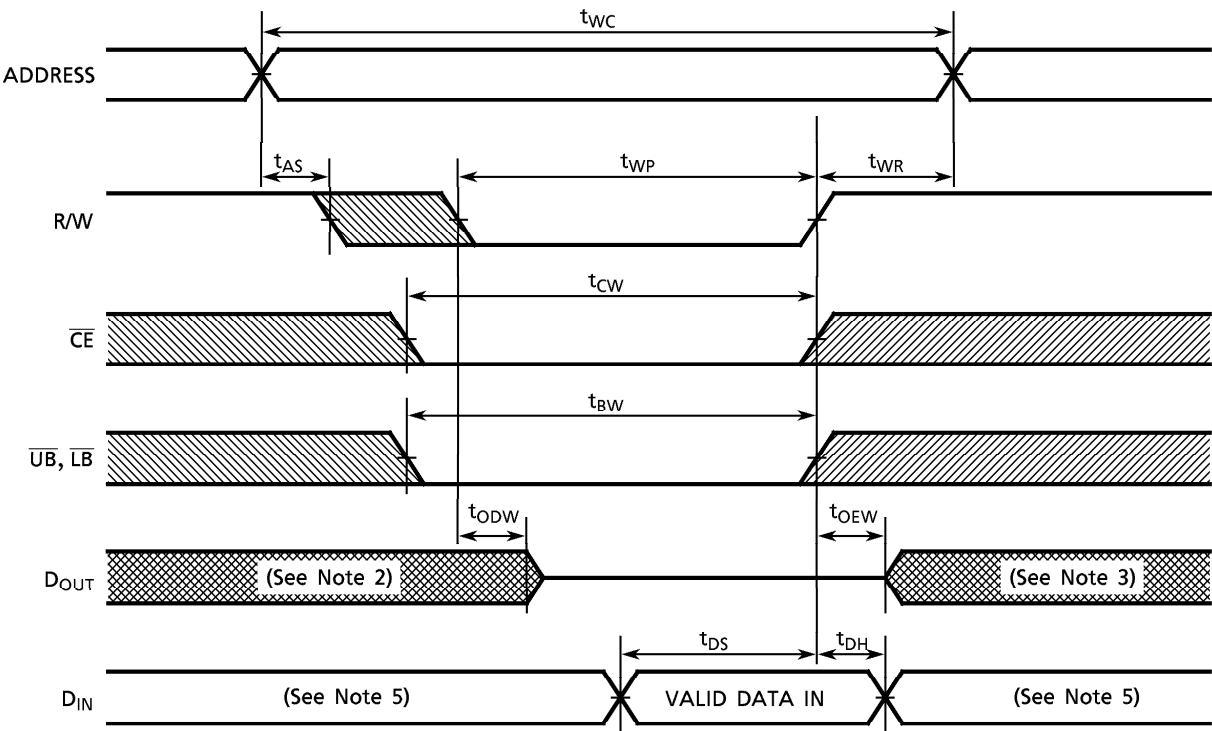
 t_R, t_F : 5 ns

TIMING DIAGRAMS

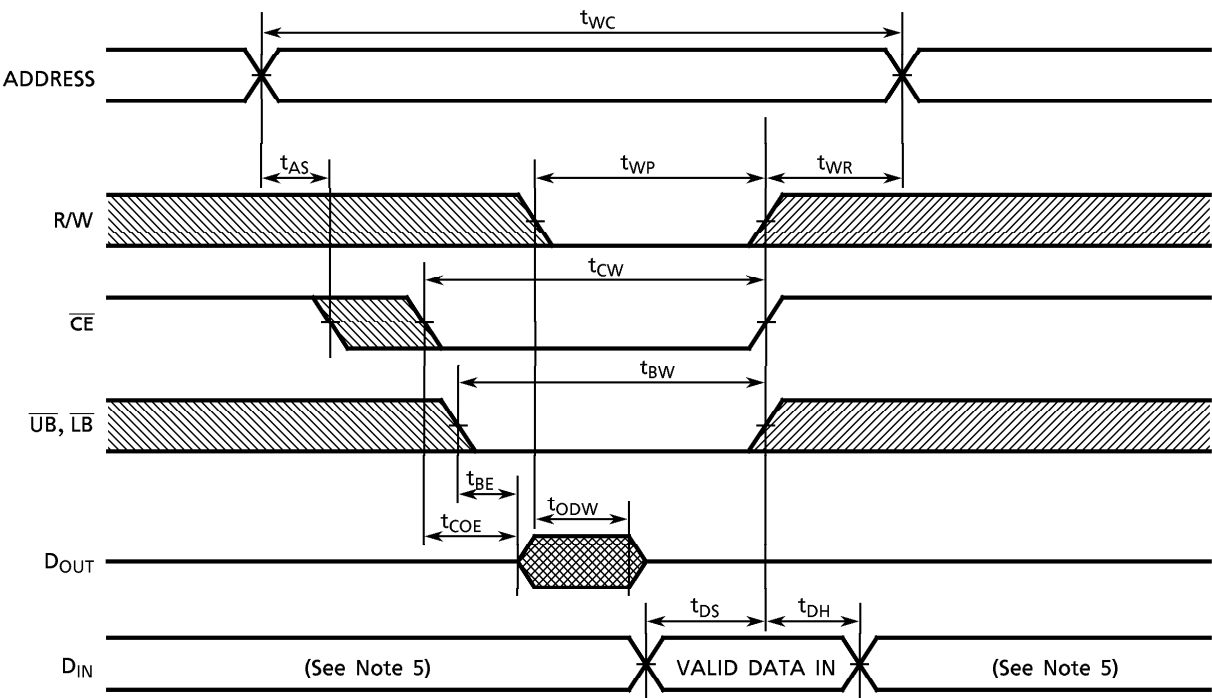
READ CYCLE (See Note 1)



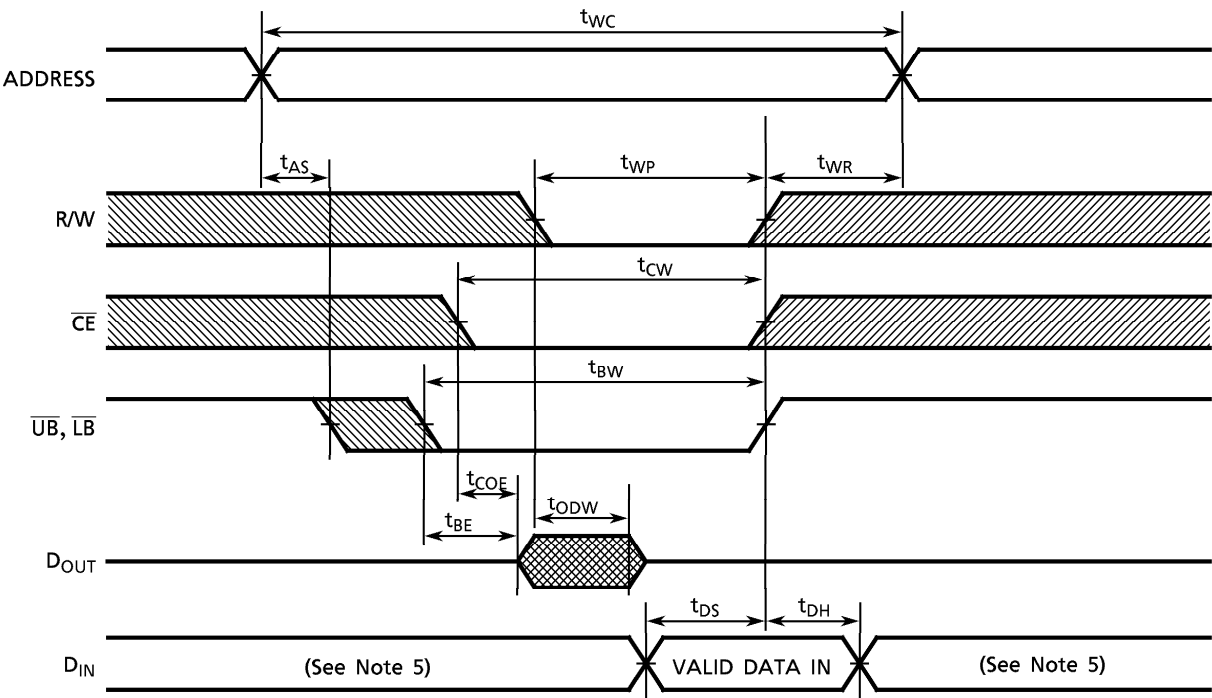
WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 ($\overline{\text{CE}}$ CONTROLLED) (See Note 4)



WRITE CYCLE 3 ($\overline{\text{UB}}, \overline{\text{LB}}$ CONTROLLED) (See Note 4)



Note: (1) R/W remains HIGH for the read cycle.

(2) If $\overline{CE}$ goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If $\overline{CE}$ goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

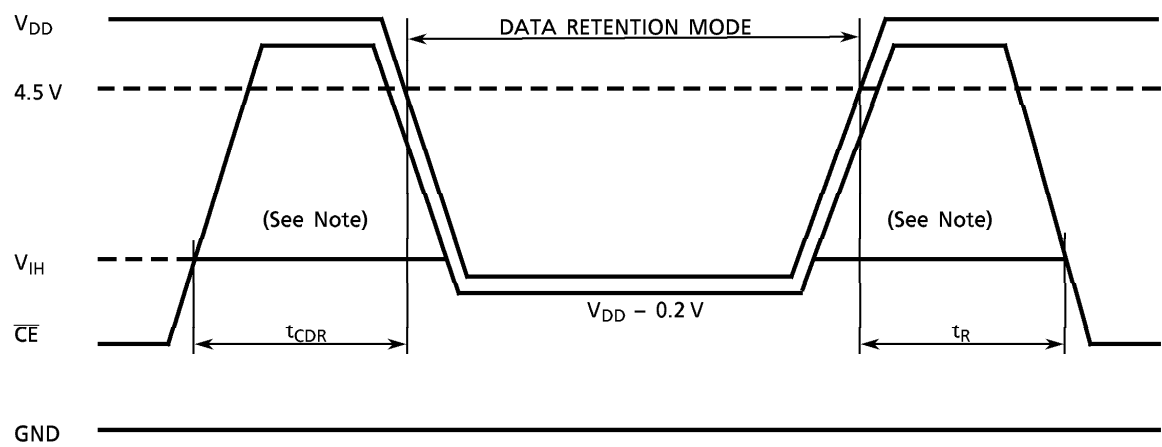
(4) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = - 40° to 85°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I _{DDS2}	Standby Current	V _{DH} = 3.0 V	–	–	100	μA
		V _{DH} = 5.5 V	–	–	200	
t _{CDR}	Chip Deselect to Data Retention Mode Time		0	–	–	nS
t _R	Recovery Time		5	–	–	mS

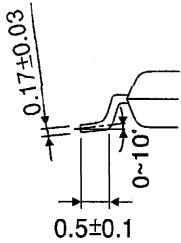
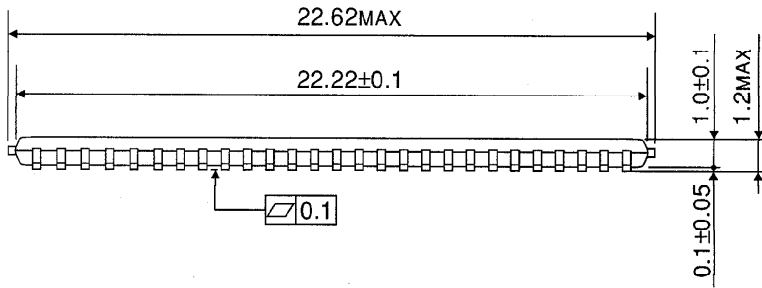
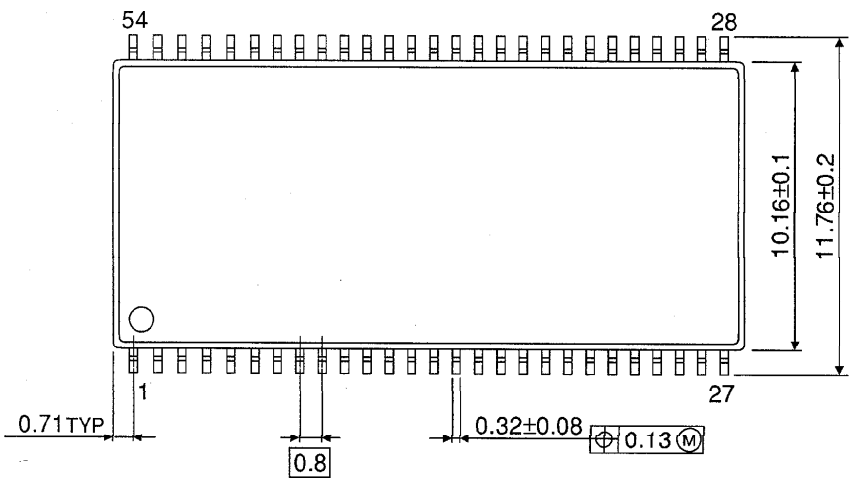
CE CONTROLLED DATA RETENTION MODE



Note: When $\overline{CE}$ is operating at the V_{IH} level (2.4 V), the operating current is given by I_{DDS1} during the transition of V_{DD} from 4.5 to 2.6 V.

PACKAGE DIMENSIONS (TSOPII 54-P-400-0.80)

Units in mm



Weight: 0.55 g (typ)