

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

The TC74AC373 is an advanced high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C²MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

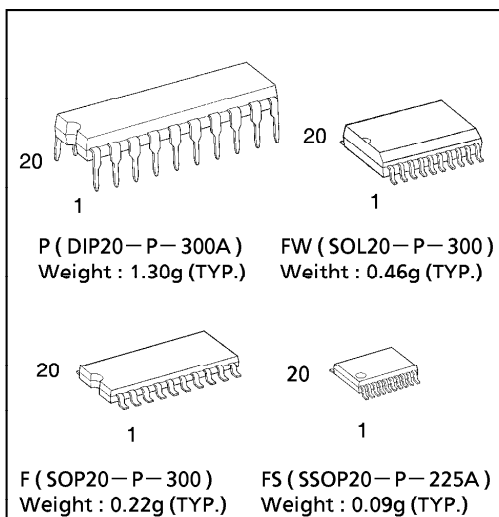
These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

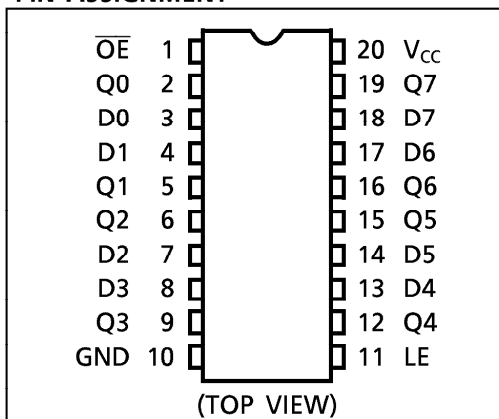
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed..... $t_{pd} = 4.8\text{ns}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 8\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}(\text{Min.})$
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 24\text{mA}(\text{Min.})$
 Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range.... $V_{CC}(\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Pin and Function Compatible with 74F373



PIN ASSIGNMENT



TRUTH TABLE

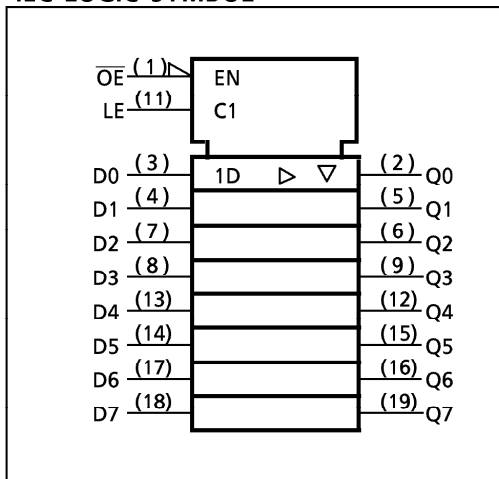
INPUTS			OUTPUTS
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

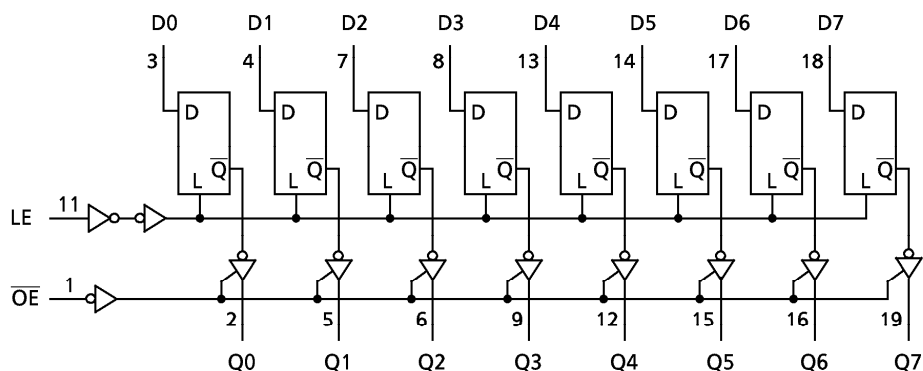
X : Don't Care

Z : High Impedance

Q_n : Q outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL





PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V _{CC}	−0.5~7.0	V
DC Input Voltage	V _{IN}	−0.5~V _{CC} +0.5	V
DC Output Voltage	V _{OUT}	−0.5~V _{CC} +0.5	V
Input Diode Current	I _{IK}	±20	mA
Output Diode Current	I _{OK}	±50	mA
DC Output Current	I _{OUT}	±50	mA
DC V _{CC} /Ground Current	I _{CC}	±200	mA
Power Dissipation	P _D	500 (DIP)* / 180 (SOP/SSOP)	mW
Storage Temperature	T _{stg}	−65~150	°C

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V _{CC}	2.0~5.5	V
Input Voltage	V _I N	0~V _{CC}	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{opr}	− 40~85	°C
Input Rise and Fall Time	dt / dV	0~ 100 (V _{CC} = 3.3 ± 0.3V) 0~ 20 (V _{CC} = 5 ± 0.5V)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}			2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V
Low - Level Input Voltage	V _{IL}			2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I _{OH} = -4mA	3.0	2.58	—	—	2.48	—	
			I _{OH} = -24mA	4.5	3.94	—	—	3.80	—	
			I _{OH} = -75mA*	5.5	—	—	—	3.85	—	
			I _{OL} = 50μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I _{OL} = 12mA	3.0	—	—	—	—	0.44	
			I _{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I _{OL} = 75mA*	5.5	—	—	—	—	1.65	
3 - State Output Off - State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	± 0.5	—	± 5.0	μA
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND		5.5	—	—	± 0.1	—	± 1.0	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	8.0	—	80.0	

* : This spec indicates the capability of driving 50Ω transmission lines.

One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C	Ta = -40~85°C	UNIT
			V _{CC} (V)	LIMIT	LIMIT	
Minimum Pulse Width (LE)	t _W (H)		3.3 ± 0.3 5.0 ± 0.5	7.0 5.0	7.0 5.0	ns
Minimum Set - up Time	t _s		3.3 ± 0.3 5.0 ± 0.5	6.0 3.5	6.0 3.5	
Minimum Hold Time	t _h		3.3 ± 0.3 5.0 ± 0.5	1.0 1.0	1.0 1.0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\Omega$, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.
Propagation Delay Time (LE—Q)	t_{pLH} t_{pHL}		3.3 ± 0.3	—	7.7	13.2	1.0	15.0
			5.0 ± 0.5	—	6.1	8.7	1.0	10.0
Propagation Delay Time (D—Q)	t_{pLH} t_{pHL}		3.3 ± 0.3	—	7.6	12.9	1.0	14.7
			5.0 ± 0.5	—	5.8	8.3	1.0	9.5
Output Enable Time	t_{pZL} t_{pZH}		3.3 ± 0.3	—	7.6	12.9	1.0	14.7
			5.0 ± 0.5	—	6.1	8.7	1.0	10.0
Output Disable Time	t_{pLZ} t_{pHZ}		3.3 ± 0.3	—	7.0	11.0	1.0	12.5
			5.0 ± 0.5	—	5.4	7.5	1.0	8.5
Input Capacitance	C _{IN}			—	5	10	—	10
Output Capacitance	C _{OUT}			—	10	—	—	—
Power Dissipation Capacitance	C _{PD} (1)			—	38	—	—	—

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

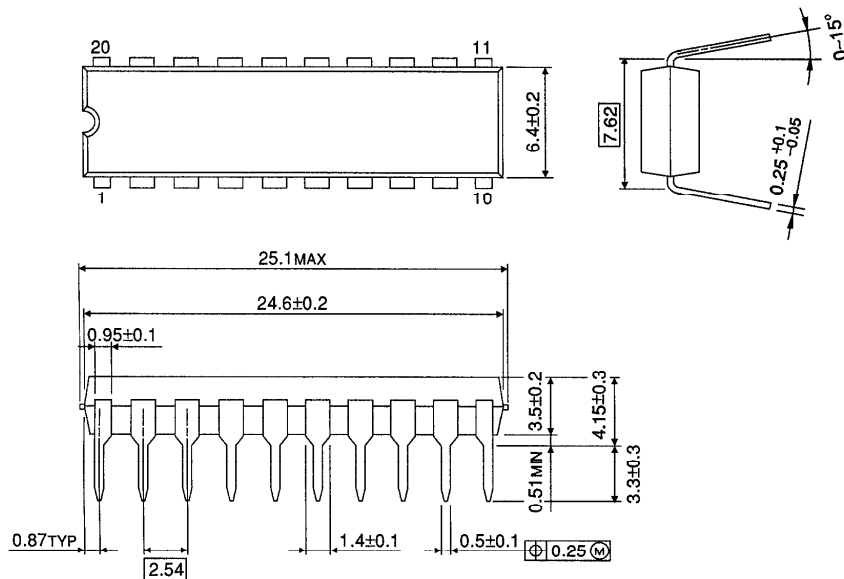
$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} \cdot I_{CC} / 8(\text{per Latch})$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation :

$$C_{PD}(\text{total}) = 26 + 12 \cdot n$$

DIP 20PIN OUTLINE DRAWING (DIP20—P—300A)

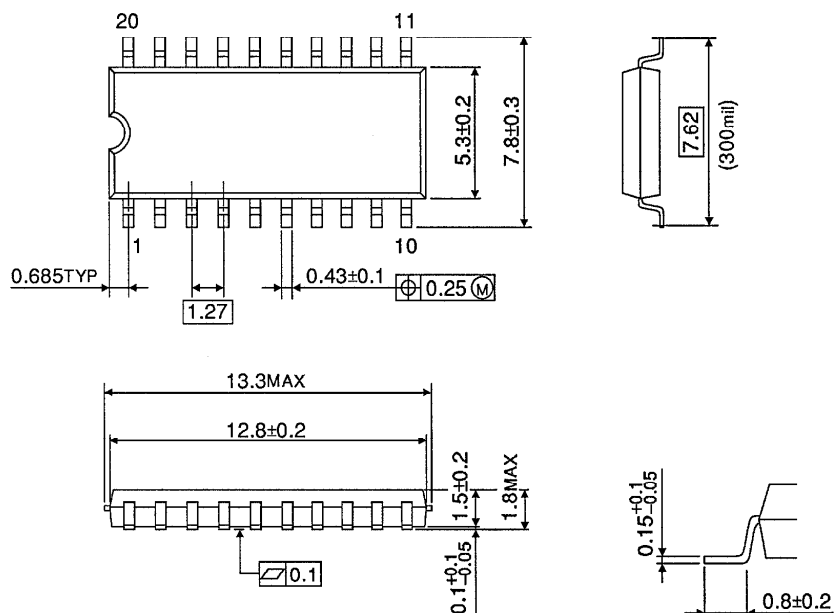
Unit in mm



Weight : 1.30g (TYP.)

SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20—P—300)

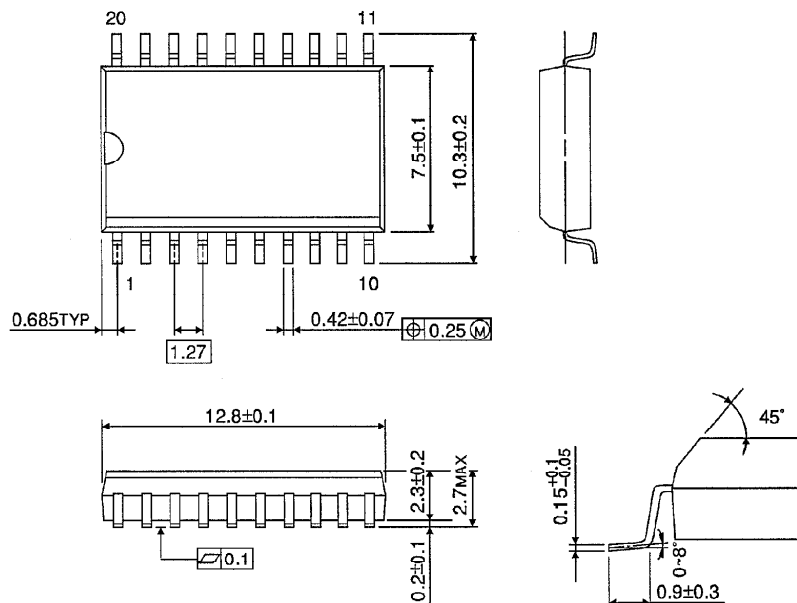
Unit in mm



Weight : 0.22g (TYP.)

SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300)

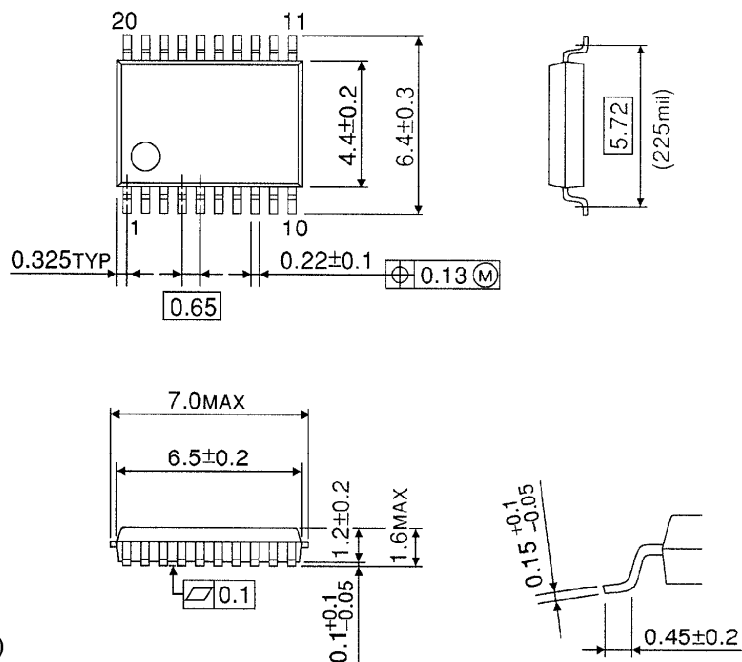
Unit in mm



Weight : 0.46g (TYP.)

SSOP 20PIN OUTLINE DRAWING (SSOP20-P-225A)

Unit in mm



Weight : 0.09g (TYP.)