

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288-WORD BY 8-BIT STATIC RAM

DESCRIPTION

The TC55V4000ST is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.3 to 3.6 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 70 ns. It is automatically placed in low-power mode at 0.5 μ A standby current ($V_{DD}=3V$, $T_a=25^{\circ}C$) when chip enable (\overline{CE}) is asserted high. There are two control inputs. \overline{CE} is used to select the device and for data retention control, and output enable (\overline{OE}) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. The TC55V4000ST is available in a normal pinout plastic 32-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
Operating: 10.8 mW/MHz (typical)
- Single power supply voltage of 2.3 to 3.6 V
- Power down features using \overline{CE}
- Data retention supply voltage of 1.5 to 3.6 V
- Direct TTL compatibility for all inputs and outputs
- Standby current (maximum)

3.6V	7 μ A
3.0V	5 μ A

- Access Times (maximum):

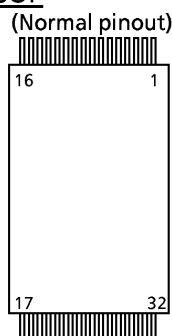
	TC55V4000ST	
	-70	-85
Access Time	70ns	85ns
\overline{CE} Access Time	70ns	85ns
\overline{OE} Access Time	35ns	45ns

- Packages:

TSOP I 32-P-0.50 (Weight: 0.24g typ)

PIN ASSIGNMENT (TOP VIEW)

○ 32 PIN TSOP

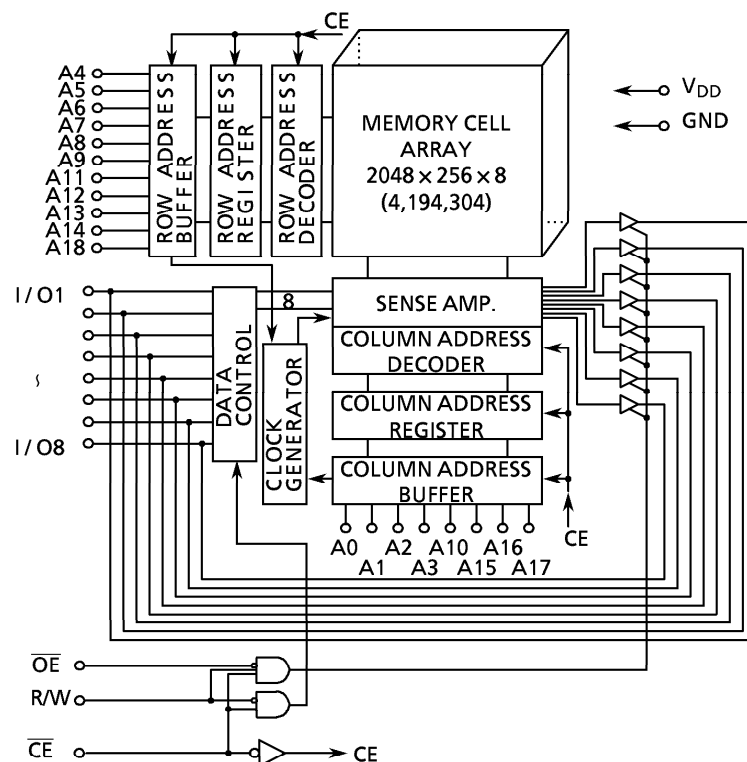
**PIN NAMES**

A0 to A18	Address Inputs	PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
R/W	Read / Write Control Input	PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	A ₁₇	A ₁₅	V _{DD}	A ₁₈	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
\overline{OE}	Output Enable Input	PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
\overline{CE}	Chip Enable Input	PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀	\overline{OE}
I/O1 to I/O8	Data Input / Output																	
V _{DD}	Power																	
GND	Ground																	

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BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{\text{CE}}$	$\overline{\text{OE}}$	R/W	I/O1 to I/O8	POWER
Read	L	L	H	D _{OUT}	I _{DDO}
Write	L	x	L	D _{IN}	I _{DDO}
Outputs Disabled	L	H	H	High-Z	I _{DDO}
Standby	H	x	x	High-Z	I _{DDs}

Note: x = don't care. H = logic high. L = logic low.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	– 0.3 to 4.6	V
V _{IN}	Input Voltage	– 0.3* to 4.6	V
V _{I/O}	Input/Output Voltage	– 0.5 to V _{DD} + 0.5	V
P _D	Power Dissipation	0.6	W
T _{solder}	Soldering Temperature (10 s)	260	°C
T _{strg.}	Storage Temperature	– 55 to 150	°C
T _{opr.}	Operating Temperature	– 40 to 85	°C

* – 3.0 V when measured at a pulse width of 50 ns.

DC RECOMMENDED OPERATING CONDITIONS ($T_a = -40^\circ\text{ to }85^\circ\text{C}$)

SYMBOL	PARAMETER	2.3 to 3.6V			UNIT
		MIN	TYP	MAX	
V_{DD}	Power Supply Voltage	2.3	3.0	3.6	V
V_{IH}	Input High Voltage	2.2	–	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3^*	–	$V_{DD} \times 0.22$	V
V_{DH}	Data Retention Supply Voltage	1.5	–	3.6	V

* – 3.0 V when measured at a pulse width of 50 ns.

DC CHARACTERISTICS ($T_a = -40^\circ\text{ to }85^\circ\text{C}$, $V_{DD} = 2.3\text{ to }3.6\text{ V}$)

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DD}				–	–	± 1.0	μA
I _{OH}	Output High Current	V _{OH} = V _{DD} – 0.5 V				– 0.5	–	–	mA
I _{OL}	Output Low Current	V _{OL} = 0.4 V				2.1	–	–	mA
I _{LO}	Output Leakage Current	CE = V _{IH} or R/W = V _{IL} or OE = V _{IH} , V _{OUT} = 0 V to V _{DD}				–	–	± 1.0	μA
I _{DDO1}	Operating Current	CE = V _{IL} and R/W = V _{IH} , I _{OUT} = 0 mA Other Input = V _{IH} /V _{IL}	V _{DD} = 3.0V ± 10%	T _{cycle}	min	–	–	50	mA
					1 μs	–	–	10	
I _{DDO2}		CE = 0.2 V R/W = V _{DD} – 0.2 V, I _{OUT} = 0 mA Other Inputs = V _{DD} – 0.2 V/0.2 V			min	–	–	45	
					1 μs	–	–	5	
I _{DDS1}	Standby Current	CE = V _{IH}				–	–	2	mA
I _{DDS2}		CE = V _{DD} – 0.2 V V _{DD} = 1.5 to 3.6 V	V _{DD} = 3.0V ± 10%	Ta = 25°C		–	–	0.6	μA
				Ta = – 40~85°C		–	–	6	
			V _{DD} = 3.3V ± 0.3V	Ta = 25°C		–	–	0.7	
				Ta = – 40~85°C		–	–	7	
			V _{DD} = 3.0V	Ta = 25°C		–	0.05	0.5	
				Ta = – 40~40°C		–	–	1	
			Ta = – 40~85°C		–	–	5		

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 2.7$ to 3.6 V)READ CYCLE

SYMBOL	PARAMETER	TC55V4000ST				UNIT
		-70		-85		
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	70	–	85	–	ns
t _{ACC}	Address Access Time	–	70	–	85	
t _{CO}	Chip Enable Access Time	–	70	–	85	
t _{OE}	Output Enable Access Time	–	35	–	45	
t _{COE}	Chip Enable Low to Output Active	5	–	5	–	
t _{OEE}	Output Enable Low to Output Active	0	–	0	–	
t _{OD}	Chip Enable High to Output High-Z	–	30	–	35	
t _{ODO}	Output Enable High to Output High-Z	–	30	–	35	
t _{OH}	Output Data Hold Time	10	–	10	–	

WRITE CYCLE

SYMBOL	PARAMETER	TC55V4000ST				UNIT
		-70		-85		
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	70	–	85	–	ns
t _{WP}	Write Pulse Width	50	–	55	–	
t _{CW}	Chip Enable to End of Write	60	–	70	–	
t _{AS}	Address Setup Time	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	
t _{ODW}	R/W Low to Output High-Z	–	25	–	35	
t _{OEW}	R/W High to Output Active	0	–	0	–	
t _{DS}	Data Setup Time	30	–	35	–	
t _{DH}	Data Hold Time	0	–	0	–	

AC TEST CONDITIONS

Output load: 30 pF + 1TTL Gate

Input pulse level: 0.4 V, 2.4 V

Timing measurements: $V_{DD} \times 0.5$ Reference level: $V_{DD} \times 0.5$ t_R, t_F : 5 ns

AC CHARACTERISTICS AND OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 2.3$ to 3.6 V)READ CYCLE

SYMBOL	PARAMETER	TC55V4000ST				UNIT
		-70		-85		
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	85	–	100	–	ns
t _{ACC}	Address Access Time	–	85	–	100	
t _{CO}	Chip Enable Access Time	–	85	–	100	
t _{OE}	Output Enable Access Time	–	45	–	50	
t _{COE}	Chip Enable Low to Output Active	5	–	5	–	
t _{OEE}	Output Enable Low to Output Active	0	–	0	–	
t _{OD}	Chip Enable High to Output High-Z	–	35	–	40	
t _{ODO}	Output Enable High to Output High-Z	–	35	–	40	
t _{OH}	Output Data Hold Time	10	–	10	–	

WRITE CYCLE

SYMBOL	PARAMETER	TC55V4000ST				UNIT
		-70		-85		
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	85	–	100	–	ns
t _{WP}	Write Pulse Width	55	–	60	–	
t _{CW}	Chip Enable to End of Write	70	–	80	–	
t _{AS}	Address Setup Time	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	
t _{ODW}	R/W Low to Output High-Z	–	35	–	40	
t _{OEW}	R/W High to Output Active	0	–	0	–	
t _{DS}	Data Setup Time	40	–	40	–	
t _{DH}	Data Hold Time	0	–	0	–	

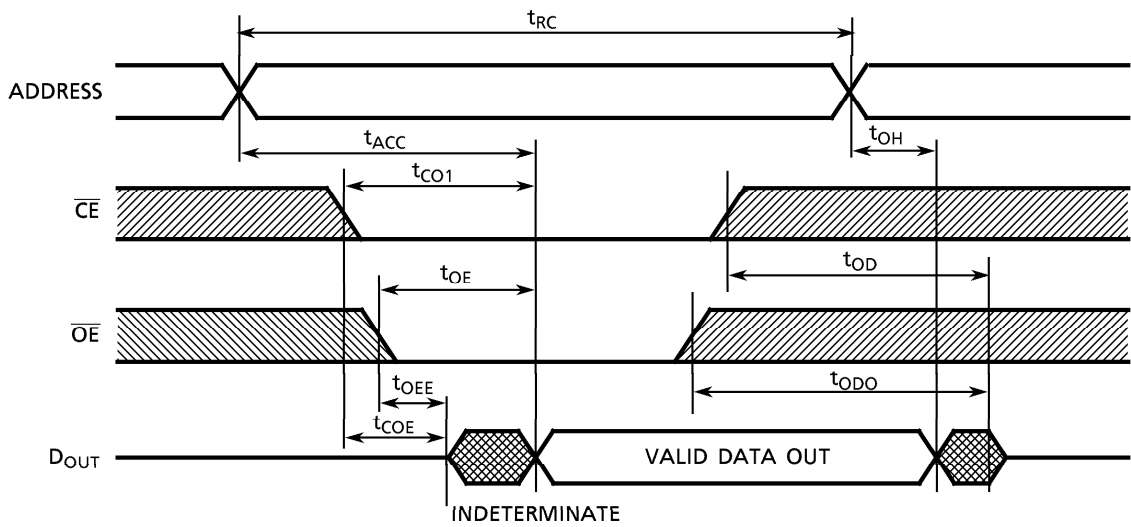
AC TEST CONDITIONS

Output load: 30 pF + 1TTL Gate

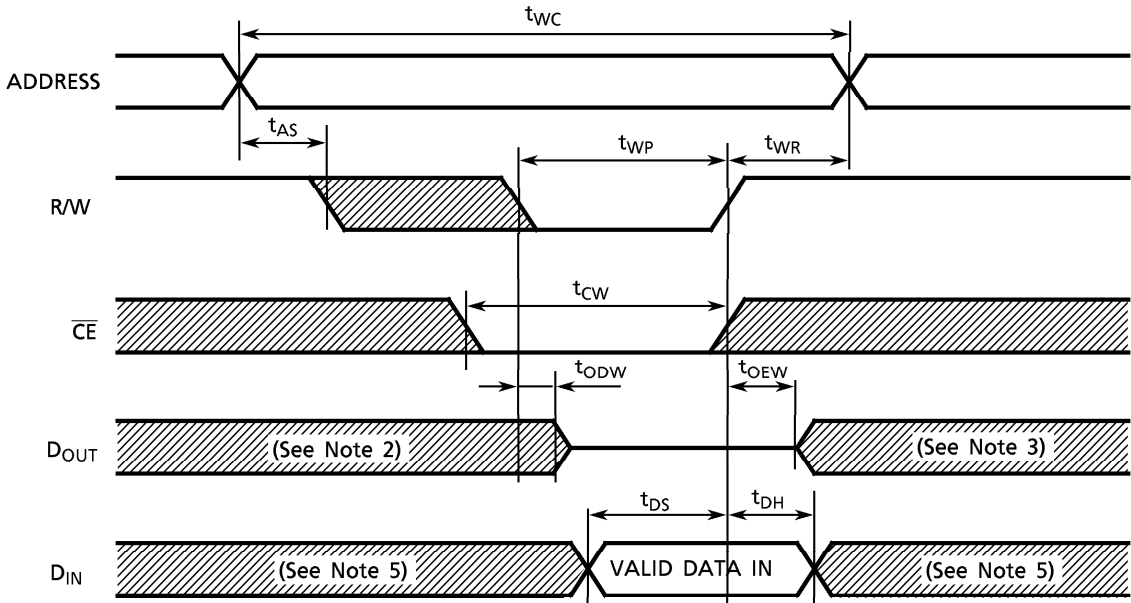
Input pulse level: $V_{DD} - 0.2\text{ V}$, 0.2VTiming measurements: $V_{DD} \times 0.5$ Reference level: $V_{DD} \times 0.5$ t_R, t_F : 5 ns

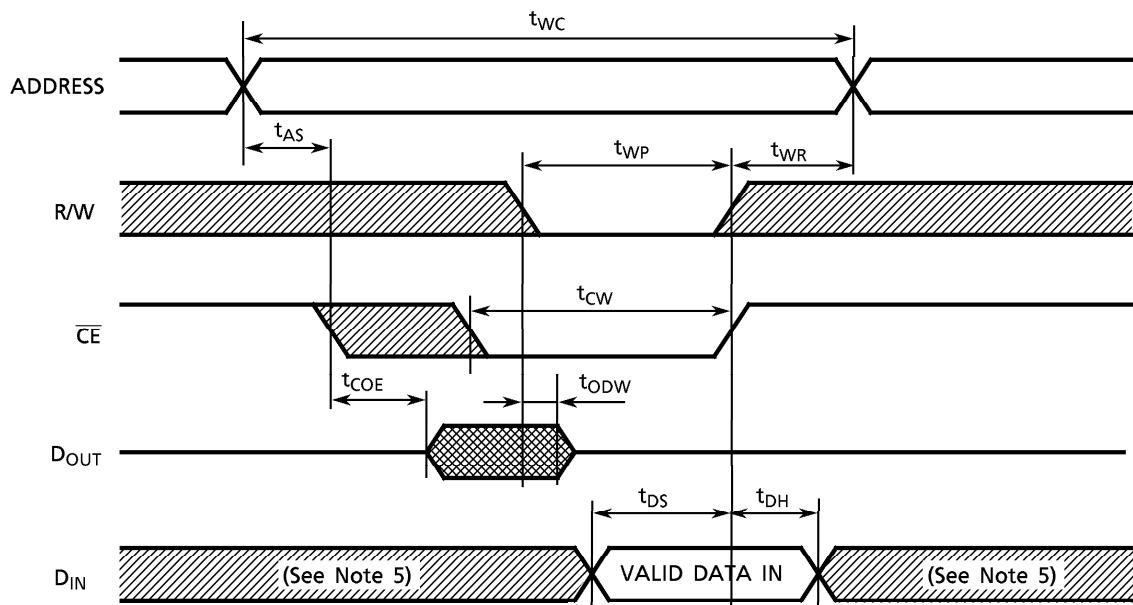
TIMING DIAGRAMS

READ CYCLE (See Note 1)



WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 ($\overline{\text{CE}}$ CONTROLLED) (See Note 4)

Note: (1) R/W remains HIGH for the read cycle.

(2) If $\overline{\text{CE}}$ goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If $\overline{\text{CE}}$ goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

(4) If $\overline{\text{OE}}$ is HIGH during the write cycle, the outputs will remain at high impedance.

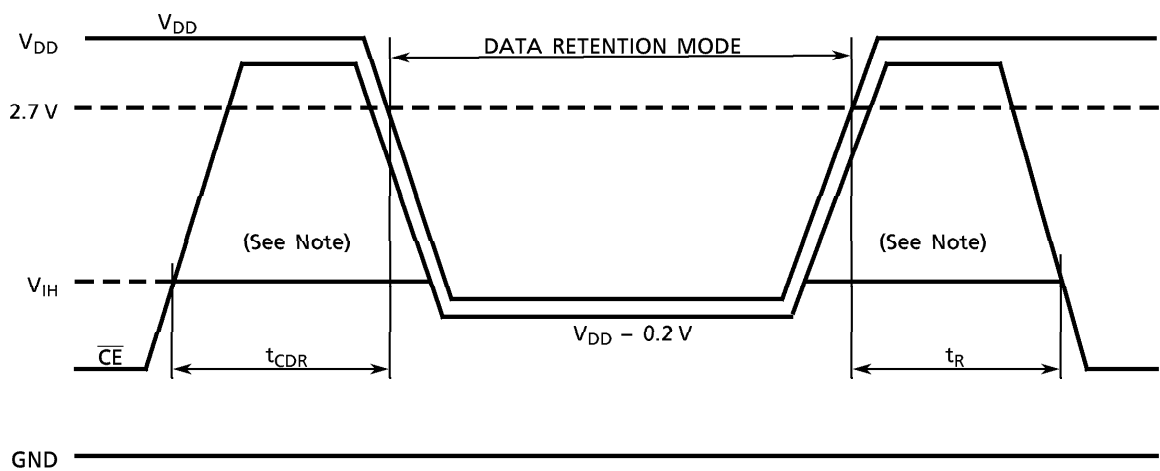
(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = - 40° to 85°C)

SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
V _{DH}	Data Retention Supply Voltage			1.5	–	3.6	V
I _{DDS2}	Standby Current	V _{DH} = 3.0V	Ta = - 40 to 40°C	–	–	1	μA
			Ta = - 40 to 85°C	–	–	5	
		V _{DH} = 3.6V	Ta = - 40 to 85°C	–	–	7	
t _{CDR}	Chip Deselect to Data Retention Mode Time			0	–	–	nS
t _R	Recovery Time			t _{RC} (1)	–	–	nS

Note: (1) Read cycle time

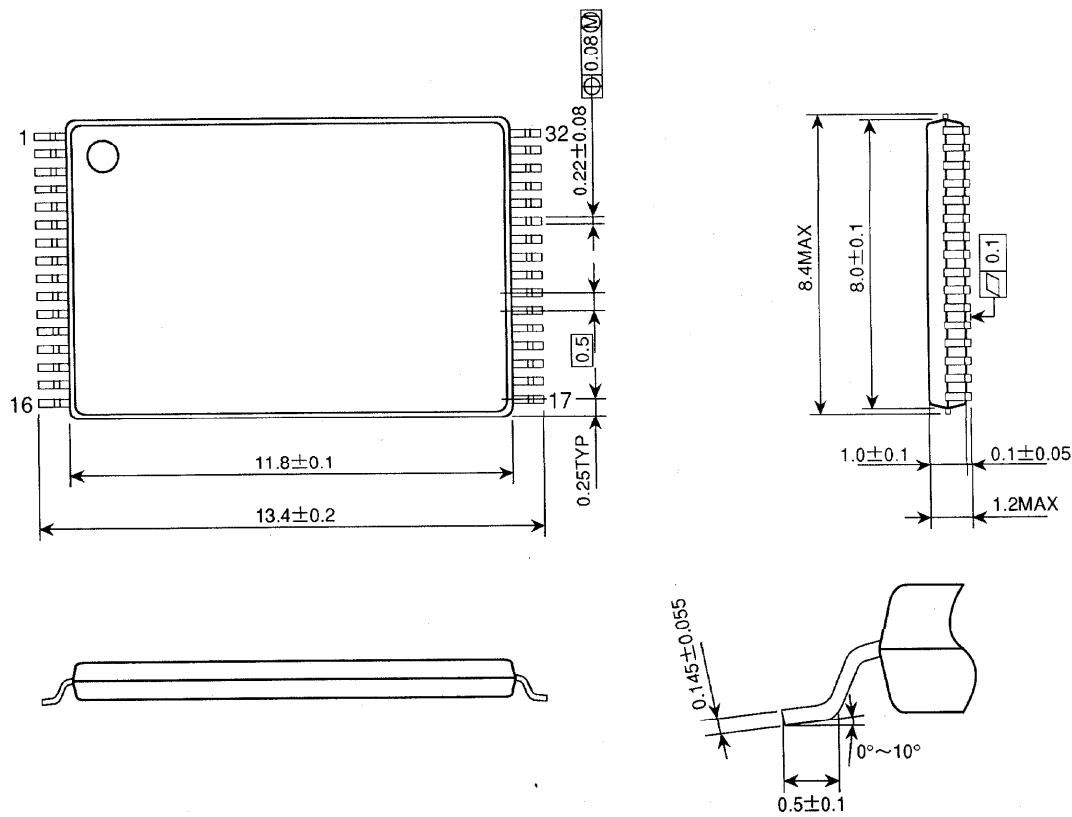
CE CONTROLLED DATA RETENTION MODE



Note: When \overline{CE} is operating at the V_{IH} level (2.2 V), the operating current is given by I_{DDS1} during the transition of V_{DD} from 3.6 to 2.4 V.

PACKAGE DIMENSIONS (TSOP I 32-P-0.50)

Units in mm



Weight: 0.24 g (typ)