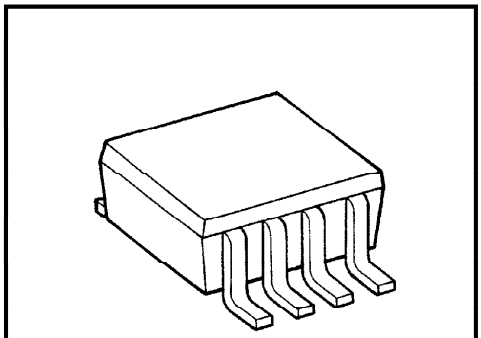
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7WH74FU

D-TYPE FLIP FLOP WITH PRESET AND CLEAR

The TC7WH74FU is an advanced high speed CMOS D-FLIP FLOP fabricated with silicon gate CMOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.
CLR and PR are independent of the CK and are accomplished by setting the appropriate input low.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V system and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.



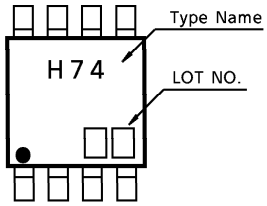
SSOP8-P-0.65

Weight : 0.02g (Typ.)

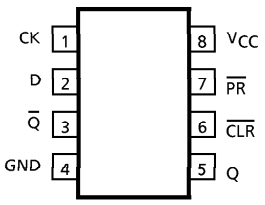
FEATURES

- High Speed ····· f_{MAX} = 170MHz (Typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 2μA (Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operation Voltage Range ··· V_{CC} (opr) = 2~5.5V

MARKING



PIN ASSIGNMENT (TOP VIEW)

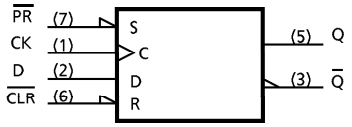


MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} / Ground Current	I_{CC}	±25	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature (10 s)	T_L	260	°C

961001EBA2

LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	×	×	L	H	CLEAR
H	L	×	×	H	L	PRESET
L	L	×	×	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	×	↓	Q_n	$\overline{Q}_n$	NO CHANGE

× : Don't care

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100 (V_{CC} = 3.3 ± 0.3V)	ns
		0~20 (V_{CC} = 5 ± 0.5V)	

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}	—		2.0	1.5	—	—	1.5	—	V
				3.0~5.5	V_{CC} ×0.7	—	—	V_{CC} ×0.7	—	
Low-Level Input Voltage	V_{IL}	—		2.0	—	—	0.5	—	0.5	V
				3.0~5.5	—	—	V_{CC} ×0.3	—	V_{CC} ×0.3	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −8mA	4.5	3.94	—	—	3.80	—	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 4mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 8mA	4.5	—	—	0.36	—	0.44	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	2.0	—	20.0	μA

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYP.	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width (CLOCK)	t_W (L) t_W (H)		3.3 ± 0.3	—	6.0	7.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	t_W (L)		3.3 ± 0.3	—	6.0	7.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum Set-up Time	t_s		3.3 ± 0.3	—	7.0	7.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum Hold Time	t_h		3.3 ± 0.3	—	0.5	0.5	ns
			5.0 ± 0.5	—	0.5	0.5	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	3.0	3.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

CHARACTERISTIC	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK-Q, $\overline{Q}$)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	—	6.7	11.9	1.0	14.0	ns
				50	—	9.2	15.4	1.0	17.5	
			5.0 ± 0.5	15	—	4.6	7.3	1.0	8.5	
				50	—	6.1	9.3	1.0	10.5	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	—	7.6	12.3	1.0	14.5	ns
				50	—	10.1	15.8	1.0	18.0	
			5.0 ± 0.5	15	—	4.8	7.7	1.0	9.0	
				50	—	6.3	9.7	1.0	11.0	
Maximum Clock Frequency	f_{MAX}		3.3 ± 0.3	15	80	125	—	70	—	MHz
				50	50	75	—	45	—	
			5.0 ± 0.5	15	130	170	—	110	—	
				50	90	115	—	75	—	
Input Capacitance	C_{IN}				—	4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)			—	22	—	—	—	pF

(Note 1) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

$$I_{CC\,(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$