

TC74HCT74AP, TC74HCT74AF, TC74HCT74AFN**DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR**

The TC74HCT74A is a high speed CMOS D FLIP FLOP fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CLOCK pulse.

CLEAR and PRESET are independent of the CLOCK and are accomplished by setting the appropriate input to an "L" level. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

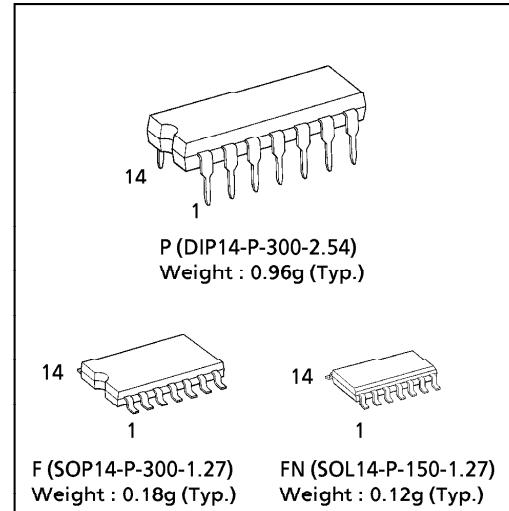
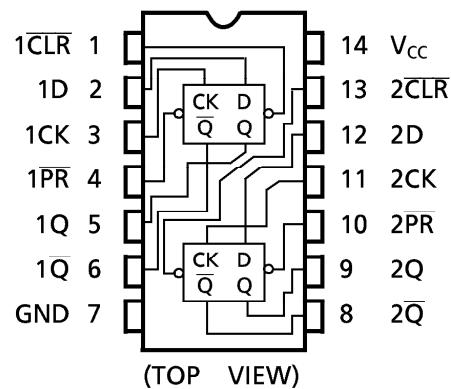
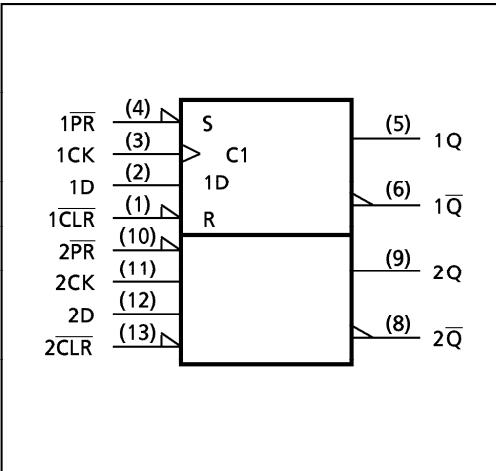
- High Speed..... $f_{MAX} = 53\text{MHz}$ (typ.) at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 2\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs.... $V_{IH} = 2\text{V}$ (Min.) $V_{IL} = 0.8\text{V}$ (Max.)
- Wide Interfacing ability.....LSTTL, NMOS, CMOS
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..... $|I_{OH}| = |I_{OL}| = 4\text{mA}$ (Min.)
- Balanced Propagation Delays..... $t_{PLH} \approx t_{PHL}$
- Pin and Function Compatible with 74LS74

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
CLR	\overline{PR}	D	CK	Q	\overline{Q}	
L	H	X	X	L	H	CLR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	—	L	H	—
H	H	H	—	H	L	—
H	H	X	—	Q_n	\overline{Q}_n	NO CHANGE

X : Don't Care

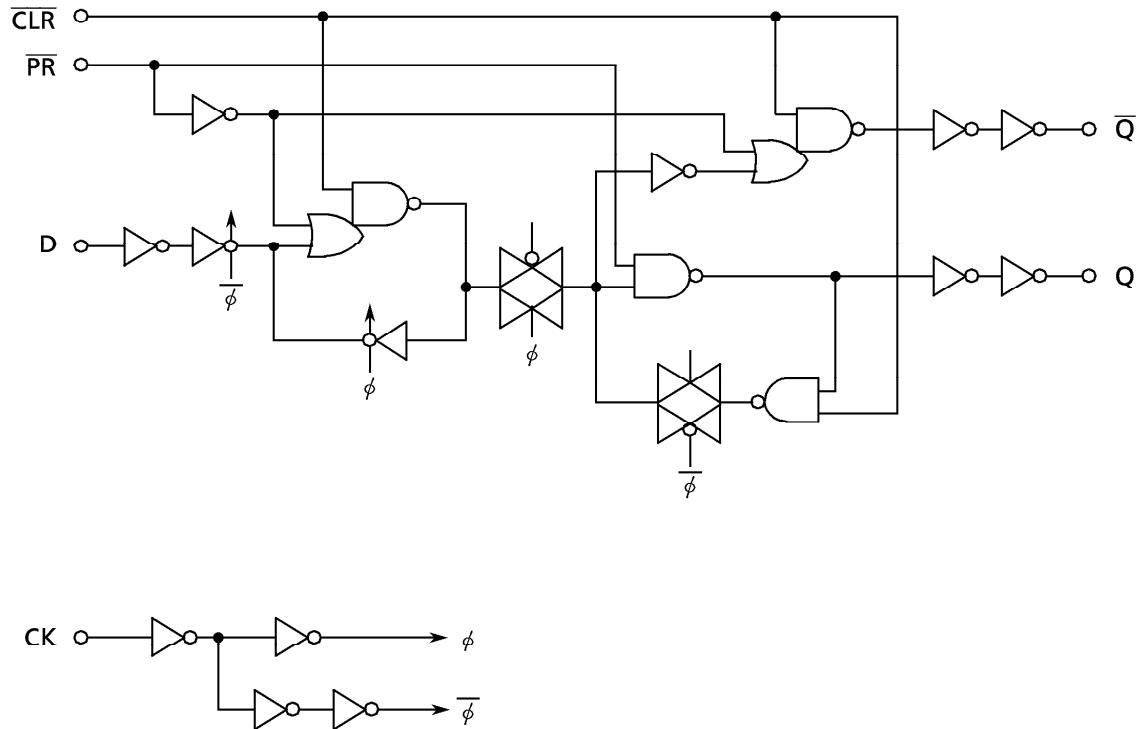
(Note) The JEDEC SOP (FN) is not available in Japan.

**PIN ASSIGNMENT****IEC LOGIC SYMBOL**

961001EBA2

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SYSTEM DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V _{CC}	-0.5~7	V
DC Input Voltage	V _{IN}	-0.5~V _{CC} +0.5	V
DC Output Voltage	V _{OUT}	-0.5~V _{CC} +0.5	V
Input Diode Current	I _{IK}	±20	mA
Output Diode Current	I _{OK}	±20	mA
DC Output Current	I _{OUT}	±25	mA
DC V _{CC} / Ground Current	I _{CC}	±50	mA
Power Dissipation	P _D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T _{STG}	-65~150	°C

*500mW in the range of Ta = -40°C~65°C. From Ta = 65°C to 85 °C a derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V _{CC}	4.5~5.5	V
Input Voltage	V _{IN}	0~V _{CC}	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{OPR}	-40~85	°C
Input Rise and Fall Time	t _r , t _f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}		4.5 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V _{IL}		4.5 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	4.5	4.4	4.5	—	4.4	V
			I _{OH} = -4 mA	4.5	4.18	4.31	—	4.13	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	4.5	—	0.0	0.1	—	V
			I _{OL} = 4 mA	4.5	—	0.17	0.26	—	
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND	5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	2.0	—	20.0	
	I _C	PER INPUT: V _{IN} = 0.5V or 2.4V OTHER INPUT: V _{CC} or GND	5.5	—	—	2.0	—	2.9	mA

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(\text{V})$	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$		4.5	—	15	19	ns
	$t_{W(H)}$		5.5	—	14	16	
Minimum Pulse Width (CLR , PR)	$t_{W(L)}$		4.5	—	15	19	
			5.5	—	14	17	
Minimum Set-up Time	t_s		4.5	—	15	19	
			5.5	—	14	17	
Minimum Hold Time	t_h		4.5	—	0	0	
			5.5	—	0	0	
Minimum Removal Time (CLR , PR)	t_{rem}		4.5	—	5	5	
			5.5	—	5	5	
Clock Frequency	f		4.5	—	27	22	MHz
			5.5	—	30	24	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, Ta = 25°C, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(\text{V})$	MIN.	TYP.	MAX.	UNIT
				MIN.	TYP.	MAX.	
Output Transition Time	t_{TLH}			—	6	12	ns
	t_{THL}			—	—	—	
Propagation Delay Time (CK-Q , Q)	t_{PLH}			—	17	28	
	t_{PHL}			—	—	—	
Propagation Delay Time (CLR , PR-Q , Q)	t_{PLH}			—	15	25	
	t_{PHL}			—	—	—	
Maximum Clock Frequency	f_{MAX}			29	53	—	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(\text{V})$	Ta = 25°C		Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	
Output Transition Time	t_{TLH}			4.5	—	8	15	ns
	t_{THL}			5.5	—	7	13	
Propagation Delay Time (CK-Q , Q)	t_{PLH}			4.5	—	21	33	
	t_{PHL}			5.5	—	19	30	
Propagation Delay Time (CLR , PR-Q , Q)	t_{PLH}			4.5	—	18	30	
	t_{PHL}			5.5	—	15	27	
Maximum Clock Frequency	f_{MAX}			4.5	27	48	—	MHz
				5.5	30	53	—	
Input Capacitance	C_{IN}			—	5	10	—	10
Power Dissipation Capacitance	C_{PD}	(1)		—	32	—	—	pF

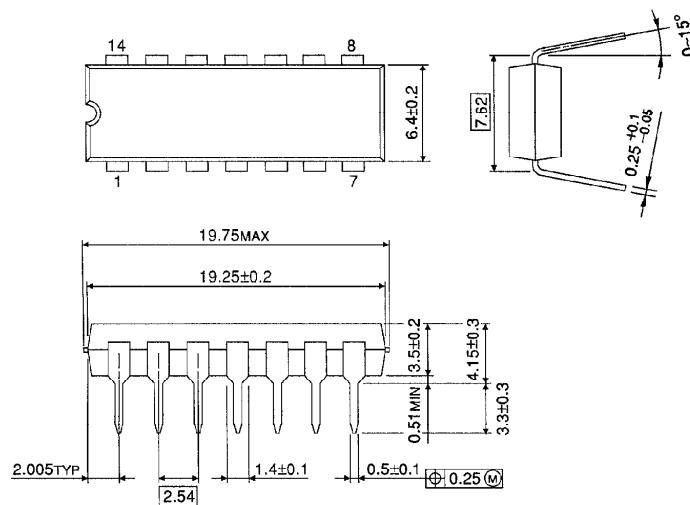
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54)

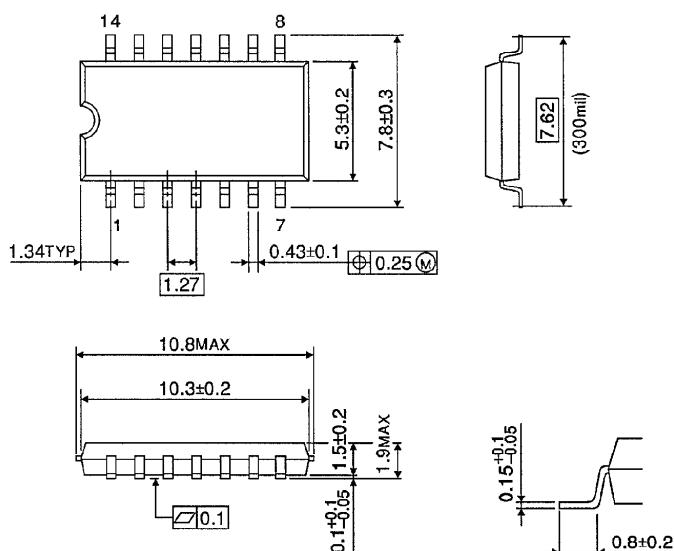
Unit in mm



Weight : 0.96g (Typ.)

SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27)

Unit in mm

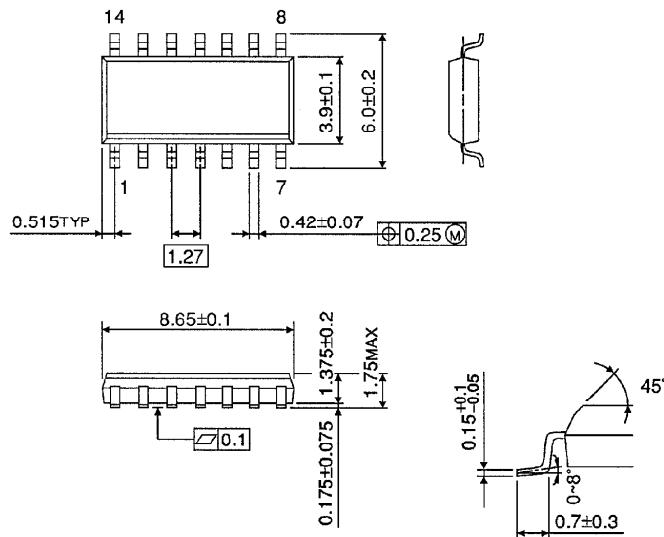


Weight : 0.18g (Typ.)

SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)