TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7MH175FK

Quad D-Type Flip-Flop with Clear

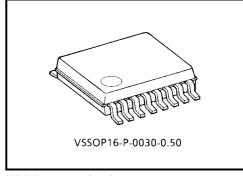
The TC7MH175FK is an advanced high speed CMOS quad D-type flip-flop fabricated with silicon gate $\rm C^2MOS$ technology.

It achieves the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

These four flip-flops are controlled by a clock input (CK) and a clear input (\overline{CLR}).

The information data applied to the D inputs (D1 thru D4) are transferred to the outputs (Q1 thru Q4 and $\overline{Q}1$ thru $\overline{Q}4$) on the positive-going edge of the clock pulse.

When the \overline{CLR} input is held low, the Q outputs are at the low logic level and the \overline{Q} outputs are at the high logic level, regardless of other input conditions.



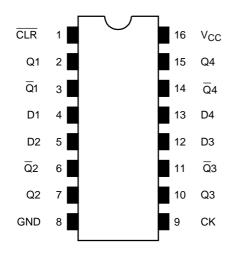
Weight: 0.02 g (typ.)

An input protection circuit ensures that 0 to 7 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

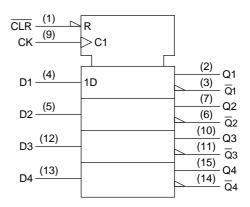
Features

- High speed: $f_{max} = 210 \text{ MHz (typ.) (VCC} = 5 \text{ V)}$
- Low power dissipation: $I_{CC} = 4 \mu A \text{ (max) (Ta} = 25 ^{\circ}\text{C)}$
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_pLH \approx t_pHL$
- Wide operating voltage range: $V_{CC (opr)} = 2 \sim 5.5 \text{ V}$
- Low noise: VOLP = 0.8 V (max)
- Pin and function compatible with 74ALS175

Pin Assignment (top view)



IEC Logic Symbol

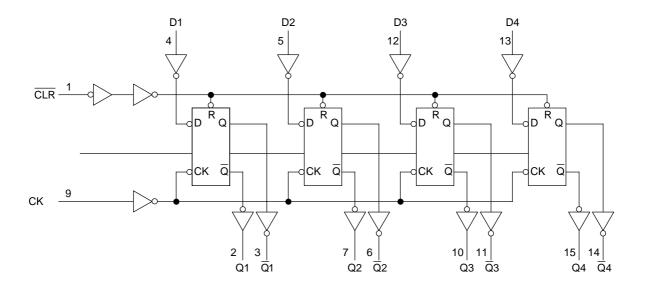


Truth Table

	Inputs			Outputs		
CLR	D	CK	Q	Q	Function	
L	Х	Х	L	Н	Clear	
Н	L	_	L	Н	_	
Н	Н		Н	L	_	
Н	Х		Q _n	\overline{Q}_n	No change	

X: Don't care

System Diagram



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Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	-0.5~7.0	V
DC input voltage	V _{IN}	-0.5~7.0	V
DC output voltage	V _{OUT}	-0.5~V _{CC} + 0.5	٧
Input diode current	I _{IK}	-20	mA
Output diode current	lok	±20	mA
DC output current	Гоит	±25	mA
DC V _{CC} /ground current	Icc	±50	mA
Power dissipation	PD	180	mW
Storage temperature	T _{stg}	-65~150	°C

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	2.0~5.5	V
Input voltage	V _{IN}	0~5.5	V
Output voltage	V _{OUT}	0~V _{CC}	V
Operating temperature	T _{opr}	-40~85	°C
Input rise and fall time	dt/dv	$0 \sim 100 \text{ (V}_{CC} = 3.3 \pm 0.3 \text{ V)}$	ns/V
input nse and rail time	ui/uv	$0 \sim 20 \ (V_{CC} = 5 \pm 0.5 \ V)$	113/ V

Electrical Characteristics

DC Characteristics

Characteristics		Symbol	Symbol Test Condition			Ta = 25°C			Ta = -40~85°C		Unit
		Symbol Test Condition		Condition	V _{CC} (V)	Min	Тур.	Max	Min	Max	Offic
			_		2.0	1.50	_	_	1.50	_	V
	High level	V _{IH}			3.0~5.5	V _{CC} × 0.7	_	_	V _{CC} × 0.7		
Input voltage					2.0			0.50	_	0.50	V
	Low level	V _{IL}	_		3.0~5.5			V _{CC} × 0.3	_	V _{CC} × 0.3	
	High level	V _{ОН}	V _{IN} = V _{IH} or V _{IL}		2.0	1.9	2.0	_	1.9	_	
				$I_{OH} = -50 \mu A$	3.0	2.9	3.0	_	2.9	_	
					4.5	4.4	4.5	_	4.4	_	
				$I_{OH} = -4 \text{ mA}$	3.0	2.58	_	_	2.48		
Output voltage				$I_{OH} = -8 \text{ mA}$	4.5	3.94			3.80		
Output voltage		V _{OL}			2.0		0	0.1		0.1	V
				$I_{OL} = 50 \mu A$	3.0		0	0.1	_	0.1	
	Low level		$V_{IN} = V_{IH}$ or V_{IL}		4.5		0	0.1	_	0.1	
				I _{OL} = 4 mA	3.0	_	_	0.36	_	0.44	
				I _{OL} = 8 mA	4.5	_	_	0.36	_	0.44	
Input leakage current		I _{IN}	V _{IN} = 5.5 V or GND		0~5.5	_	_	±0.1	_	±1.0	μΑ
Quiescent supply	y current	Icc	$V_{IN} = V_{CC}$	or GND	5.5		_	4.0		40.0	μΑ

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Timing Requirements (Input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	vmbol Test Condition -		Ta = 25°C		Ta = -40~85°C	Unit	
Characteristics	Symbol	rest Condition	V _{CC} (V)	Тур.	Limit	Limit	Offic	
Minimum pulse width	t _{w (L)}		3.3 ± 0.3	_	5.0	5.0	ne	
(CK)	t _{w (H)}	_	5.0 ± 0.5	_	5.0	5.0	ns	
Minimum pulse width	t 4.		3.3 ± 0.3	_	5.0	5.0	ns	
(CLR)	t _{w (L)}	_	5.0 ± 0.5	_	5.0	5.0	115	
Minimum set-up time	t _s		3.3 ± 0.3	_	5.0	5.0	ns	
wiiniinam set-up time		_	5.0 ± 0.5	_	4.0	4.0	115	
Minimum hold time	t _h		3.3 ± 0.3	_	1.0	1.0	ns	
Minimum noid time		_	5.0 ± 0.5	_	1.0	1.0	115	
Minimum removal time			3.3 ± 0.3	_	5.0	5.0	nc	
(CLR)	t _{rem}	_	5.0 ± 0.5	_	5.0	5.0	ns	

AC Characteristics (Input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	_		Ta = 25°C			Ta = -40~85°C		- Unit
Characteristics	Symbol	rest Condition	V _{CC} (V)	C _L (pF)	Min	Тур.	Max	Min	Max	Offic
			3.3 ± 0.3	15	_	7.5	11.5	1.0	13.5	ns
Propagation delay time	t _{pLH}		3.3 ± 0.3	50		10.0	15.0	1.0	17.0	
(CK-Q)	tpHL	_	5.0 ± 0.5	15		4.8	7.3	1.0	8.5	113
			3.0 ± 0.5	50		6.3	9.3	1.0	10.5	
			3.3 ± 0.3	15		6.3	10.1	1.0	12.0	
Propagation delay time	t _{pHL}	_	3.3 ± 0.3	50		8.8	13.6	1.0	15.5	ns
(CLR -Q)			5.0 ± 0.5	15		4.3	6.4	1.0	7.5	113
				50		5.8	8.4	1.0	9.5	
	f _{max}	_	3.3 ± 0.3	15	90	140		75	_	
Maximum clock frequency				50	50	75		45		MHz
Maximum clock frequency			5.0 ± 0.5	15	150	210		125		
				50	85	115	_	75	_	
Output to output skew	t _{osLH}	(Note1)	3.3 ± 0.3	50		—	1.5		1.5	ns
Output to output skew	t _{osHL}	(Note1)	5.0 ± 0.5	50		_	1.0		1.0	10
Input capacitance	C _{IN}		_			4	10	_	10	pF
Power dissipation capacitance	C _{PD}			(Note2)	_	44	_	_	_	pF

Note1: Parameter guaranteed by design.

 $t_{OSLH} = |t_{DLHm} - t_{DLHn}|, t_{OSHL} = |t_{DHLm} - t_{DHLn}|$

Note2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 (per bit)$

And the total CPD when n pcs of flip-flop operate can be gained by the following equation:

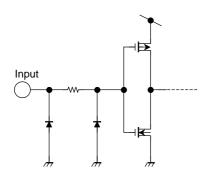
 C_{PD} (total) = 30 + 14 · n

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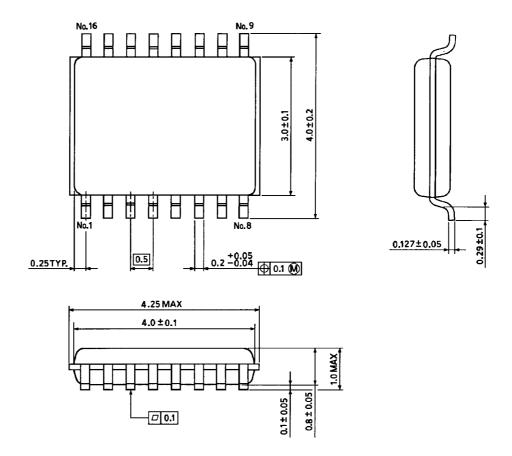
Noise Characteristics (Input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition		Ta = 25°C		Unit
Gilalacteristics	Syllibol	rest condition	V _{CC} (V)	Тур.	Limit	Offic
Quiet output maximum dynamic V _{OL}	V _{OLP}	C _L = 50 pF	5.0	0.4	0.8	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	C _L = 50 pF	5.0	-0.4	-0.8	V
Minimum high level dynamic input voltage V_{IH}	V_{IHD}	C _L = 50 pF	5.0	_	3.5	V
Maximum low level dynamic input voltage $V_{\rm IL}$	V _{ILD}	C _L = 50 pF	5.0	_	1.5	V

Input Equivalent Circuit



Package Dimensions



Weight: 0.02 g (typ.)

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