TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

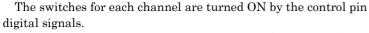
TC7MZ4051FK,TC7MZ4052FK,TC7MZ4053FK

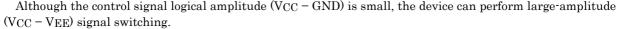
TC7MZ4051FK 8-Channel Analog Multiplexer/Demultiplexer TC7MZ4052FK Dual 4-Channel Analog Multiplexer/Demultiplexer

TC7MZ4053FK Triple 2-Channel Analog Multiplexer/Demultiplexer

The TC7MZ4051/4052/4053FK are high-speed, low-voltage drive analog multiplexer/demultiplexers using silicon gate CMOS technology. In 3 V and 5 V systems these can achieve high-speed operation with the low power dissipation that is a feature of CMOS.

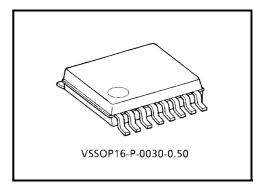
The TC7MZ4051/4052/4053FK offer analog/digital signal selection as well as mixed signals. The 4051 has an 8-channel configuration, the 4052 has an 4-channel \times 2 configuration, and the 4053 has a 2-channel \times 3 configuration.





For example, if VCC = 3 V, GND = 0 V, and VEE = -3 V, signals between -3 V and +3 V can be switched from the logical circuit using a single 3 V power supply.

All input pins are equipped with a newly developed input protection circuit that avoids the need for a diode on the plus side (forward side from the input to the VCC). As a result, for example, 5 V signals can be permitted on the inputs even when the power supply voltage to the circuits is off. As a result of this input power protection, the TC7MZ4051/4052/4053FK can be used in a variety of applications, including in the system which has two power supplies, and in battery backup circuits.



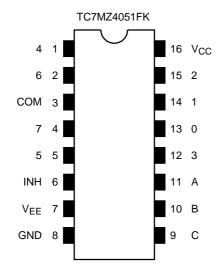
Weight: 0.02 g (typ.)

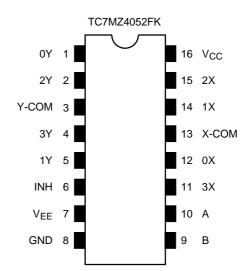
Features

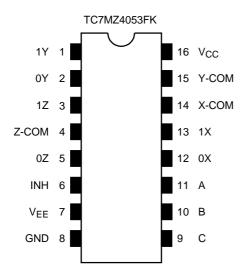
- Low ON resistance: $R_{on} = 22 \Omega$ (typ.) (V_{CC} V_{EE} = 3 V) $R_{on} = 15 \Omega$ (typ.) (V_{CC} - V_{EE} = 6 V)
- High speed: $t_{pd} = 3 \text{ ns (typ.) (V}_{CC} = 3.0 \text{ V})$
- Low power dissipation: $ICC = 4 \mu A \text{ (max)} \text{ (Ta} = 25 \text{°C)}$
- Input level: VIL = 0.8 V (max) (VCC = 3 V)VIH = 2.0 V (min) (VCC = 3 V)
- Power down protection is provided on all control inputs
- Pin and function compatible with 74HC4051/4052/4053



Pin Assignment (top view)







Truth Table

	Contro	l Inputs		"ON" Channel				
Inhibit	C*	В	Α	MZ4051FK	MZ4052FK	MZ4053FK		
L	L	L	L	0	0X, 0Y	0X, 0Y, 0Z		
L	L	L	Н	1	1X, 1Y	1X, 0Y, 0Z		
L	L	Н	L	2	2X, 2Y	0X, 1Y, 0Z		
L	L	Н	Н	3	3X, 3Y	1X, 1Y, 0Z		
L	Н	L	L	4	_	0X, 0Y, 1Z		
L	Н	L	Н	5	_	1X, 0Y, 1Z		
L	Н	Н	L	6	_	0X, 1Y, 1Z		
L	Н	Н	Н	7	_	1X, 1Y, 1Z		
Н	Х	Х	Х	None	None	None		

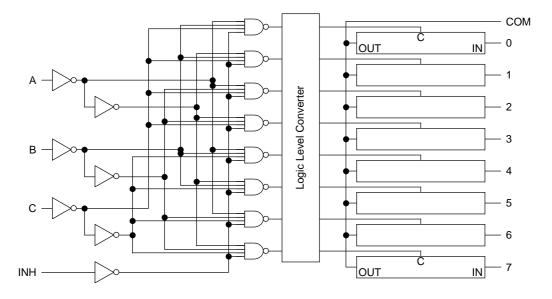
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X: Don't care, *: Except MZ4052FK

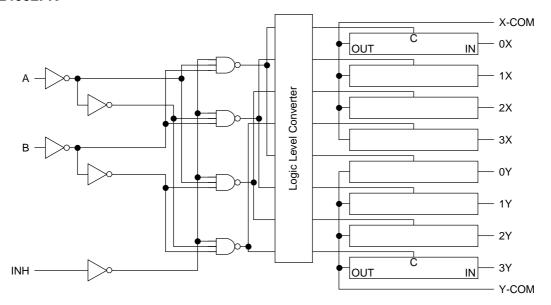
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System Diagram

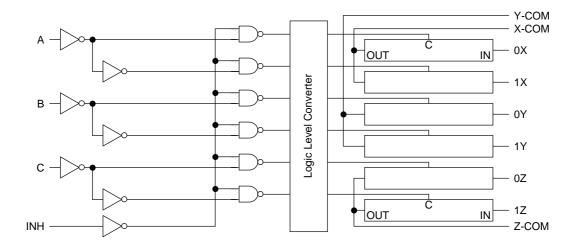
TC7MZ4051FK



TC7MZ4052FK



TC7MZ4053FK



3



Absolute Maximum Ratings

Characteristics	Symbol	Rating	Unit	
Power supply voltage	V _{CC}	-0.5~7.0	V	
Fower supply voltage	V _{CC} ~V _{EE}	-0.5~7.0	V	
Control input voltage	V _{IN}	-0.5~7.0	٧	
Switch I/O voltage	V _{I/O}	V _{EE} - 0.5~V _{CC} + 0.5	V	
Input diode current	I _{IK}	-20	mA	
I/O diode current	I _{IOK}	±20	mA	
Switch through current	Ι _Τ	±25	mA	
DC V _{CC} or ground current	Icc	±50	mA	
Power dissipation	PD	180	mW	
Storage temperature	T _{stg}	-65~150	°C	

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit	
	V _{CC}	2~6		
Power supply voltage	V _{EE}	-4~0	V	
	V _{CC} ~V _{EE}	2~6		
Input voltage	V _{IN}	0~6.0	V	
Switch I/O voltage	V _{I/O}	V _{EE} ~V _{CC}	V	
Operating temperature	T _{opr}	-40~85	°C	
Input rise and fall time	dt/dv	$0 \sim 100 \; (V_{CC} = 3.3 \pm 0.3 \; V)$	ns/V	
input noe and fall time	ui/uv	0~20 (V _{CC} = 5 ± 0.5 V)	115/ V	



Electrical Characteristics

DC Electrical Characteristics

Characteristics		Symbol Test Condition				Ta = 25°C			Ta = -40~85°C		Unit
Onaracie	Characteristics		rest Condition	V _{EE} (V)	V _{CC} (V)	Min	Тур.	Max	Min	Max	Offic
					2.0	1.5	_	_	1.5	_	
	High-level	V _{IH}			3.0	2.0	_	_	2.0	_	
	I light level	V IH			4.5	3.15		_	3.15		
Input voltage					6.0	4.2		_	4.2	_	V
input voltage					2.0		—	0.5	_	0.5	V
	Low-level	V _{IL}			3.0		_	0.8	_	0.8	
	LOW-level	V IL	_		4.5		_	1.35	_	1.35	
					6.0			1.8	_	1.8	
			V V or V	GND	2.0		200	_	_	_	Ω
		\	$V_{IN} = V_{IL}$ or V_{IH} $V_{I/O} = V_{CC}$ to V_{EE} $I_{I/O} = 2$ mA	GND	3.0		45	86	_	108	
				GND	4.5		24	37	_	46	
ON resistance				-3.0	3.0		17	26	_	33	
ON resistance		TON	V _{IN} = V _{IL} or V _{IH}	GND	2.0		28	73		84	52
			$V_{I/O} = V_{IC}$ or V_{EE} $I_{I/O} = 2 \text{ mA}$	GND	3.0		22	38	_	44	
				GND	4.5		17	27	_	31	
			11/0 – 2 111/4	-3.0	3.0	_	15	24	_	28	
			$V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{I/O} = V_{CC} \text{ to } V_{EE}$	GND	2.0		10	25	_	35	Ω
Difference of Ol resistance betw		ΔR _{ON}		GND	3.0		5	15	_	20	
switches	CCII	ZIVON	$I_{I/O} = 2 \text{ mA}$	GND	4.5		5	13	_	18	
			1 /O = 2 111A	-3.0	3.0		5	10	_	15	
Input/Output lea	akage		$V_{OS} = V_{CC}$ or GND	GND	3.0			±0.25		±2.5	
current (switch OFF)		l _{OFF}	$V_{IS} = GND \text{ to } V_{CC}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$	-3.0	3.0		_	±0.5	_	±5.0	μА
Input/Output leakage current (switch ON, output open)		. Vo	$V_{OS} = V_{CC}$ or GND	GND	3.0	_		±0.25	_	±2.5	μА
		I _{IN}	$V_{IN} = V_{IL}$ or V_{IH}	-3.0	3.0	_	_	±0.5	_	±5.0	
Control input current		I _{IN}	$V_{IN} = V_{CC}$ or GND	GND	6.0	_	_	±0.1	_	±0.1	μΑ
Quiescent supply current				GND	3.0	_	_	4.0	_	40.0	
		Icc	$V_{IN} = V_{CC}$ or GND	-3.0	3.0		_	8.0	_	80.0	μΑ

5



AC Electrical Characteristics ($C_L = 50 \text{ pF}$, Input: $t_r = t_f = 3 \text{ ns}$, GND = 0 V)

Characteristics	Symbol	ol Test Condition					Ta = 25°C			Ta = -40~85°C	
Characteristics	Symbol			V _{EE} (V)	V _{CC} (V)	Min	Тур.	Max	Min	Max	Unit
		All types		GND	2.0	_	3.2	6.0	_	6.9	ns
Phase difference between	φΙ/О			GND	3.0		1.8	3.0	_	3.5	
input and output	ψι/Ο	All type		GND	4.5		1.3	1.8		2.1	113
				-3.0	3.0		1.1	1.3		1.5	
				GND	2.0		9.0	17		20	
Output enable time	t _{pZL}	Figure	1 (Note 1)	GND	3.0		5.7	9.0	_	11	ne
Output enable time	t _p ZH	rigure	(14016-1)	GND	4.5		4.5	6.0		7.0	ns
				-3.0	3.0		5.8	8.0		10	
			1 (Note 1)	GND	2.0		13.5	21		25	ns
Output disable time	t _{pLZ}	Figure 1 (Note 1)		GND	3.0		11.3	15	_	18	
Output disable time	t _{pHZ}		GND	4.5		10.3	12	_	14	115	
				-3.0	3.0		10.9	13			15
Control input capacitance	C _{in}	All type	es (Note 2)		_		5	10		10	pF
		4051	Figure 2 (Note 2)				11	25		25	
COMMON terminal capacitance	C _{IS}	4052		-3.0	3.0	_	9	20		20	pF
		4053					7	15		15	
		4051	Figure 2				6	13		13	
SWITCH terminal capacitance	Cos	4052	(Note 2)	-3.0	3.0	_	6	13	_	13	pF
		4053	(14016-2)				6	13		13	
		4051					3	6		6	
Feedthrough capacitance	C _{IOS}	4052	Figure 2 (Note 2)	-3.0	3.0	_	3	6	_	6	pF
		4053	,				3	6		6	
		4051		GND	6.0	_	14				
Power dissipation capacitance	C_{PD}	4052	Figure 2 (Note 3)				24	_	_	_	рF
		4053					18				

Note1: $R_L = 1 k\Omega$

Note2: C_{in} , C_{IS} , C_{OS} and C_{IOS} are guaranteed by the design.

Note3: C_{PD} is defined as the value of the internal equivalent capacitance of IC which is calculated from the

6

operating current consumption without load.

Average operating current can be obtained by the equation:

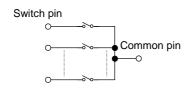
 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$



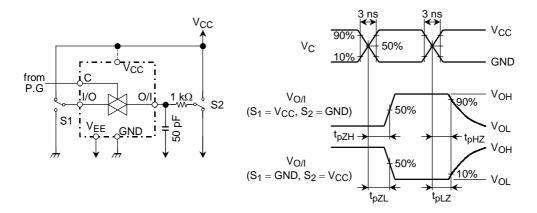
*Analog Switch Characteristics (GND = 0 V, Ta = 25°C)

Characteristics	Symbol	Test Condition			Тур.	Unit	
Characteristics	Symbol	rest condition		V _{EE} (V)	V _{CC} (V)	Typ.	Offic
			$V_{IN} = 2.0 V_{p-p}$	0	3.0	0.100	%
Sine Wave Distortion (T.H.D)		$R_L = 10 \text{ k}\Omega, C_L = 50 \text{ pF},$ $f_{IN} = 1 \text{ kHz}$	$V_{IN} = 4.0 V_{p-p}$	0	4.5	0.030	
			$V_{IN} = 6.0 V_{p-p}$	-0.3	3.0	0.020	
			4051			150	MHz
			4052	0	3.0	180	
		Adjust f _{IN} voltage to obtain 0dBm at V _{OS} .	4053			200	
Eroguanay roopana		Increase f _{IN} frequency until dB	4051			150	
Frequency response (switch ON)	f _{max}	meter reads –3dB.	4052	0	4.5	180	
(SWILCH OIV)		$R_L = 50 \Omega$, $C_L = 10 pF$, $f_{IN} = 1 MHz$, sine wave	4053			200	
		Figure 3	4051		3.0	150	
			4052	-3.0		180	
			4053			200	
		V _{IN} is centered at (V _{CC} – V _{EE})/2.	0	3.0	-45	dB	
		Adjust input for 0dBm.		0	0 4.5		-45
		$R_L = 600 \Omega$, $C_L = 50 pF$, $f_{IN} = 1 M$	0	4.5	-45		
Feed through attenuation (switch OFF)		Figure 4	-3.0	3.0	-45		
,			0	3.0	-60		
		$R_L = 50 \ \Omega, \ C_L = 10 \ pF, \ f_{IN} = 1 \ MHz, \ sine \ v$		0	4.5		-60
			-3.0	3.0	-60		
Crosstalk		$R_L = 600 \Omega$, $C_L = 50 pF$, $f_{IN} = 1 M$	Hz, square wave	0	3.0	90	
(control input to signal		$(t_r = t_f = 6 \text{ ns})$		0	4.5	150	mV
output)		Figure 5		-3.0	3.0	120	
Crosstalk		Adjust V _{IN} to obtain 0dBm at inpu	0	3.0	-45	dB	
(between any switches)		$R_L = 600 \Omega$, $C_L = 50 pF$, $f_{IN} = 1 M$	0	4.5	-45		
(SSCHOOLI GITY OWNORDS)		Figure 6		-3.0	3.0	-45	

^{*:} These characteristics are determined by design of devices.



AC Test Circuit



 $\label{eq:figure 1} \textbf{Figure 1} \quad t_{\text{pLZ}},\, t_{\text{pHZ}},\, t_{\text{pZL}},\, t_{\text{pZH}}$

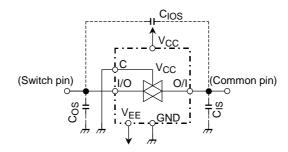


Figure 2 C_{IOS}, C_{IS}, C_{OS}

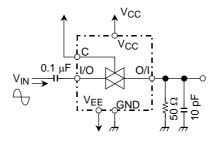


Figure 3 Frequency Response (switch on)

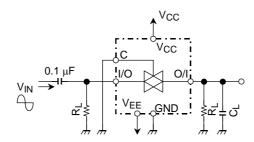


Figure 4 Feedthrough

8

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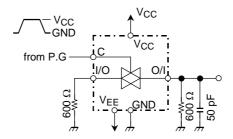


Figure 5 Cross Talk (control input to output signal)

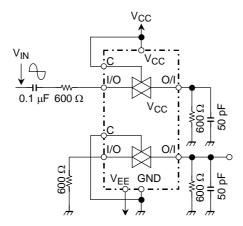
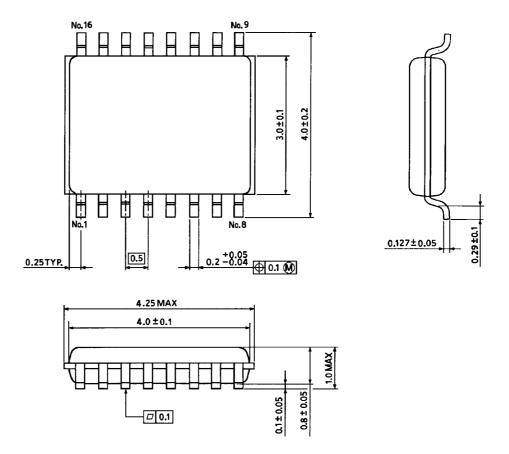


Figure 6 Cross Talk (between any two switches)

9



Package Dimensions



Weight: 0.02 g (typ.)

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