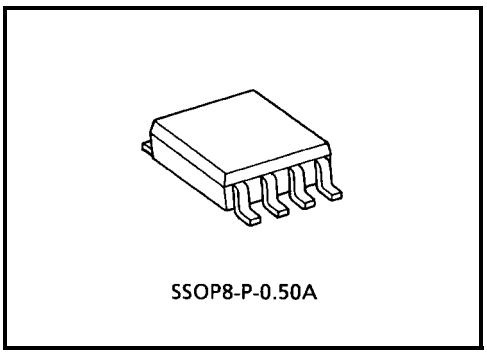
TOSHIBA CMOS Digital Integrated Circuits Silicon Monolithic

TC9WMA1FK

1,024-Bit (128 × 8 Bit) Serial E^2PROM

The TC9WMA1FK is electrically erasable/programmable nonvolatile memory (E^2PROM).

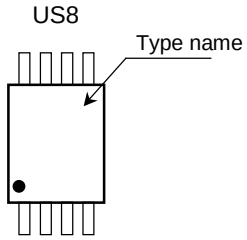


Weight: 0.01 g (typ.)

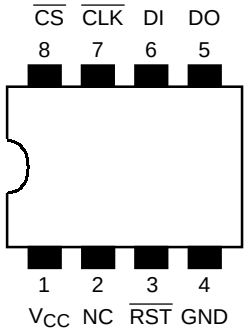
Features

- Serial data input/output
- Programmable in units of one word and collectively erasable in one operation
- Automatically set programming time (built-in timer)
- Programming time: 10 ms (max) (V_{CC} = 3.0 to 3.6 V)
  13 ms (max) (V_{CC} = 2.7 to 3.6 V)
- Overwriting enabled or disabled by software
- Single power supply and low power consumption
- Operating power supply voltage (2.7 to 3.6 V)
- Wide operating temperature range (−40 to 85°C)

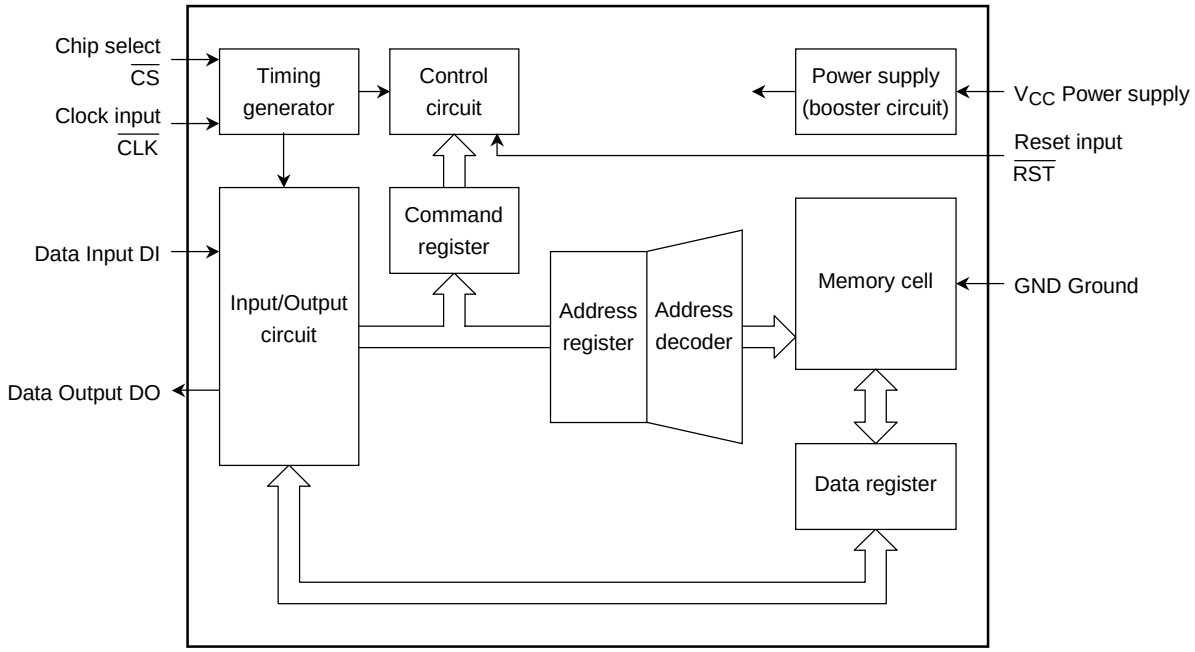
Product Marking



Pin Assignment (top view)



Block Diagram



Pin Function

Pin Name	Input/Output	Function
$\overline{CS}$	Input	Chip select A low on $\overline{CS}$ selects the chip. Always return $\overline{CS}$ high temporarily before executing instructions.
$\overline{CLK}$	Input	Clock input The data on DI is latched by a rising edge of $\overline{CLK}$. Data is output to DO by a falling edge of $\overline{CLK}$. $\overline{CLK}$ is effective when $\overline{CS}$ is low.
DI	Input	Serial data input This pin is used to enter addresses, commands, and data into the chip.
DO	Output	Serial data output This pin outputs data from the chip.
$\overline{RST}$	Input	Reset input A low on this input resets the chip.
NC	—	No connection (not connected internally)
V_{CC}	Power supply	2.7 V~3.6 V
GND		0 V (GND)

Functional Description

1. Types of Instructions

Operation	Address	Command								Data
		C0	C1	C2	C3					
Read	A0~A6, 0	1	0	0	0	0	0	0	0	
Program	A0~A6, 0	0	1	1	0	0	0	0	0	D0~D7
All erase	********	0	0	1	1	0	0	0	0	
Busy monitor	********	1	0	1	1	0	0	0	0	
Overwrite enable	********	1	0	0	1	0	0	0	0	
Overwrite disable	********	1	1	0	1	0	0	0	0	

*: Don't care

2. Operation Method

Be sure to return $\overline{CS}$ and $\overline{CLK}$ high temporarily before entering instructions.

After $\overline{CS}$ is asserted low, $\overline{CLK}$ becomes effective, acting as a serial transfer synchronizing signal. The data on DI is latched by a rising edge of $\overline{CLK}$, while data is output to DO by a falling edge of $\overline{CLK}$. Instructions can only be executed when the chip is not being programmed or collectively erased (i.e., when the ready/busy status signal is high). However, the Busy Monitor instruction can be entered at any time.

Only the commands listed in the above table can be used. Do not use any other command.

(1) Read

When the Read instruction is entered, memory data at the specified address is read out and is serially output from the DO pin.

(2) Program

When the Program instruction is entered, overwrite operation automatically starts internally in the chip, and memory data at the specified address is overwritten with the input data. After the instruction is entered, $\overline{CS}$ can be returned high even while overwrite operation is in progress internally.

(3) All Erase

When the All Erase instruction is entered, erase operation automatically starts internally in the chip, and memory data at all addresses are erased. After the instruction is entered, $\overline{CS}$ can be returned high even while erase operation is in progress internally. Execution of this command clears the memory data to 0.

(4) Busy Monitor

When the Busy Monitor instruction is entered, a ready/busy status signal is output from the DO pin. This output signal is low while the chip is being programmed or collectively erased, and is high after programming or collective erase operation is completed.

The ready/busy status signal is output continuously until $\overline{CS}$ is returned high.

(5) Overwrite Enable/Disable

When the Overwrite Enable instruction is entered, the chip is placed in overwrite enable mode, where the Program and All Erase instructions are enabled. When the Overwrite Disable instruction is entered, the chip is placed in overwrite disable mode, where the Program and All Erase instructions both are disabled.

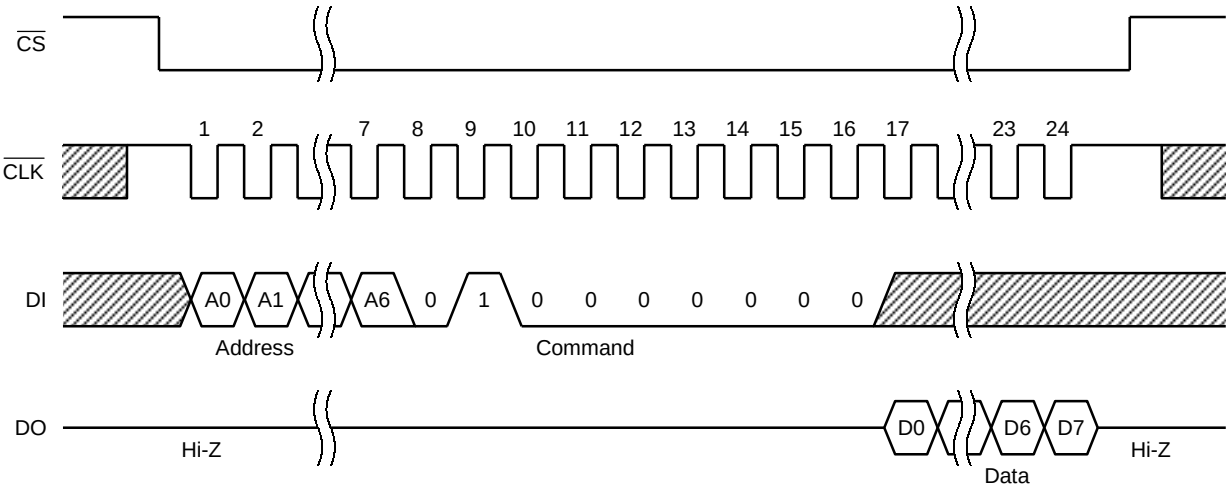
Once the chip is placed in overwrite disable mode, it remains disabled against overwriting unless the Overwrite Enable instruction is entered.

3. Precautions to be Taken at Power ON/OFF

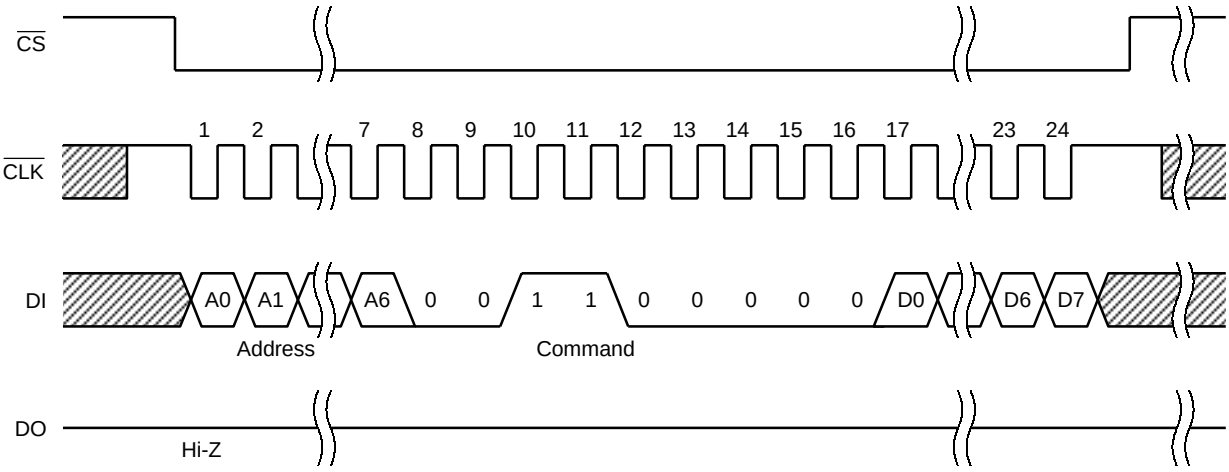
(1) A wait time of 1 ms is required before the chip starts operation after it is powered on.
(2) $\overline{\text{RST}}$ must be pulled low when the power to the chip turns ON or OFF.
(3) The chip is placed in overwrite disable mode by reset.

4. Timing Chart

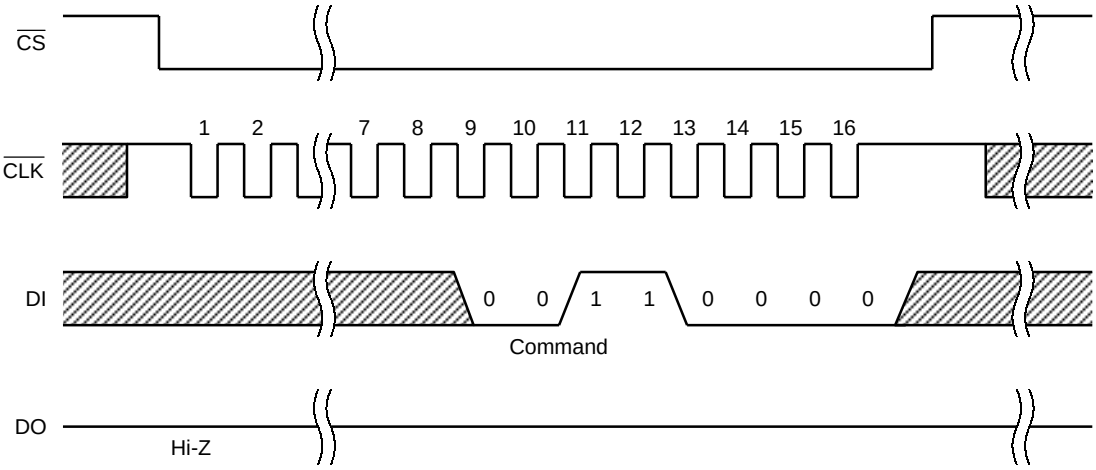
(1) Read



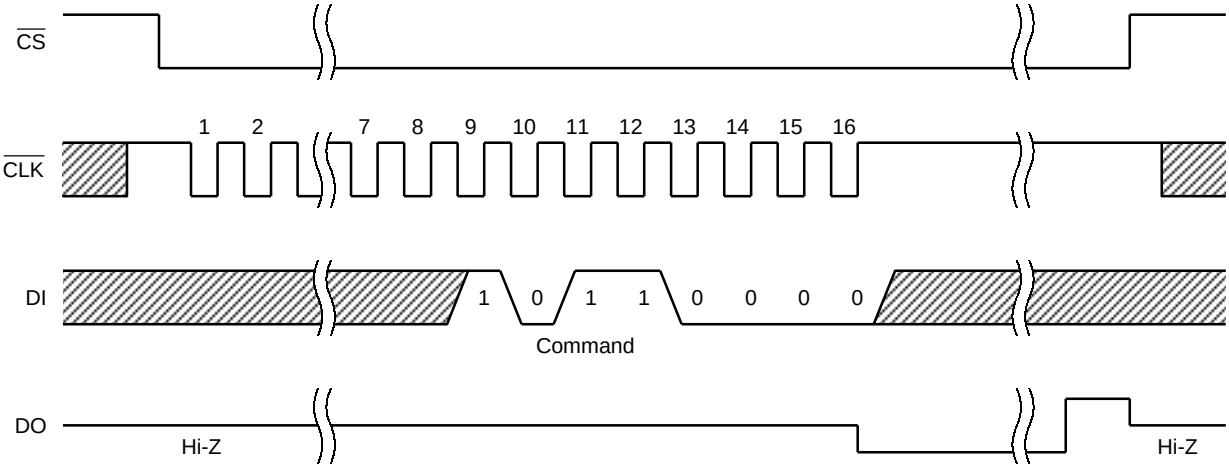
(2) Program



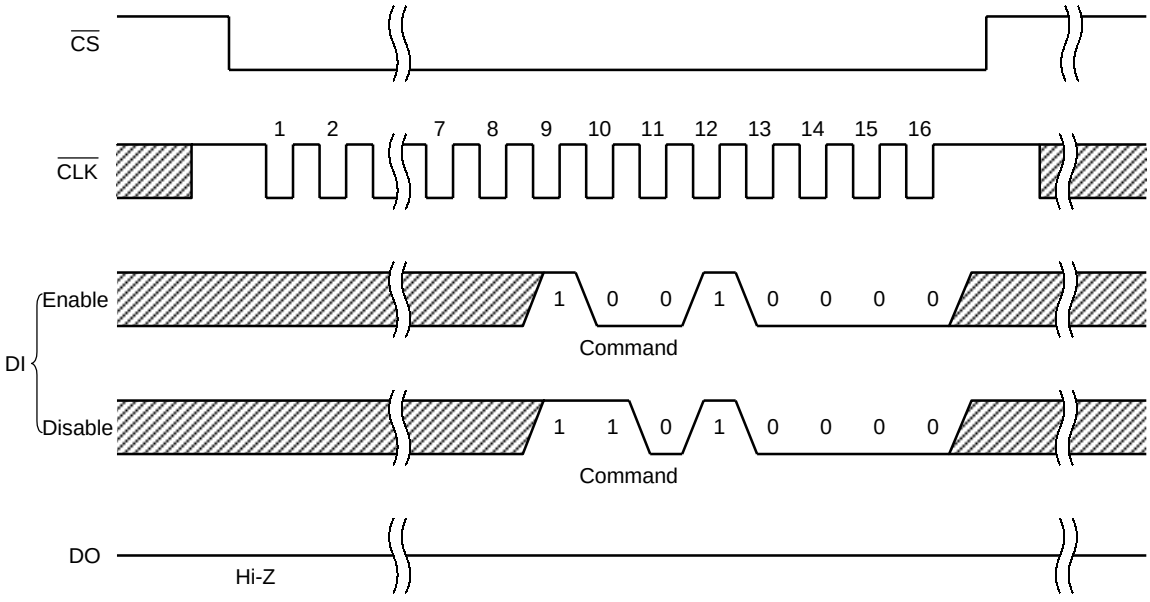
(3) All Erase



(4) Busy Monitor



(5) Overwrite Enable/Disable



Maximum Ratings (GND = 0 V)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.3~4.6	V
Input voltage	V_{IN}	−0.3~V_{CC} + 0.3	V
Output voltage	V_{OUT}	−0.3~V_{CC} + 0.3	V
Power dissipation	P_D	200 (25°C)	mW
Soldering temperature (in time)	T_{sld}	260 (10 s)	°C
Storage temperature	T_{stg}	−55~125	°C
Operating temperature	T_{opr}	−40~85	°C

Recommended Operating Conditions (GND = 0 V, T_{opr} = −40~85°C)

Characteristics	Symbol	Test Condition	Min	Max	Unit
Power supply voltage	V_{CC}		2.7	3.6	V

Recommended Operating Conditions (GND = 0 V, V_{CC} = 2.7~3.6 V, T_{opr} = −40~85°C)

Characteristics	Symbol	Pin	Test Condition	Min	Max	Unit
Low level input voltage	V_{IL}		V_{CC} = 2.7 V	0	0.45	V
High level input voltage	V_{IH1}	$\overline{CS}$, DI, $\overline{RST}$	V_{CC} = 3.6 V	1.6	V_{CC}	V
	V_{IH2}	$\overline{CLK}$	V_{CC} = 3.6 V	2.2	V_{CC}	
Operating frequency	f_{CLK}			0	1	MHz

Electrical Characteristics

D.C. Characteristics (GND = 0 V, V_{CC} = 2.7~3.6 V, T_{opr} = –40~85°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input current	I_{LI}		—	—	±5	μA
Output leakage current	I_{LO}		—	—	±5	μA
High level output voltage	V_{OH}	V_{CC} = 2.7 V, I_{OH} = –1 mA	V_{CC} – 0.4	—	—	V
Low level output voltage	V_{OL}	V_{CC} = 2.7 V, I_{OL} = 2 mA	—	—	0.4	V
Quiescent supply current	I_{CC1} (Note1)		—	—	5	μA
Supply current during read	I_{CC2} (Note2)		—	—	1.5	mA
Supply current during all erase/program	I_{CC3} (Note3)		—	—	1.0	mA

Note 1: $\overline{CS}$ = 1 (except when busy, however)

Note 2: Current that flows for a period from a fall of the 14th to a fall of the 17th $\overline{CLK}$ pulse when executing the read instruction.

Note 3: Current that flows while executing the all erase or program instruction.

A.C. Characteristics (GND = 0 V, V_{CC} = 2.7~3.6 V, T_{opr} = –40~85°C)

Characteristics	Symbol	Test Condition	Min	Max	Unit
Maximum clock frequency	f_{MAX}		0	1	MHz
Minimum clock pulse width	twCLK (L)		400	—	ns
	twCLK (H)				
Minimum reset pulse width	t_{WRST}		1	—	μs
Minimum chip select pulse width	t_{WCS}		1	—	μs
Reset setup time	t_{RSS}	$\overline{RST}$ setup time when $\overline{CS}$ is switched over	1	—	μs
Clock setup time	t_{CKS}	$\overline{CLK}$ setup time when $\overline{CS}$ is switched over	250	—	ns
$\overline{CS}$ setup time	t_{CSS}	$\overline{CS}$ setup time when $\overline{CLK}$ is switched over	250	—	ns
Propagation delay time (Note4)	t_{pLH} t_{pHL} t_{pZH} t_{pZL}	Time from $\overline{CLK}$ switchover until valid data is output	—	250	ns
	t_{pLZ} t_{pHZ}	Time from $\overline{CS}$ switchover until output data goes Hi-Z	—	500	
Input data setup time	t_s	Input data setup time when $\overline{CLK}$ is switched over	250	—	ns
Input data hold time	t_h	Input data hold time when $\overline{CLK}$ is switched over	250	—	ns

Note 4: C_L = 100 pF, R_L = 1 kΩ

E^2PROM Characteristics (GND = 0 V, 3.0 V ≦ V_{CC} ≦ 3.6 V, T_{opr} = –40~85°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
All erase time	t_E		—	6	10	ms
Program time	t_P		—	6	10	ms
Endurance	N_{EW}		1×10^5	—	—	Times
Data retention time	t_{RET}		10	—	—	Year

E^2PROM Characteristics (GND = 0 V, 2.7 V ≦ V_{CC} ≦ 3.6 V, T_{opr} = –40~85°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
All erase time	t_E		—	7	13	ms
Program time	t_P		—	7	13	ms
Endurance	N_{EW}		1×10^5	—	—	Times
Data retention time	t_{RET}		10	—	—	Year

Capacitance Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}		3.3	4	pF
Output capacitance	C_O		3.3	3	pF
Equivalent Internal capacitance	C_{PD}	f_{IN} = 1 MHz (Note5)	3.3	8.5	pF

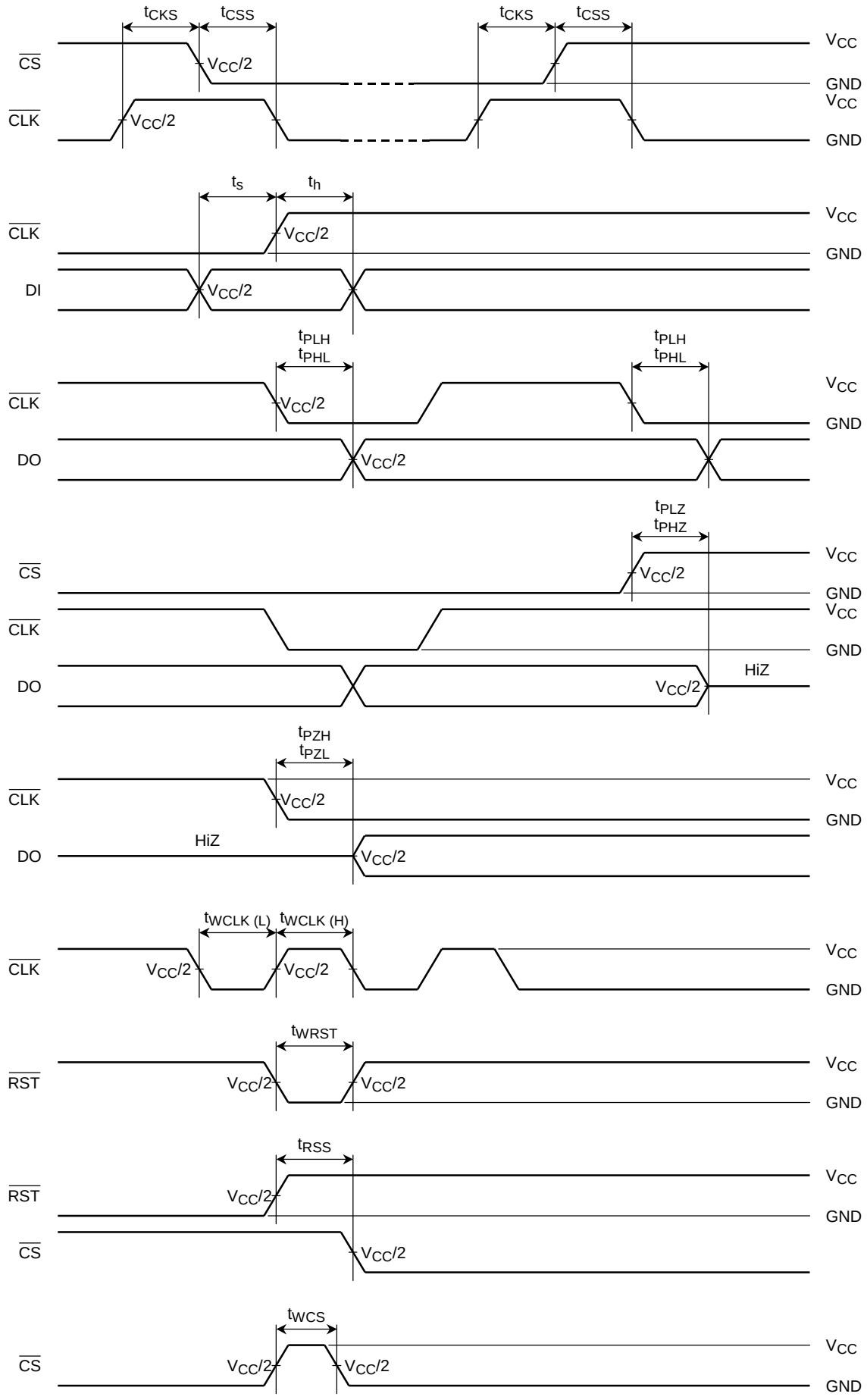
Note 5: C_{PD} denotes the IC's internal equivalent capacitance calculated from the amount of current it consumes while operating.

The average current consumption during non-loaded operation is obtained from the equations below.

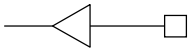
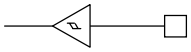
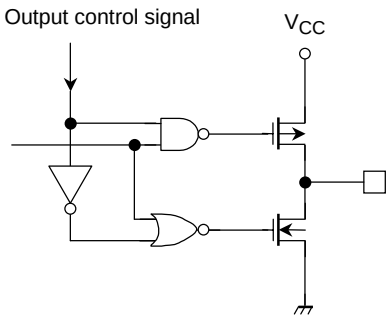
$I_{CC\ (Read)} = f_{CLK} \cdot C_{PD} \cdot V_{CC} + I_{CC1} + I_{CC2} \cdot 3.5/24$

$I_{CC\ (Prog)} = f_{CLK} \cdot C_{PD} \cdot V_{CC} + I_{CC1} + I_{CC3}$

A.C. Characteristics Timing Chart

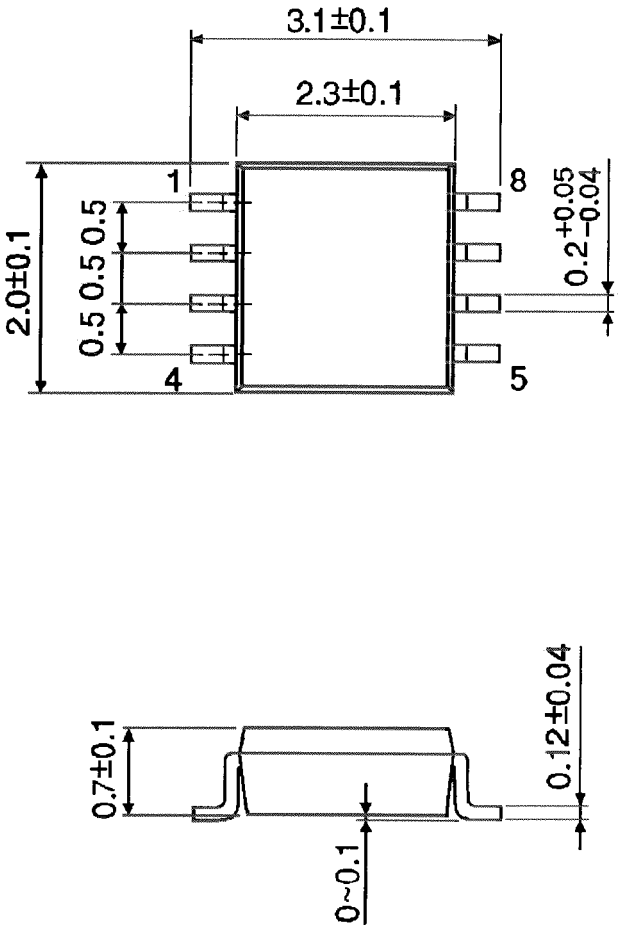


Input/Output Circuits of Pins

Pin Name	Type	Input/Output Circuit	Remarks
$\overline{CS}$ DI $\overline{RST}$	Input		
$\overline{CLK}$	Input		Hysteresis input
DO	Output		Initial “HiZ”

Package Dimensions

SSOP8-P-0.50A Unit : mm



Weight: 0.01 g (typ.)

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