

TC74HC259AP, TC74HC259AF, TC74HC259AFN

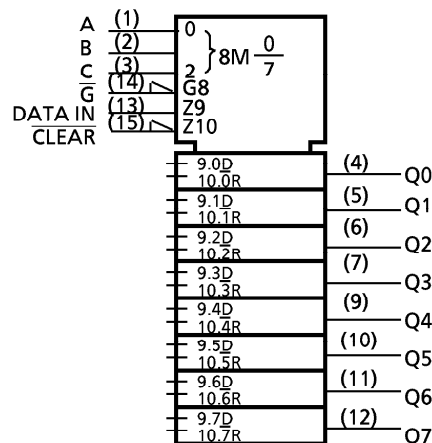
8-BIT ADDRESSABLE LATCH

The TC74HC259A is a high speed CMOS ADDRESSABLE LATCH fabricated with silicon gate C²MOS technology. It achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The respective bits are controlled by address inputs A, B, and C. When $\overline{\text{CLEAR}}$ input is held high and enable input G is held low, the data is written into the bit selected by address inputs, the other bit hold their previous conditions. When both $\overline{\text{CLEAR}}$ and $\overline{\text{G}}$ held high, writing of all bits is inhibited regardless of adress inputs, and their previous condition are held. When $\overline{\text{CLEAR}}$ is held low and $\overline{\text{G}}$ is held high, all bits are resnt to low regardless of the other inputs. When both of $\overline{\text{CLEAR}}$ and $\overline{\text{G}}$ held low, all bits whichi isn't selected by adress inputs are resnt to low. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

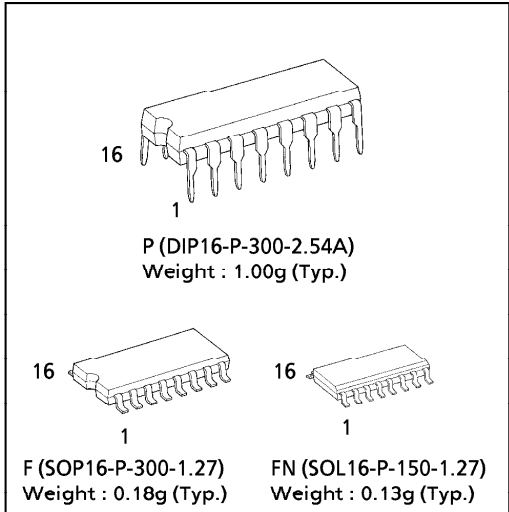
FEATURES:

- High Speed..... $t_{pd} = 15\text{ns}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}(\text{Min.})$
- Output Drive Capability..... 10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range.... $V_{CC}(\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS259

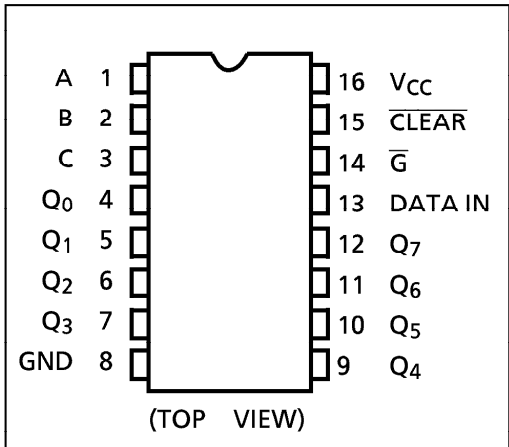
IEC LOGIC SYMBOL



(Note) The JEDEC SOP (FN) is not available in Japan.



PIN ASSIGNMENT



961001EBA2

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TRUTH TABLE

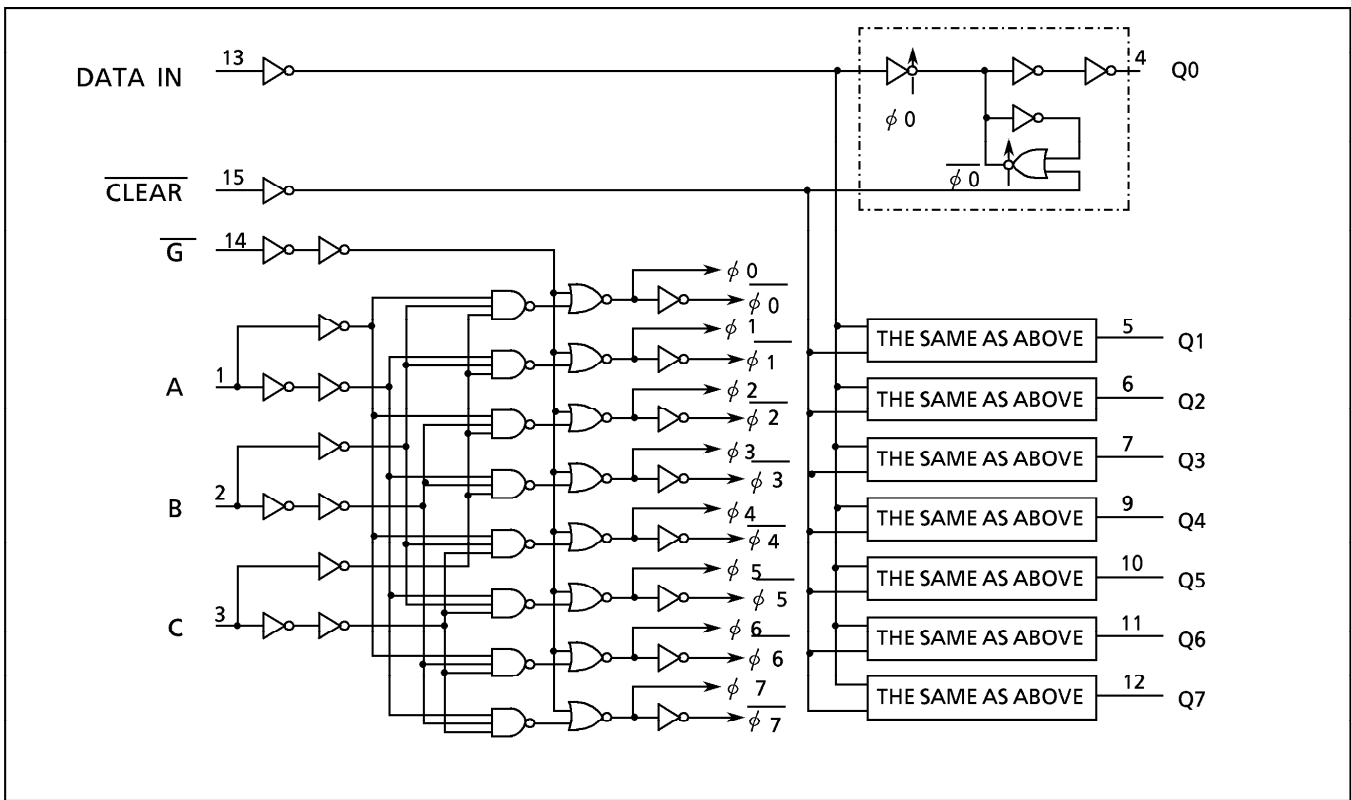
INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLEAR	$\overline{G}$			
H	L	D	Q _{iO}	ADDRESSABLE LATCH MEMORY 8— LINE DEMULTIPLEXER CLEAR ALL BITS TO "L"
H	H	Q _{iO}	Q _{iO}	
L	L	D	L	
L	H	L	L	

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

D : The level at the data input.

Q_{iO} : The level before the indicated steady— state input conditions were established (i = 0, 1, ...7)

SYSTEM DIAGRAM



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- The products described in this document are subject to foreign exchange and foreign trade control laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} / Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	0~1000 ($V_{CC} = 2.0\text{V}$) 0~500 ($V_{CC} = 4.5\text{V}$) 0~400 ($V_{CC} = 6.0\text{V}$)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	V
			$I_{OH} = -4 \text{ mA}$	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	
			$I_{OH} = -5.2 \text{ mA}$	6.0	5.68	5.80	—	5.63	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	V
			$I_{OL} = 4 \text{ mA}$	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	
			$I_{OL} = 5.2 \text{ mA}$	6.0	—	0.18	0.26	—	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width ($\overline{G}$)	$t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{W(L)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (DATA)	t_s		2.0	—	50	60	
			4.5	—	10	12	
			6.0	—	9	11	
Minimum Set-up Time (A, B, C)	t_s		2.0	—	25	30	
			4.5	—	5	6	
			6.0	—	5	5	
Minimum Set-up Time (DATA)	t_h		2.0	—	25	30	
			4.5	—	5	6	
			6.0	—	5	5	
Minimum Hold Time (A, B, C)	t_h		2.0	—	0	0	MHz
			4.5	—	0	0	
			6.0	—	0	0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, Ta = 25°C, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (DATA—Q)	t_{pLH} t_{pHL}		—	15	22	
Propagation Delay Time (A, B, C—Q)	t_{pLH} t_{pHL}		—	21	32	
Propagation Delay Time ($\overline{G}$ —Q)	t_{pLH} t_{pHL}		—	16	28	
Propagation Delay Time ($\overline{CLEAR}$ —Q)	t_{pHL}		—	13	23	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.
Output Transition Time	t_{TLH} t_{THL}		2.0	—	30	75	—	95
			4.5	—	8	15	—	19
			6.0	—	7	13	—	16
Propagation Delay Time (DATA—Q)	t_{PLH} t_{PHL}		2.0	—	56	130	—	165
			4.5	—	18	26	—	33
			6.0	—	15	22	—	28
Propagation Delay Time (A, B, C—Q)	t_{PLH} t_{PHL}		2.0	—	83	185	—	230
			4.5	—	25	37	—	46
			6.0	—	21	31	—	39
Propagation Delay Time ($\overline{G}$ —Q)	t_{PLH} t_{PHL}		2.0	—	67	165	—	205
			4.5	—	20	33	—	41
			6.0	—	17	28	—	35
Propagation Delay Time ($\overline{\text{CLEAR}}$ —Q)	t_{PHL}		2.0	—	52	135	—	170
			4.5	—	16	27	—	34
			6.0	—	14	23	—	29
Input Capacitance	C _{IN}			—	5	10	—	10
Power Dissipation Capacitance	C _{PD} (1)			—	35	—	—	—

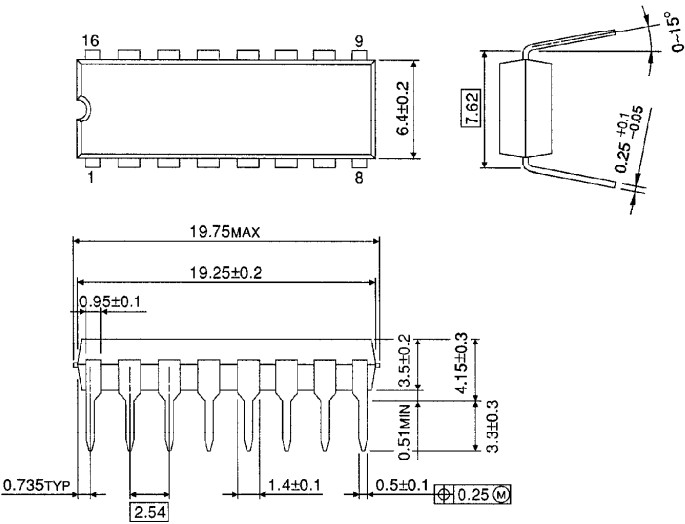
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

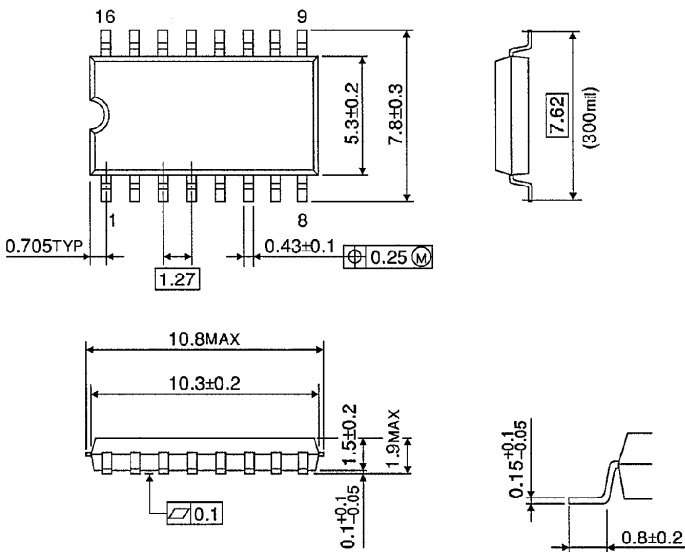
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm

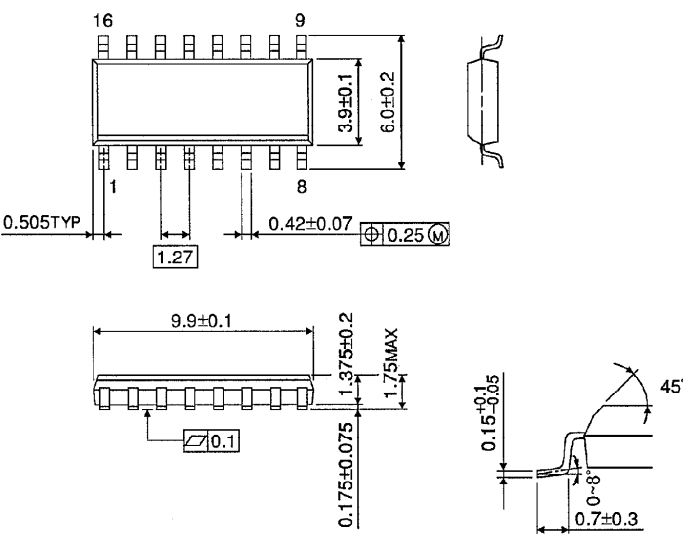


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)