

TC74HC251AP, TC74HC251AF

8 - CHANNEL MULTIPLEXER (3 - STATE)

The TC74HC251A is a high speed CMOS 8 - CHANNEL MULTIPLEXER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

One of eight data input signals (D0 - D7) is selected by decoding of the address input (A, B, C). The selected data appears on two outputs; non - inverting (Y) and inverting (W). When the strobe input is held high, both outputs are in the high-impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

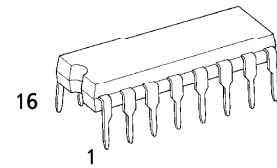
- High Speed..... $t_{pd} = 15\text{ns}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}(\text{Min.})$
- Output Drive Capability..... 10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range.... $V_{CC}(\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS251

TRUTH TABLE

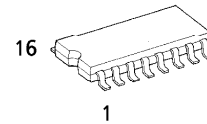
INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	$\overline{ST}$		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

X : Don't Care

H : High Impedance

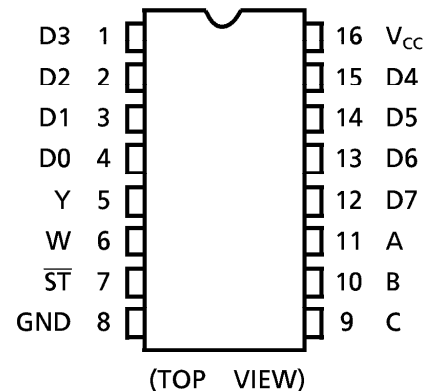


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

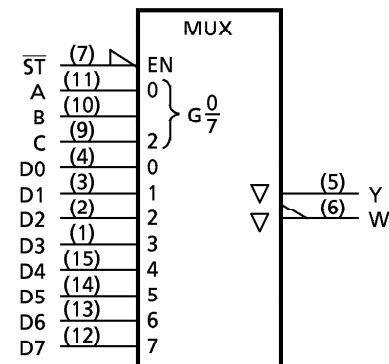


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL



961001EBA2

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The diagram illustrates the internal logic of a 74181 ALU. It features several input lines on the left: $\overline{ST}$ (pin 7), data inputs $D0$ through $D7$ (pins 4, 3, 2, 1, 15, 14, 13, 12), and control inputs A , B , and C (pins 11, 10, 9). Each data input D_i is connected to a buffer (labeled S_i) and an inverter (labeled $\overline{S_i}$). The $\overline{ST}$ input is connected to a network of inverters. The control inputs A , B , and C are connected to a network of inverters and AND gates. The output W (pin 6) is the result of a complex logic function involving the data inputs and control signals. The output Y (pin 5) is the result of a similar logic function. The status outputs $S0$ through $S7$ are the outputs of the buffers, and $\overline{S0}$ through $\overline{S7}$ are the outputs of the inverters.

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} / Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000 (V_{CC} = 2.0\text{V})$ $0 \sim 500 (V_{CC} = 4.5\text{V})$ $0 \sim 400 (V_{CC} = 6.0\text{V})$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
			4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
3 - State Off Leak Current	I_{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or GND}$	6.0	—	—	± 0.5	—	± 5.0	μA
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	± 0.1	—	± 1.0	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	4.0	—	40.0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (D—Y)	t_{pLH} t_{pHL}		—	14	24	
Propagation Delay Time (D—W)	t_{pLH} t_{pHL}		—	15	24	
Propagation Delay Time (A, B, C—Y)	t_{pLH} t_{pHL}		—	19	31	
Propagation Delay Time (A, B, C—W)	t_{pLH} t_{pHL}		—	19	31	
3-State Output Enable Time	t_{pZL} t_{pZH}		—	10	18	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C				Ta = -40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t _{TLH} t _{THL}		2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time (D—Y)	t _{pLH} t _{pHL}		2.0	—	65	140	—	175	
			4.5	—	17	28	—	35	
			6.0	—	14	24	—	30	
Propagation Delay Time (D—W)	t _{pLH} t _{pHL}		2.0	—	70	140	—	175	
			4.5	—	18	28	—	35	
			6.0	—	15	24	—	30	
Propagation Delay Time (A, B, C—Y)	t _{pLH} t _{pHL}		2.0	—	80	180	—	225	
			4.5	—	23	36	—	45	
			6.0	—	19	31	—	38	
Propagation Delay Time (A, B, C—W)	t _{pLH} t _{pHL}		2.0	—	80	180	—	225	
			4.5	—	23	36	—	45	
			6.0	—	19	31	—	38	
3-State Output Enable Time	t _{pZL} t _{pZH}		2.0	—	40	105	—	130	
			4.5	—	13	21	—	26	
			6.0	—	10	19	—	22	
3-State Output Disable Time	t _{pLZ} t _{pHZ}		2.0	—	25	105	—	130	
			4.5	—	13	21	—	26	
			6.0	—	11	19	—	22	
Input Capacitance	C _{IN}		—	5	10	—	10	pF	
Power Dissipation Capacitance	C _{PD} (1)		—	69	—	—	—		

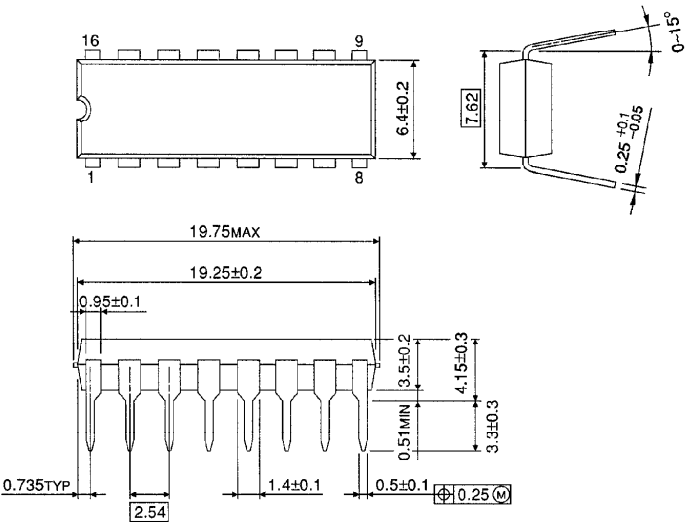
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

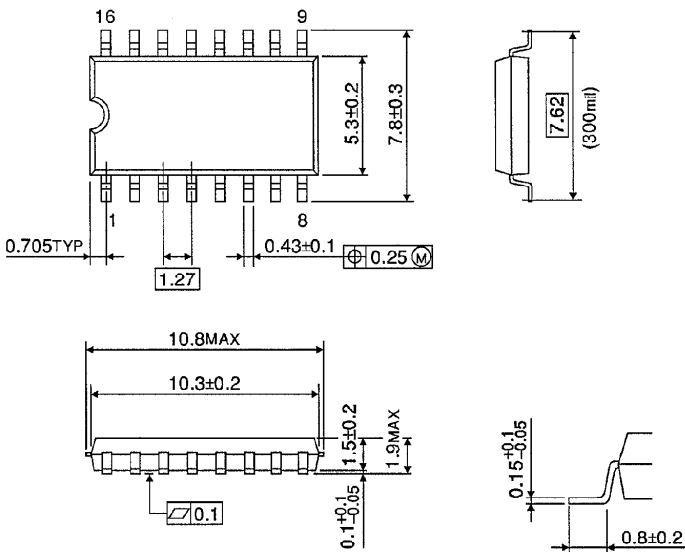
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm



Weight : 0.18g (Typ.)